Application note

L9663 operation in PSI5-P operation mode

Introduction

PSI5 is a standard for sensor interface in the Automotive field developed for safe critical airbag application and used then in other domains (Power Train, Chassis and safety applications).

STMicroelectronics is a member of the PSI5 Consortium and L9663 is the ST solution for PSI5 standalone transceiver supporting both 1.3 and 2.x revisions (see L9663 datasheet for details).

L9663 is capable of operating with different supplies configuration in order to match the application needs and optimize cost vs performance. For example, in case the needed supplies are not available in the ECU, the device is able to generate them from VB battery and a supply rail VDD with few external components.

Purpose of this document is to give guidelines for setting up an application with L9663 in PSI5 synchronous operation mode.

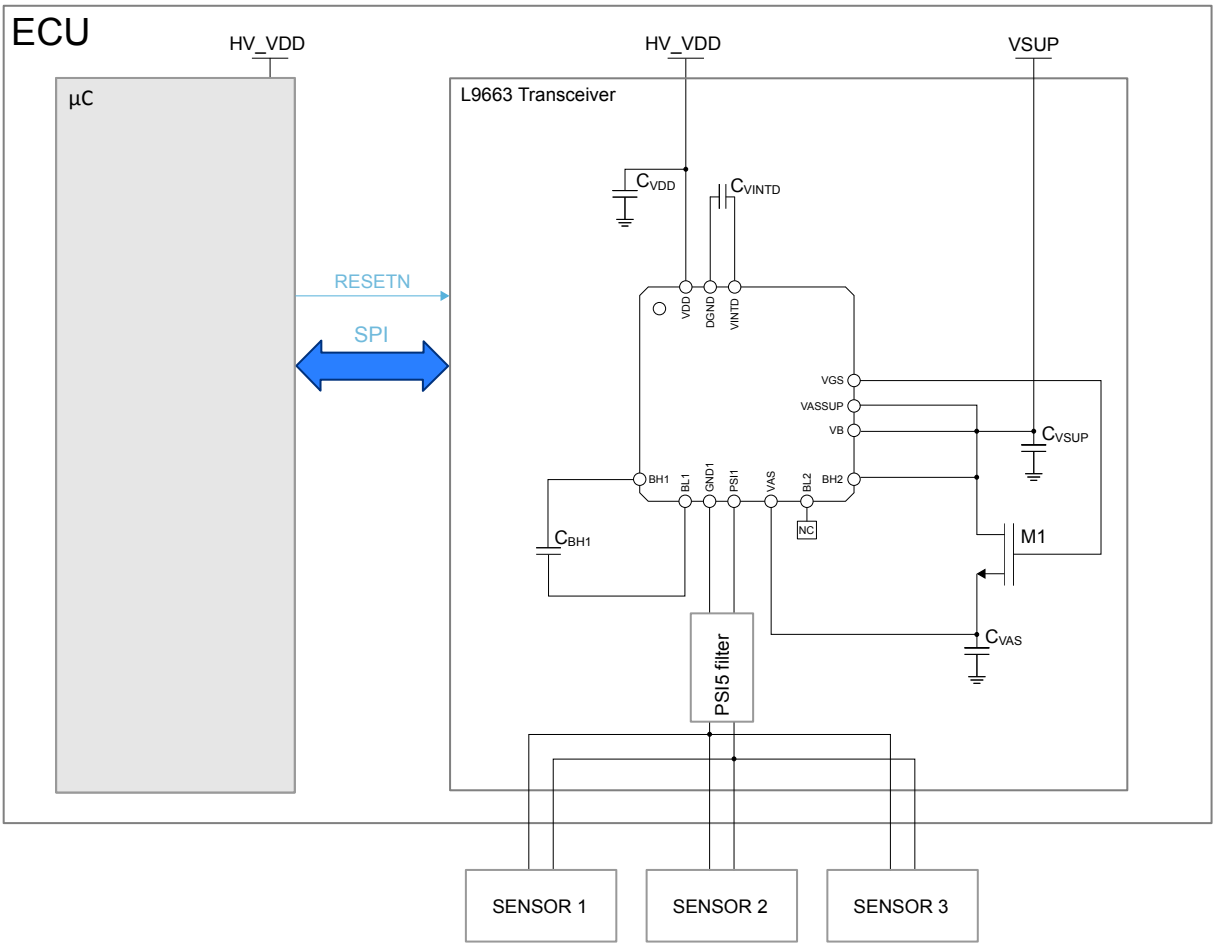
1 Application description

In case of synchronous sensor a typical system configuration is shown in Figure 1.
The present configuration is assumed for the rest of this document:

- PSI2 interface not used
- SPI mode used with polling mode readout (SYNCx not used, DOUTx not used)
- CLKIN not used

Notes will be present for applications which require different configurations.

Figure 1. PSI5P synchronous sensors application

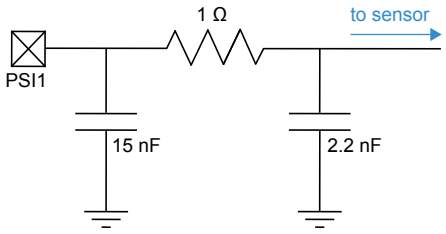


L9663 receives VDD from the microcontroller IO supply rail, while VSUP is connected to the battery line.
The connected sensors are considered to have a cumulative base current of max 35 mA.
The following parts could be used (20% tolerance, ceramic):

- CVAS = 4.7 µF
- CVINTD = 100 nF
- CVSUP = 2.2 µF || 100nF
- CVDD = 100 nF
- CBH1 = 10 µF
- M1 : ST STN4NF06L
- PSI5 filter

– CE = 15 nF
– RE2 = 1 Ω
– CL = 2.2 nF

Figure 2. PSI1 filter



In addition to the connection of Figure 1, the following guidelines are given for x = [1,2]:

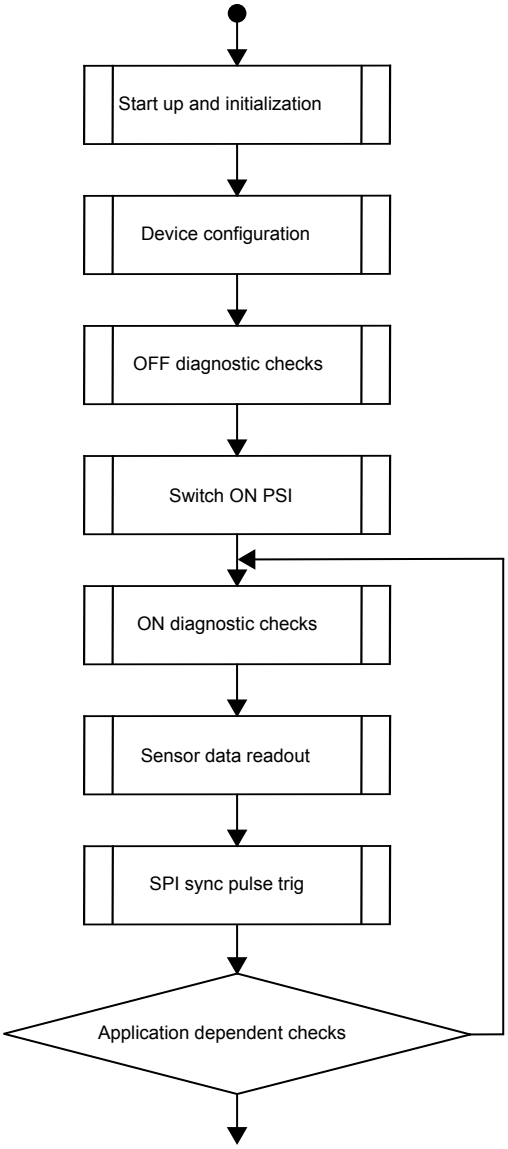
- CLKIN connected to GND
- PSI2 = OPEN
- BL2 open, BH2 connected to VSUP voltage (bootstrap capacitor not needed on PSI2)
- SYNCx open (SYNCx pin not used)
- DOUTx left OPEN in polling mode (they can be also connected to MCU GPIO in interrupt mode)

For general guidelines and connection please refer to Section 3 .

2 L9663 operation

Under the previous assumption, the simplified flow diagram described in Figure 3. L9663 simplified flow diagram will be taken as reference.

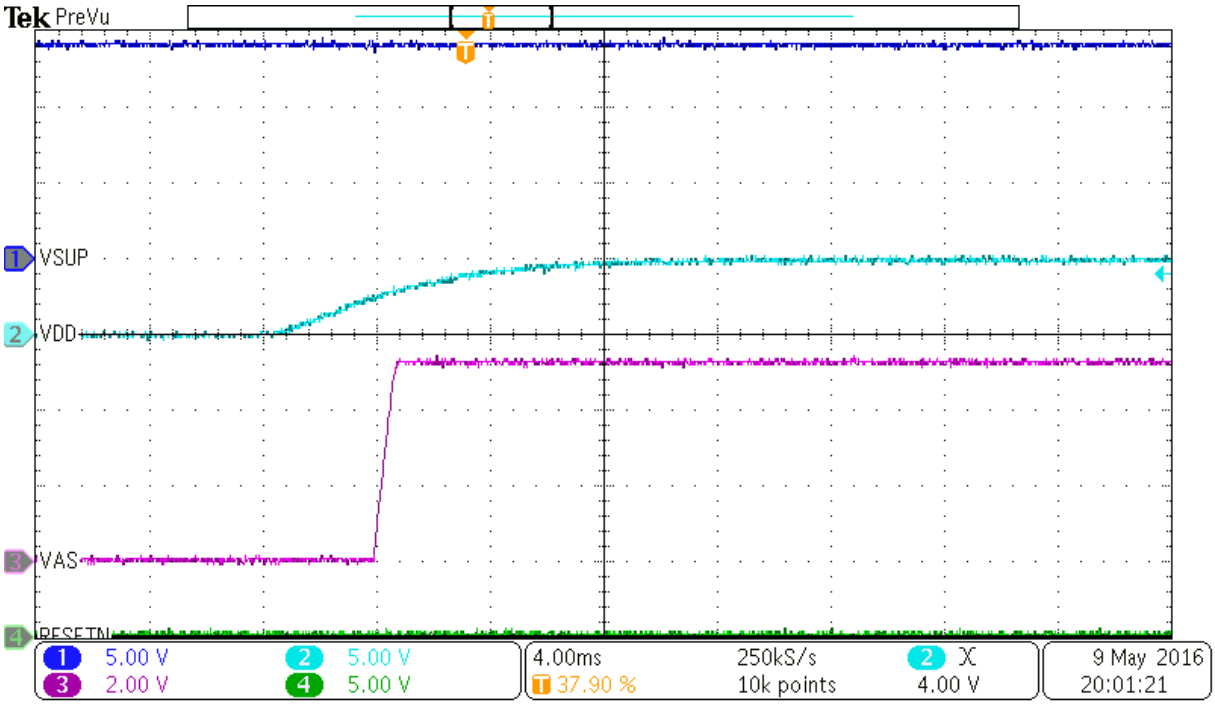
Figure 3. L9663 simplified flow diagram



2.1 Start up and initialization

After VSUP and VDD startup, the VAS is started automatically by the device while IC is still under logical reset as shown in Figure 4 and MCU holds low RESETN signal.

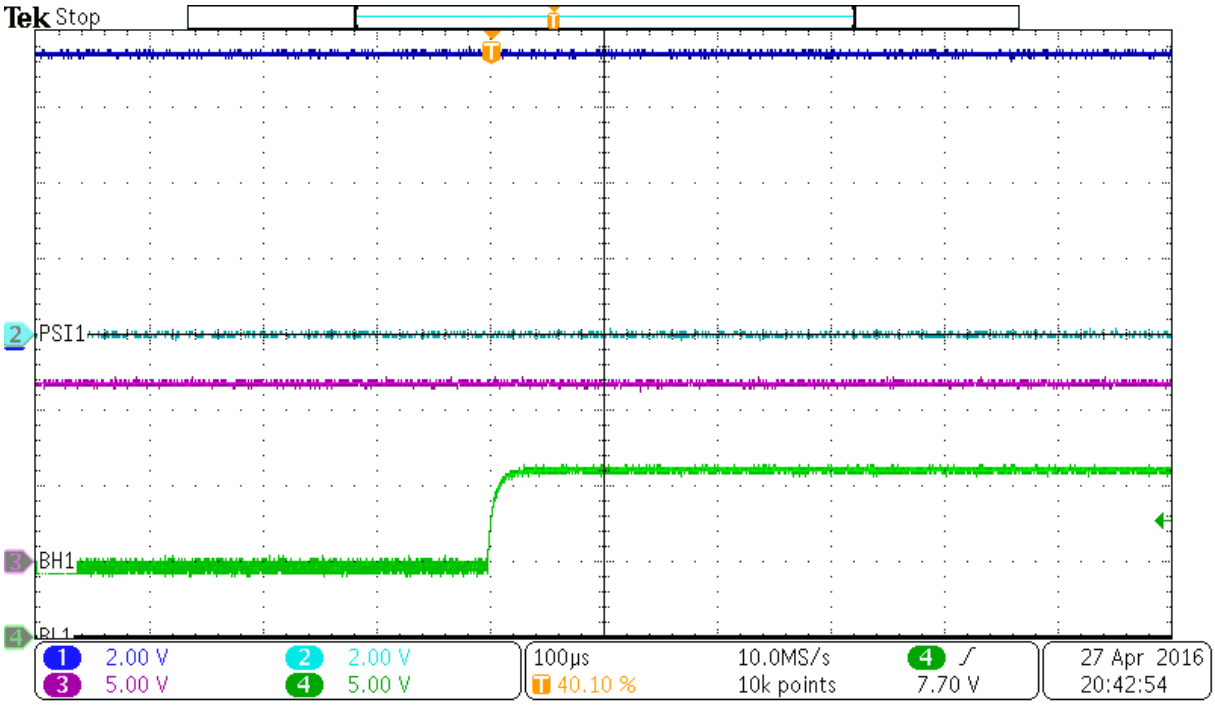
Figure 4. **Power up**



As soon as RESETN is released, the MCU needs to write the relevant L9663 registers according to 0 .

Regarding the power supplies, the internal bootstrap control circuits of the unused channel, need to be disabled by writing bit 12 of CH2_CR2 to ‘1’ (this will disable the circuit as shown in Figure 5) and in case the application requires a different voltage level from the 5.3 V default value, bit 0 of GCR1 needs to be changed accordingly.

Figure 5. **Bootstrap disable**



2.2 Device configuration

For synchronous operation the registers to be configured are shown in Table 1.

At the end of the configuration phase EOP command (0x1111) can be sent on DCR register to lock the relevant settings.

Table 1. L9663 relevant configuration register in synchronous mode

Address	Name	Description	Mandatory
0	RESERVED		-
1	GCR1	General config 1	Y
2	CHCNT	channel control	Y
7	UDB_CR	Upstream databf Config for PSI1/2	N
8	UDB1_1	PSI1: Upstream Data Buffer [63:48]	N
9	UDB1_2	PSI1: Upstream Data Buffer [47:32]	N
10	UDB1_3	PSI1: Upstream Data Buffer [31:16]	N
11	UDB1_4	PSI1: Upstream Data Buffer [15:0]	N
12	UDB2_1	PSI2: Upstream Data Buffer [63:48]	N
13	UDB2_2	PSI2: Upstream Data Buffer [47:32]	N
14	UDB2_3	PSI2: Upstream Data Buffer [31:16]	N
15	UDB2_4	PSI2: Upstream Data Buffer [15:0]	N
16	SYNC_PT	SYNC pulse timer PSI 1 / PSI 2	Y
17	CH1_CR1	PSI 1: Configuration register 1	Y
18	CH1_CR2	PSI 1: Configuration register 2	Y
19	CH1_CR3	PSI 1: Configuration register 3	Y
20	CH1_CR4	PSI 1: Configuration register 4	Y
21	SID1_TS13	PSI1: SID bits for Time slot 1 to 3	Y
22	SID1_TS46	PSI1: SID bits for Time slot 4 to 6	Y
23	TSM1_ES1	PSI1: Time for Earliest start of slot 1	Y
24	TSM1_ES2	PSI1: Time for Earliest start of slot 2	Y
25	TSM1_ES3	PSI1: Time for Earliest start of slot 3	Y
26	TSM1_ES4	PSI1: Time for Earliest start of slot 4	Y
27	TSM1_ES5	PSI1: Time for Earliest start of slot 5	Y
28	TSM1_ES6	PSI1: Time for Earliest start of slot 6	Y
29	TSM1_END6	PSI1: Time for slot 6 end	Y
30	DCR	Direct command register	Y
44	STS	Self test setting 1 : prog time	N
45	STSR	Self test setting 2 : runtime	N
46	ADVSET1	Settings for tracking ch1	N
47	ADVSET2	Settings for manchester , ch1, ch2	N
48	ADVSET3	Settings for tracking ch2	N

2.2.1 Time slot monitoring

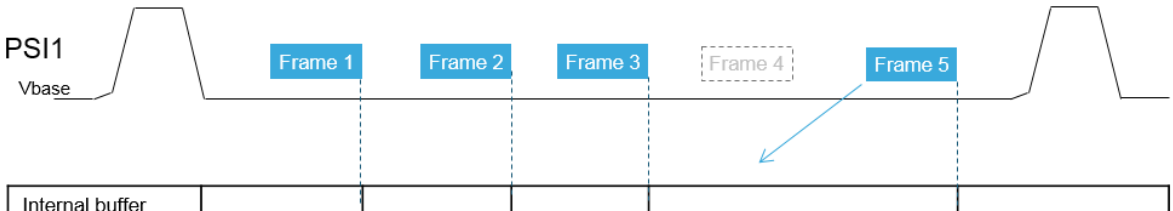
2.2.1.1 *TSM description*

L9663 provides several methods to implement timeslot monitoring (TSM) and the suitable choice depends on the application needs.

In case the application does not require frame monitoring, the feature can be disabled by writing the relative bits TSM1_SEL; in this case, data are stored in consecutive buffer positions as shown in Figure 6 and there is no need to configure TSM_Ex registers.

As an example, it's assumed that all frames are transmitted in the correct slot except for the missing frame 4; in this case the IC stores frame 5 data in the fourth buffer position and no other action is done on IC side.

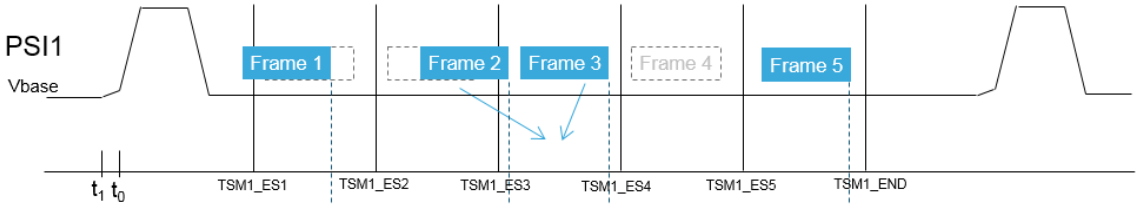
Figure 6. TMS disabled option



Internal buffer					
SensorData1	BE	Data1	Data1	Data1	Data1
SensorData2	BE	BE	Data2	Data2	Data2
SensorData3	BE	BE	BE	Data3	Data3
SensorData4	BE	BE	BE	BE	Data5
SensorData5	BE	BE	BE	BE	BE
SensorData6	BE	BE	BE	BE	BE

The most effective way to implement TSM is the so called simple TSM; this option allows the monitoring of timeslot end time as shown in Figure 7. In this picture, just for matter of monitoring explanation, it's assumed an early frame 1, a delayed frame 2 and a missing frame 4; in this case the IC stores frames in the configured timeslot according to the frame end and no other action is done on IC side. It's important to observe that selecting in an appropriate way the TSM_ESx all frames can be received without overwrite.

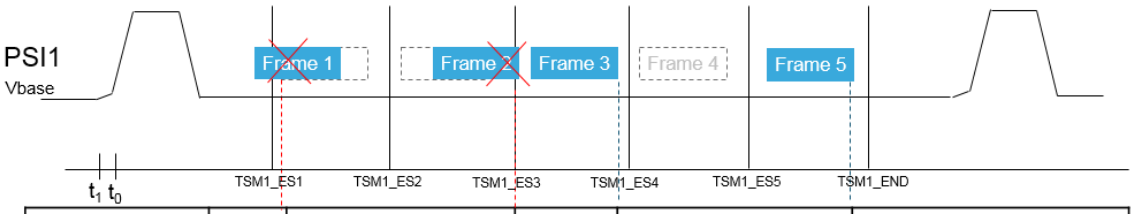
Figure 7. TSM simple option



Internal buffer					
SensorData1	BE	Data1	Data1	Data1	Data1
SensorData2	BE	BE	BE	BE	BE
SensorData3	BE	BE	Data2	Data3	Data3
SensorData4	BE	BE	BE	BE	BE
SensorData5	BE	BE	BE	BE	Data5
SensorData6	BE	BE	BE	BE	BE

The standard TSM option allows the monitoring of timeslot start time as shown in Figure 8. In this picture, just for matter of monitoring explanation, it's assumed an early frame 1, a delayed frame 2 and a missing frame 4; in this case the IC detects a manchster error with frames across the programmed slot.

Figure 8. TSM standard option



Internal buffer					
SensorData1	BE	MERR	MERR	MERR	MERR
SensorData2	BE	BE	MERR	MERR	MERR
SensorData3	BE	BE	BE	Data3	Data3
SensorData4	BE	BE	BE	BE	BE
SensorData5	BE	BE	BE	BE	Data5
SensorData6	BE	BE	BE	BE	BE

2.2.1.2 *TSM configuration*

Once the TSM option is selected, the IC must be configured accordingly, i.e. bits TSM1_SEL must be written as explained in Table 2 and TSM_Ex regs must be programmed with the correct meaning. In particular, the TSM_ES2 will monitor the ES2 when the standard option is selected, the LE1 when the simple option is chosen.

Table 2. TSM option selection

TSM1_SEL	Option
00, 11	TSM disabled
01	TSM standard
10	TSM simple

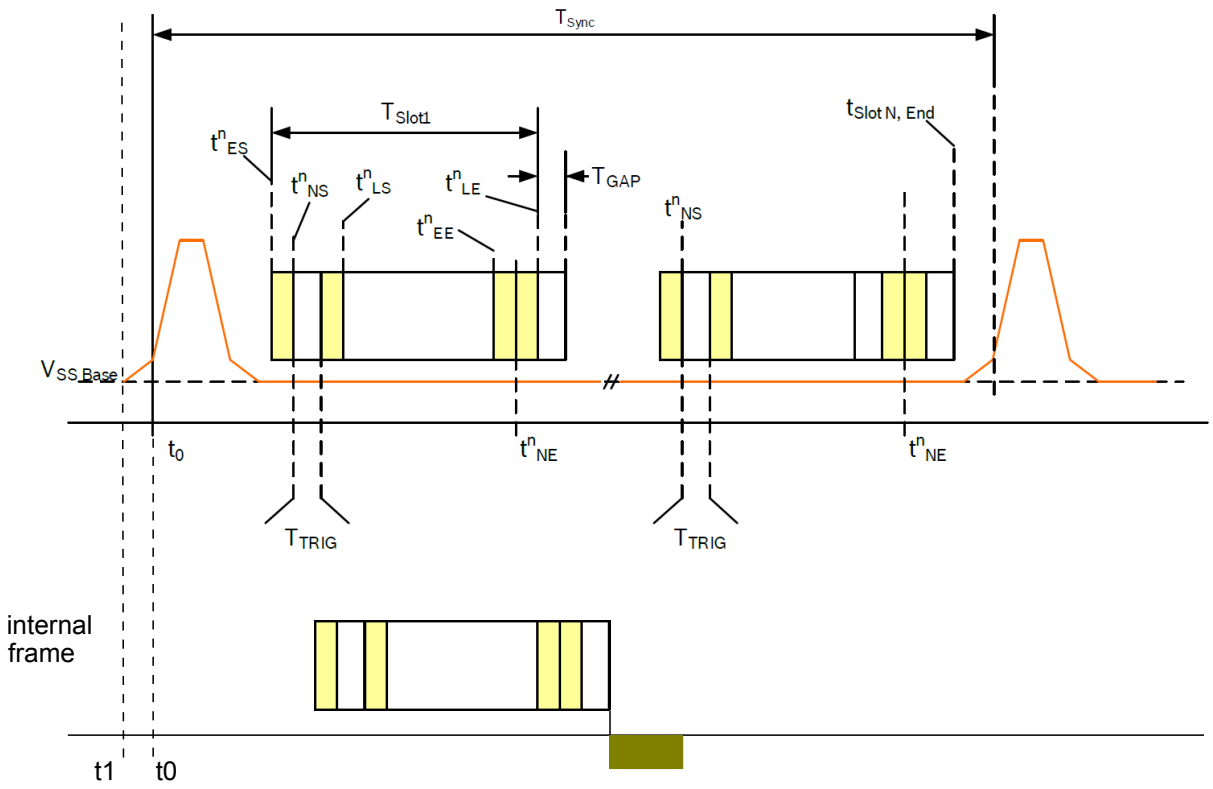
Table 3. TSM1_EX meaning

-	TSM disable	TSM standard	TSM simple
TSM1_ES1	DC	ES1	ES1(1)
TSM1_ES2	DC	ES2	LE1
TSM1_ES3	DC	ES3	LE2
TSM1_END	DC	LE3	LE3

1. *Tranceiver can accept end frames only after TSM1_ES1 time but no error is generated in case of frame start timing violation unlike the standard option (see Figure 7 for example).*

Let's see now how the TSM_Ex register must be programmed.

Figure 9. TSM configuration simple option



The following calculations apply for simple TSM with reference to Figure 9:

$$TSM1\_ES_1 \le \left(t^1_{ES} + t_{deglith}\right) \cdot (1 + CTT)^{-1} \quad (1)$$

$$TSM1\_ES_n \ge \left(t^n_{LE} - 1 + TGAP \cdot (1 + 20\%) + t_{latency\_DOUTx\_HF\_IIR} + t_{deglith} + |t_1|\right) \cdot (1 - CTT)^{-1}, \quad 1 < n < N \quad (2)$$

$$TSM1\_END \ge \left(t^N_{LE} + TGAP \cdot \left(1 + 20\%\right) + t_{latency\_DOUTx\_HF\_IIR} + t_{deglith} + |t_1|\right) \cdot (1 - CTT)^{-1} \quad (3)$$

Where:

N = 3 is the number of time slots

$t_{deglitch}$(max) = 1 µs

$|t_1|$ = 3 µs

tLatency_DOUTx_HF_IIR = 3.05 µs when selected baudrate is = 189 kbps

tLatency_DOUTx_HF_IIR = 3.6 µs when selected baudrate is = 125 kbps

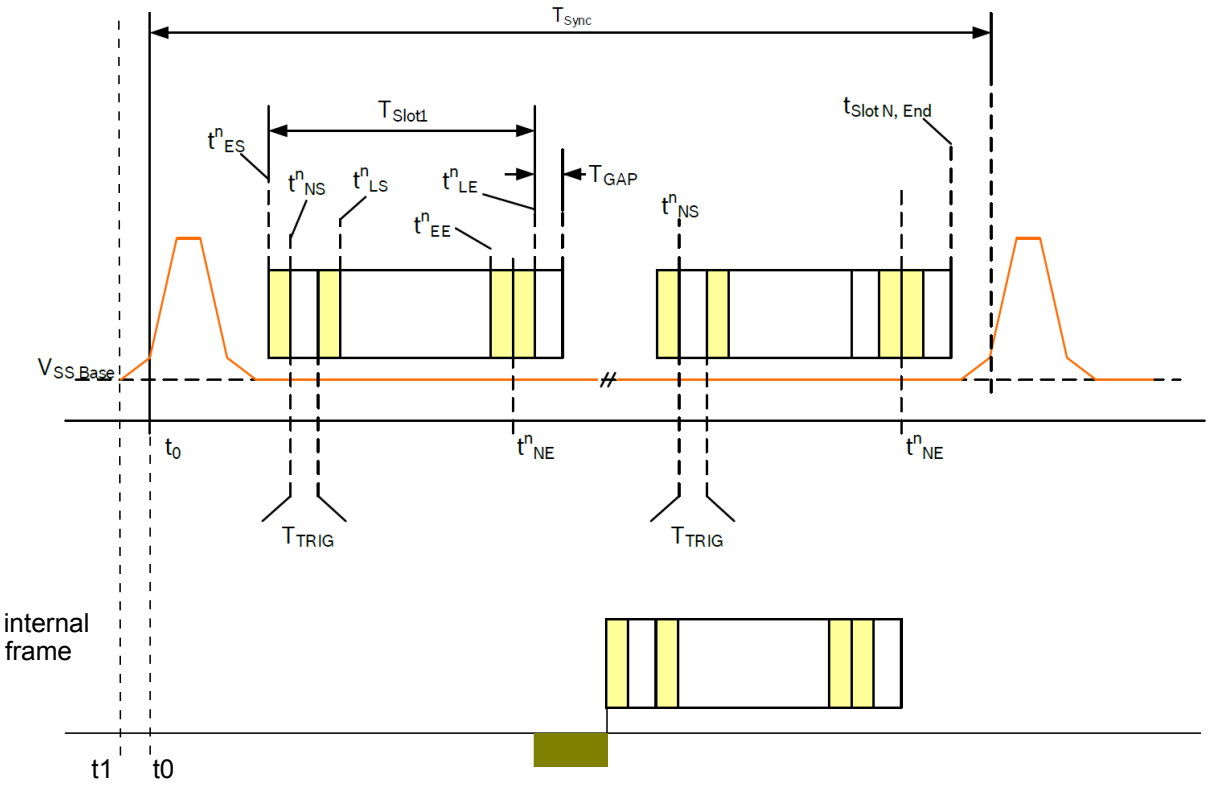
CTT is the L9663 clock tolerance

Note: For TSM1_ES1 a simplified wc formula is presented where min value of $t_{latency\_DOUTx\_HF\_IIR}$ is assumed to be 0; this parameter is not used for frame start monitoring as explained for simple TSM option.

Note: For TSM1_ESn and TSM1_END a simplified wc formula is presented where DOUT buffer delay is not extracted and taken as safe margin.

Note: Default option for start bit period measure is considered (wc).

Figure 10. TSM configuration standard option



The following calculations apply for standard TSM with reference to Figure 10:

$$TSM1\_ES_n \le \left(t^n_{ES} + t_{deglith}\right) \cdot (1 + CTT)^{-1} \quad 1 \le n \le N \quad (4)$$

$$TSM1\_END \geq \left(t^{N}_{LE} + TGAP \cdot \left(1 + 20\%\right) + t_{latency\_DOUTx\_HF\_IIR} + t_{deglith} + |t_1| \right) \cdot (1 - CTT)^{-1} \quad (5)$$

Note: in case sync pulse trigger generator is used with triggering via pulse timer the transceiver clock tolerance determines effective sync pulse duration and with default settings, transceiver clock tolerance is 5%:

*TSync, min = TSync*0,95; TSync, max = TSync*1,05*

In case a 1% transceiver clock tolerance is needed external input CLKIN is needed and the following values are obtained:

*TSync, min = TSync*0,99; TSync, max = TSync*1,01*

For example, suppose the settings for PSI5-P10P-500/3L Mode reported in Table 4 must be applied.

Table 4. PSI5-P10P-500/3L timings

N°	Parameter	Symbol	Remark	Min.	Nom.	Max.	Unit
1	Sync signal period Maximum tolerance of sync signal period +/-1	T_{Sync}		495		505	µs
				t^{N}_{Ex}	t^{N}_{Nx}	t^{N}_{Lx}	
2	Slot 1 start time	t^{1}_{xS}	Related to t_0	44			µs
3	Slot 1 end time	t^{1}_{xE}	Related to t_0				µs
4	Slot 2 start time	t^{1}_{xS}	Related to t_0	181.3			µs
5	Slot 2 end time	t^{1}_{xE}	Related to t_0				µs
6	Slot 3 start time	t^{1}_{xS}	Related to t_0	328.9			µs
7	Slot 3 end time	t^{1}_{xE}	Related to t_0			492	µs

Note: This example is calculated with a standard sensor clock tolerance of 5%.

In this case a possible choice for simple TSM with default option set could be:

- TSM1_ES1 = 41
- TSM1_ES2 = 209
- TSM1_ES3 = 364
- TSM1_END = 536

While all the other ones are set to 0.

2.3 OFF diagnosis

Before switching on the interface, the MCU must ensure that the VAS voltage is inside the functional operative range (i.e. no VAS_UV fault is present) otherwise L9663 does not allow switching on the channels.

Taking into account the device mission profile, a drift can be induced in the parameters of VAS regulator and monitor. In case the device works in the configuration where “VAS, VB, VASSUP connected to VSUP, VSYNCx generated by bootstrap, no external MOS, VGS pin open” and by considering the aging effect:

- VAS Regulator: the regulator must be disabled via SPI (if not used) to avoid drift of the VAS regulated voltage.
- VAS Monitor: If VAS voltage is different from the internally selected voltage (via SPI), a drift is generated on VAS monitor circuitry. The following parameters are extracted considering this drift. In order to avoid VAS monitor parameters degradation, the VAS voltage should be chosen as follows:
  - If VAS is in the range of 4.3 V - 6.45 V => (VVASU_low, VVASO_low) by selecting VAS = 5.3 V through SPI (default).

– If VAS is in the range of 6.45 V - 8 V => (VVASU_inc, VVASO_inc) by selecting VAS = 7.6 V through SPI.
– If VAS is in the range of 8 V - 16 V => It is suggested to select (VVASU_inc, VVASO_inc) by selecting VAS = 7.6 V.

However, the following relaxed parameters must be considered:

Table 5. Electrical parameters

-	Min.	Max.	Unit
VVASU_low	4.2	5.2	V
VVASU_inc	6	7.5	V
VVASO_low	6	7.5	V
VVASO_inc	7.5	9.5	V

For details about other possible OFF diagnostic please refer to the device DS.

2.4 Sensor ON phase

After configuration and a diagnostic phase, the channel can be switched on writing on CHCNT channel control register.

2.4.1 Init data Reading

L9663 provides a useful procedure to automatically read init data under predefined assumptions. For detailed assumption please refer to the device DS.

2.4.2 ON diagnostic

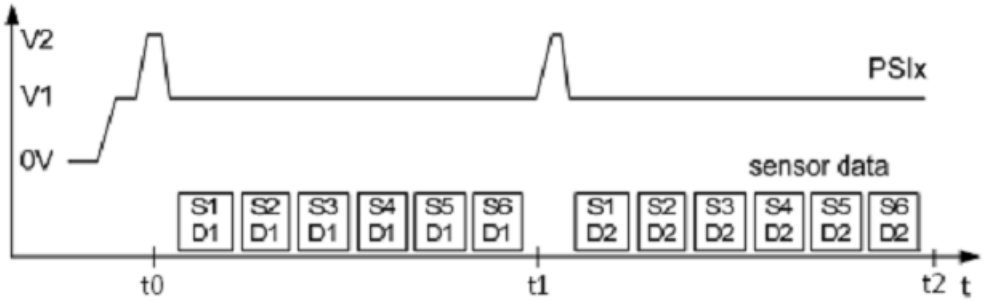
L9663 implements a set of ON diagnostic checks that can be used to monitor and detect deviations from the expected operation. For details about available ON diagnostic features please refer to the device DS.

2.5 Sensor data readout

When channel is ON, MCU can start reading sensor data through the SPI interface accessing the sensor data registers.

In synchronous mode these registers are working as depicted in Figure 11; in order to avoid data-mixing between different cycle times the data must be fetched by the µC before the next transmission cycle starts.

Figure 11. **Sensor data buffer in SYNC mode**



Time/Sensor	t0	t1	t2
SensorData1	Buffer Empty	D11	D12
SensorData2	Buffer Empty	D21	D22
SensorData3	Buffer Empty	D31	D32
SensorData4	Buffer Empty	D41	D42
SensorData5	Buffer Empty	D51	D52
SensorData6	Buffer Empty	D61	D62

In case a further GPIO is available on MCU side, L9663 allows the usage of DOUT1 pin as interrupt: DOUT1 is raised when all internal data buffers are full and is set to low when all the buffers are empty.

3 PCB layout recommendation

3.1 Layout guidelines

Layout should be done with particular care in order to keep BHx pin away from GND lines:

- GND1, GND2, DGND connected together to GND plane
- TM connected to GND
- TQFP32 option: NC-4 open, NC-7 open, NC-13 open, NC-18 open, NC-28 open
- QFN28 option: NC-6 open, NC-19 to GND

Revision history

Table 6. **Document revision history**

Date	Version	Changes
11-Jul-2019	1	Initial release.

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