

15V, 1.5W buck converter based on VIPER26K

Introduction

The **STEVAL-VP26K01B** is a 15 V – 1.5 W power supply in buck topology featuring the **VIPER265KDTR** offline high voltage converter, specifically developed for ultra-wide input range solutions.

The evaluation board has the following characteristics:

- Ultra-wide range: 90–600 V_{AC} or 60–870 V_{DC}
- Meets IEC55022 Class B conducted EMI even with a reduced EMI filter, thanks to the frequency jittering feature
- RoHS compliant

Some of the main features of the VIPER265KDTR include:

- 1050 V avalanche rugged Power MOSFET
- Embedded HV start-up
- 60 kHz fixed switching frequency with jittering
- Embedded error amplifier internally referenced to 3.3 V
- Current mode PWM controller with drain current limit protection for easy compensation
- Several protection mechanisms:
 - delayed overload protection (OLP)
 - open loop failure protection
 - thermal shutdown with hysteresis

All protections are in auto restart mode

Figure 1. STEVAL-VP26K01B evaluation board top and bottom



1 Features and specifications

Table 1. STEVAL-VP26K01B electrical specifications

Parameter	Min.	Typ.	Max.	Unit
AC main input voltage	90	-	600	VAC
DC main input voltage	60	-	870	VDC
Main frequency (fL)	47	-	63	Hz
Output Voltage	13.5	15	16.5	V
Output Current	-	-	0.1	A
Rated output power	-	1.5	-	W
Output ripple voltage	-	-	100	mV
Ambient operating temperature	-	-	60	°C

The power supply is set in buck topology. The input section includes resistor R1 for inrush current limiting, two diodes in series (D1 and D2) and an LC filter (C1, L1) for rectification and EMC suppression.

The FB pin is the inverting input of the internal transconductance error amplifier, internally referenced to 3.3 V, which allows the straightforward setting output voltage value through the R5-R6 voltage divider between the output terminal and the FB pin, according to the following equation:

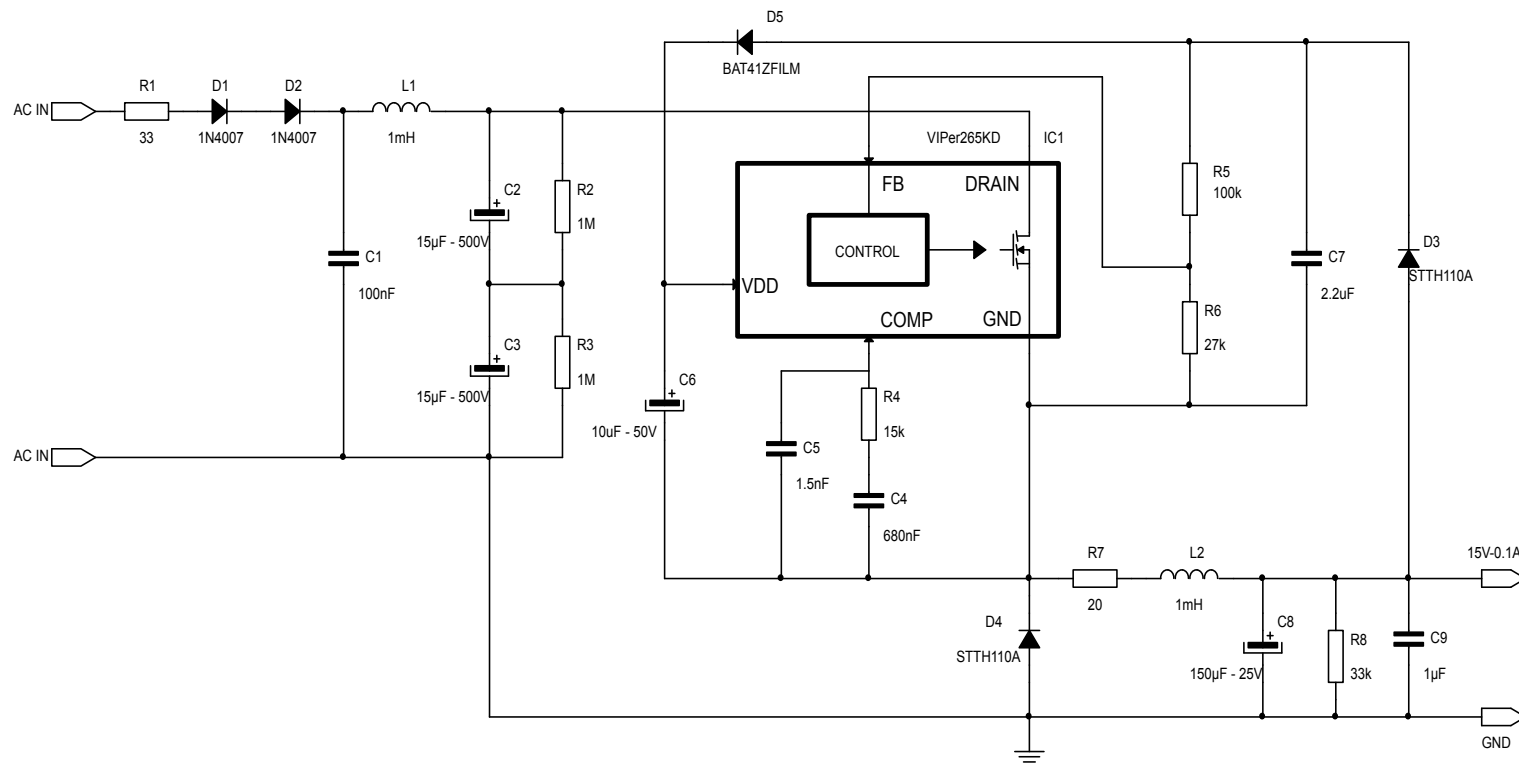
$$V_{OUT} = 3.3V \cdot \left(1 + \frac{R_5}{R_6}\right) \quad (1)$$

The R4, C4 and C5 compensation network is connected between the COMP pin (which is the output of the error amplifier) and the GND pin.

The bleeder resistor R8 provides about 0.5 mA minimum load in order to avoid overvoltage when the output load is disconnected. This value is a trade-off between output voltage increase and the extra power consumption under no load conditions.

Schematic diagrams

Figure 2. STEVAL-VP26K01B schematic diagram



1.2 Bill of materials

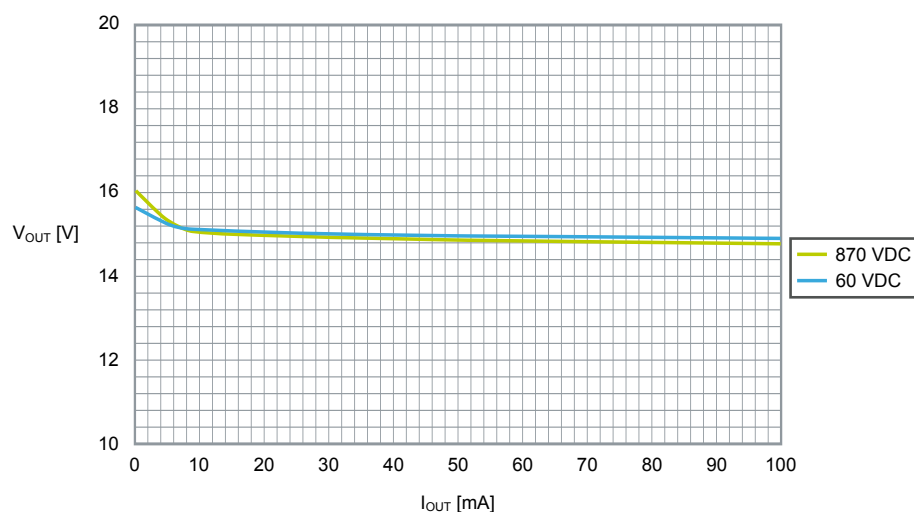
Table 2. Bill of materials

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
1	1	C1	100nF, 1000V, ±10%	Ceramic Capacitor X7R, SMD 1812	Kemet	C1812X104KDRCTU
2	2	C2, C3	15µF, 500V, ±20%	ELCAP, Dia 12.5mm x H 26.5mm Pitch 5mm	Nichicon	UCY2H150MHD1TO
3	1	C4	680nF, 50V, ±10%	Ceramic Capacitor X7R, 0805	Kemet	C0805C684K5RACTU
4	1	C5	1.5nF, 50V, ±10%	Ceramic Capacitor X7R, 0603	Wurth Elektronik	885012206084
5	1	C6	10µF, 50V, ±20%	ELCAP, Dia 5mm x H 11mm Pitch 2mm	Rubycon	50YXF10M5X11
6	1	C7	2.2µF, 50V, ±10%	Ceramic Capacitor X5R, 0805	TDK	C2012X5R1H225K125AB
7	1	C8	150µF, 25V, ±20%	ELCAP, Dia 6.3mm x H 12.5mm Pitch 2.5mm	Rubycon	25ZLH150MEFC6.3X11
8	1	C9	1µF, 25V, ±10%	Ceramic Capacitor X7R, 0805	Murata	GRM21BR71E105KA99L
9	2	D1, D2	1000V, 1A	Rectifier Diode, DO-41	Taiwan Semiconductor	1N4007G R0
10	2	D3, D4	1000V, 1A	High Voltage Ultrafast Rectifier Diode, SMA	ST	STTH110A
11	1	D5	100V	Schottky Diode, SOD-123	ST	BAT41ZFILM
12	1	IC1	1050 V	Offline HV Converter, SO16	ST	VIPER265KDTR
13	1	L1	1mH, ±5%	Radial Inductor, Dia 8mm x H 10mm Pitch 5mm	Wurth Elektronik	7447728102
14	1	L2	1mH, ±5%	Radial Inductor with 4 Pins, Dia 11mm x H 19mm	Wurth Elektronik	7447231102
15	1	M1	1000V, 30A	Input Connector, Through Hole 7.6mm pitch	Phoenix Contact	1731721
16	1	M2	250Vca, 13.5A	Output Connector, Through Hole 5.08mm pitch	TE Connectivity	282837-2
17	1	R1	33Ω, 4W, ±5%	Fusible Resistor 20ppm/°C, Through Hole	Stackpole Electronics	SP3AJT33R0
18	2	R2, R3	1MΩ, 0.66W, ±5%	Stand. Film Resistor 200ppm/°C, 1206	Panasonic	ERJP08J105V
19	1	R4	15kΩ, 0.1W, ±1%	Stand. Film Resistor 100ppm/°C, 0603	Panasonic	ERJU03F1502V

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
20	1	R5	100k Ω , 0.1W, $\pm 1\%$	Stand. Film Resistor 100ppm/ $^{\circ}\text{C}$, 0603	Panasonic	ERJ3EKF1003V
21	1	R6	27k Ω , 0.1W, $\pm 1\%$	Stand. Film Resistor 100ppm/ $^{\circ}\text{C}$, 0603	Panasonic	ERJ3EKF2702V
22	1	R7	20 Ω , 1W, $\pm 0.1\%$	Stand. Film Resistor 25ppm/ $^{\circ}\text{C}$, 1206	Vishay	PHP01206E20R0BST5
23	1	R8	33k Ω , 0.1W, $\pm 1\%$	Stand. Film Resistor 100ppm/ $^{\circ}\text{C}$, 0603	Panasonic	ERJU03F3302V

1.3 Output voltage characteristics

Figure 3. Output voltage load regulation at minimum and maximum DC input voltage



2 Typical waveforms

The GND voltage and output inductor current waveforms in full load condition are shown in the following images for minimum and maximum AC input voltages.

Figure 4. GND voltage and output inductor current at full load at 90V_{AC}

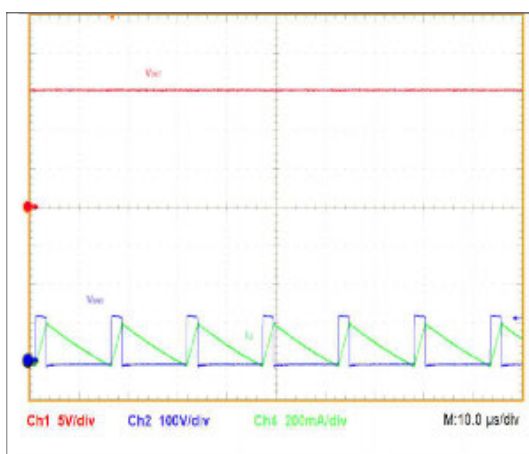
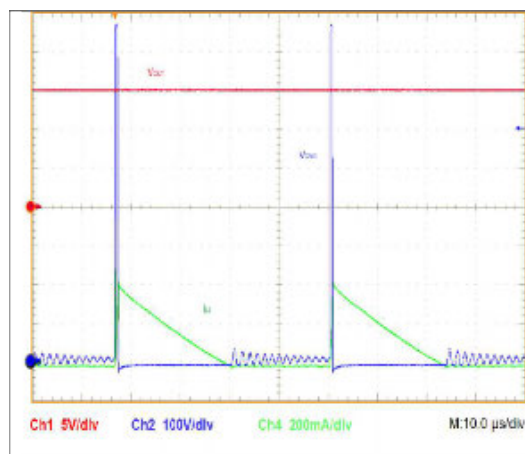


Figure 5. GND voltage and output inductor current at full load at 600V_{AC}



The GND voltage and output inductor current waveforms in full load condition are shown in the following images for the two nominal input voltages.

Figure 6. GND voltage and output inductor current at full load at 115V_{AC}

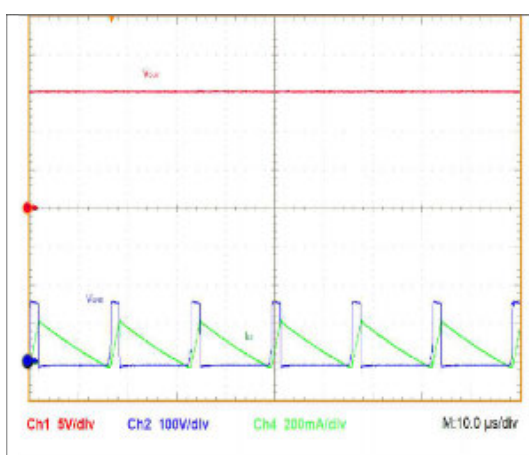
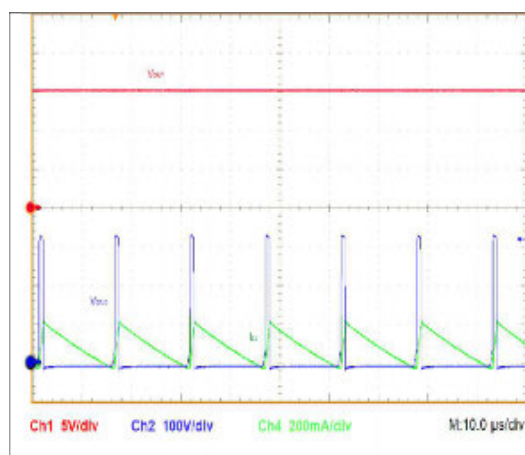


Figure 7. GND voltage and output inductor current at full load at 230V_{AC}



The output voltage ripple at the switching frequency is shown in the following images for full load at nominal voltages.

Figure 8. Output voltage ripple at full load at 115V_{AC}

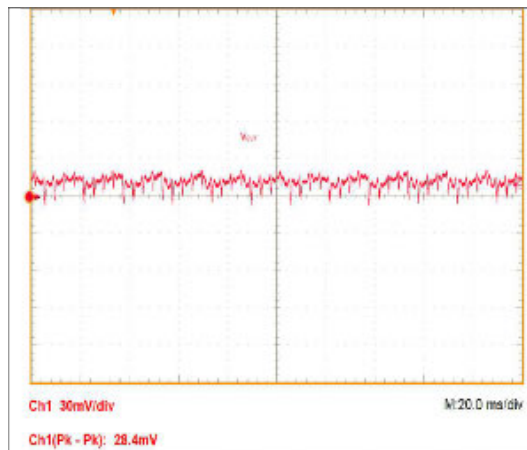
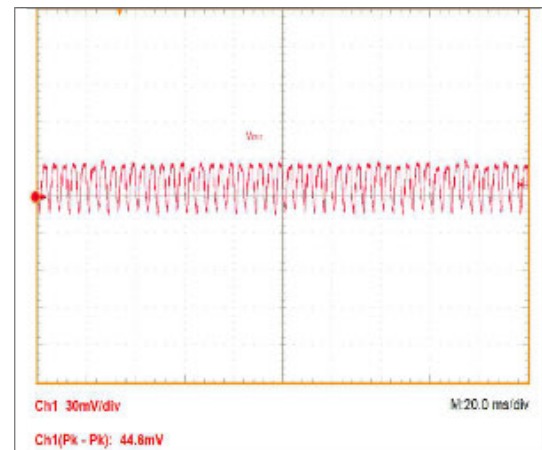


Figure 9. Output voltage ripple at full load at 230V_{AC}



The output voltage ripple at the switching frequency is shown in the following images for no load at nominal voltages.

Figure 10. Output voltage ripple at no load at 115V_{AC}

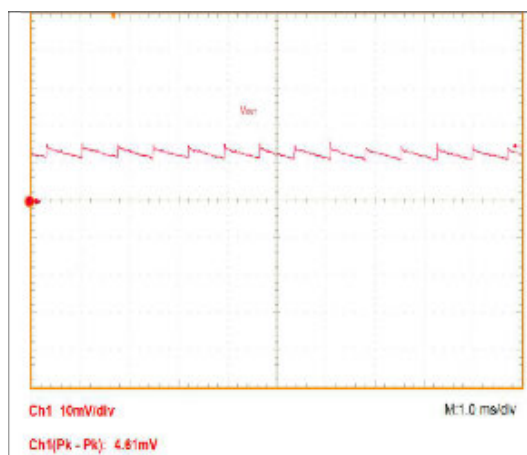
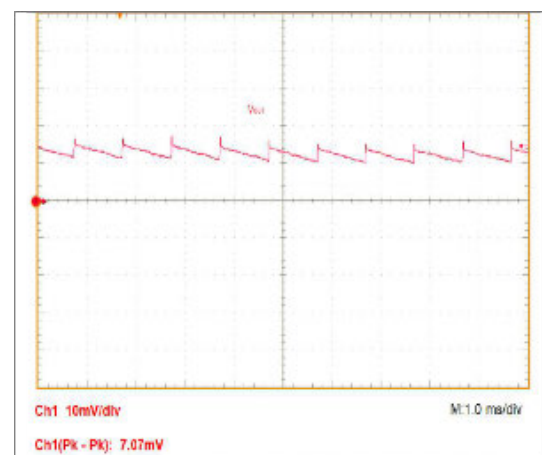


Figure 11. Output voltage ripple at no load at 230V_{AC}



2.1 Dynamic step load regulation

In any power supply, it is important to measure the output voltage when the converter is subjected to dynamic load variations in order to ensure appropriate stability free of overvoltage and undervoltage events.

The test is performed by varying the output load from 0 to 0.1 A (100% of nominal value) for both nominal input voltages.

In the tested conditions, no abnormal oscillations were observed on the output, and over- and under-shoot were well within acceptable values.

Figure 12. Dynamic step load (I_{OUT} from 0 to 0.1A) at 115V_{AC}

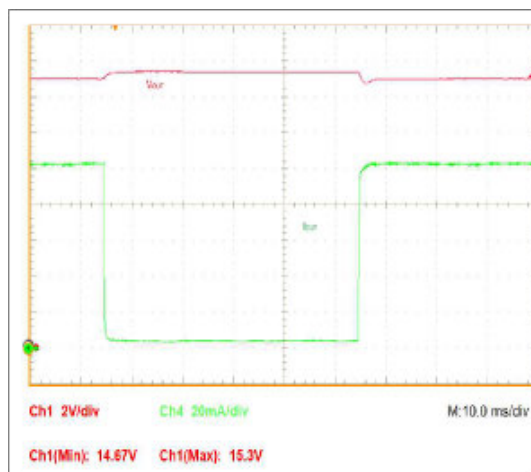
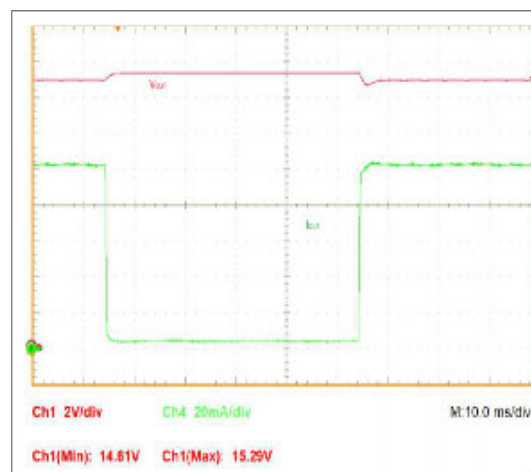


Figure 13. Dynamic step load (I_{OUT} from 0 to 0.1A) at 230V_{AC}



3 Startup

When the converter starts, the output capacitor is discharged and needs time to reach the steady state condition. During this time, the power demand from the control loop is at its maximum, leading to a deep continuous operating mode of the converter.

Another consideration is that when the MOSFET is switched on, it cannot be switched off before the minimum on time (T_{ON_MIN}) has elapsed. Because of the deep continuous working mode of the converter, an excessive drain current during T_{ON_MIN} can stress the component of the converter, the device itself, and the output inductor. Output inductor saturation may also occur under these conditions.

To avoid these negative effects, the [VIPER265KDTR](#) implements an internal soft-start feature. As the device starts to work, the drain current is allowed to increase from zero to the maximum value gradually, regardless of the control loop request.

The soft-start time t_{SS} is internally set at 8.5 ms (typical value). The R7 resistor further limits the current through the output inductor (L2) to avoid saturation during startup phase.

The following figures show the soft-start phase of the present converter at maximum load, for nominal input voltages (115V_{AC} and 230V_{AC}) and maximum input voltage (600V_{AC}).

Figure 14. Startup at 115V_{AC}, full load

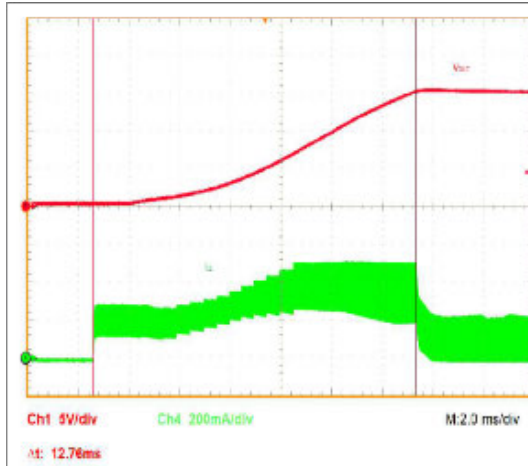


Figure 15. Startup at 115V_{AC}, full load - zoom

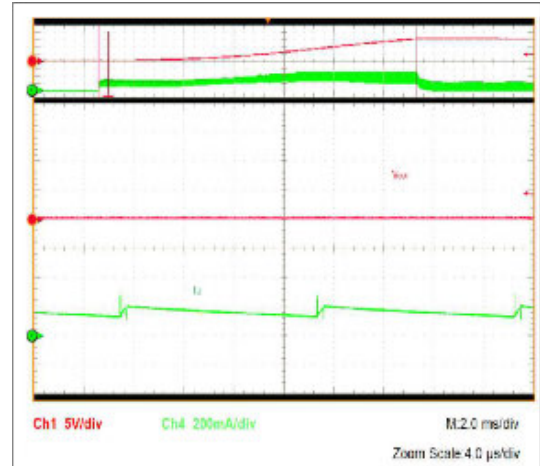


Figure 16. Startup at 230V_{AC}, full load

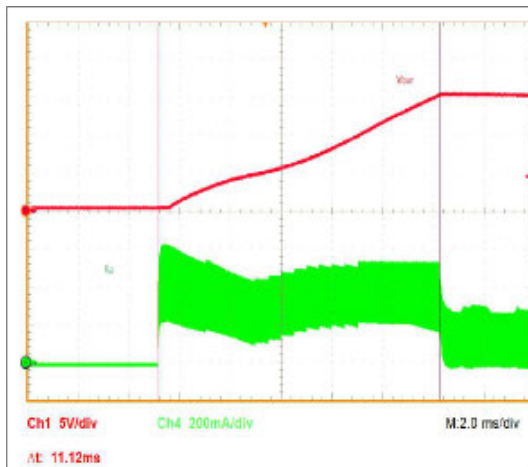


Figure 17. Startup at 230V_{AC}, full load - zoom

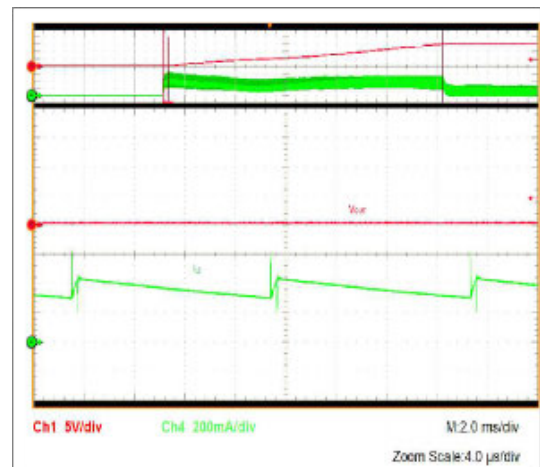


Figure 18. Startup at 600V_{AC}, full load

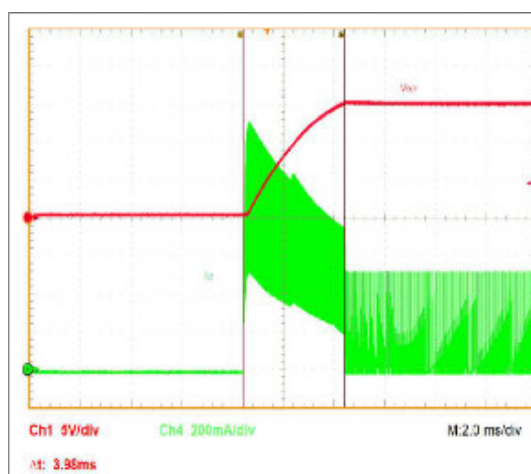
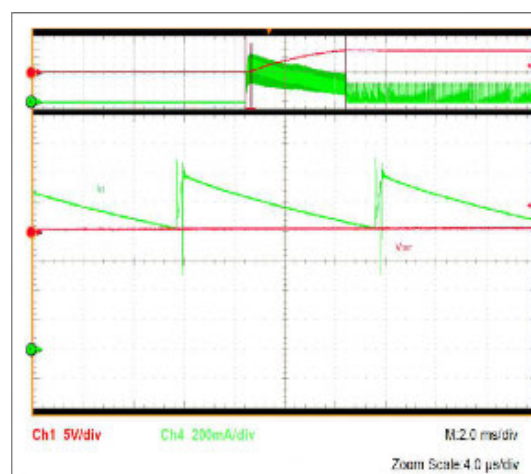


Figure 19. Startup at 600V_{AC}, full load - zoom



4 Protection features

4.1 Overload and short circuit protection

When the load power demand increases, the feedback loop reacts by increasing the voltage on the COMP pin. In this way, the PWM current set point increases and the power delivered to the output rises. This process ends when the delivered power equals the load power request.

In case of overload or output short circuit, the drain current value reaches the I_{DLIM} . For every cycle that this condition is met, an internal OCP counter is incremented and the protection is tripped if the overload condition persists for time t_{OVL} (50 ms typical). The power section is turned off and the converter is disabled for time $t_{RESTART}$ (1s typical). After this time has elapsed, the IC resumes switching and the protection continues to be triggered indefinitely if the fault condition remains. This ensures a low converter restart attempt rate, providing safe operation with extremely low power throughput and avoiding IC overheating in case of repeated overload events.

Figure 20. Overload event, OLP tripping

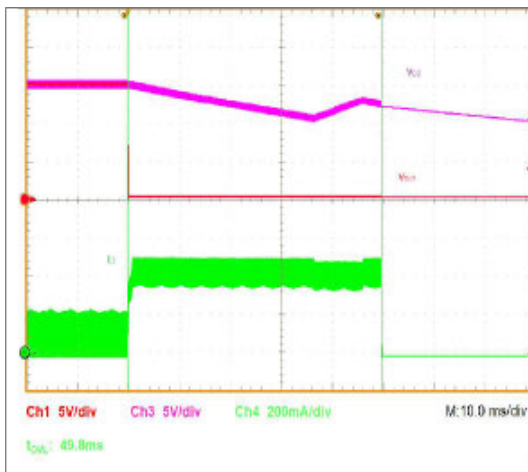
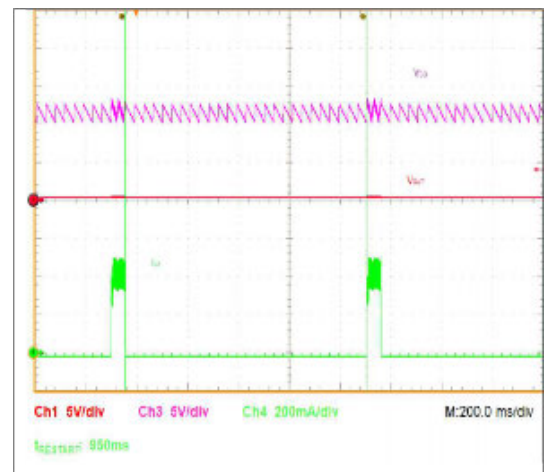
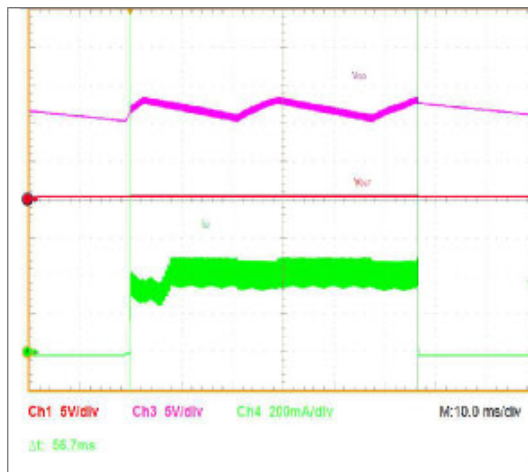
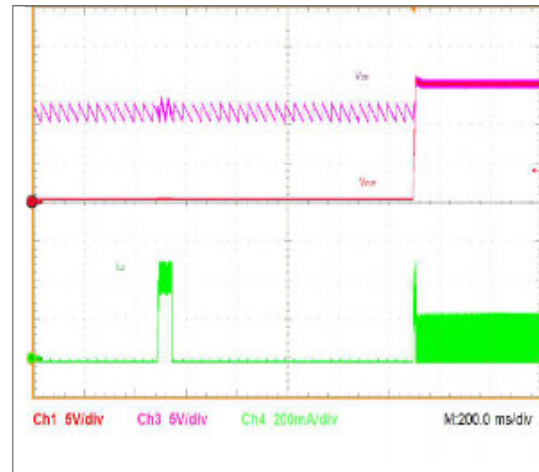


Figure 21. Overload event, continuous overload



Furthermore, the internal soft start function is invoked at startup after protection tripping.

After the fault is removed, the IC resumes working normally. If the fault is removed before the protection is triggered during t_{SS} or t_{OVL} , the counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped. If the short circuit is removed during $t_{RESTART}$, the IC waits until $t_{RESTART}$ has elapsed before resuming switching.

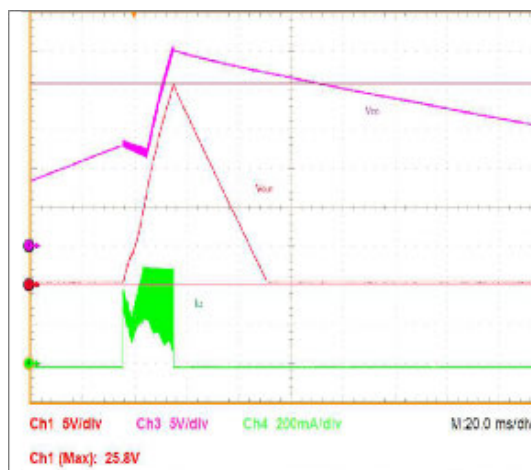
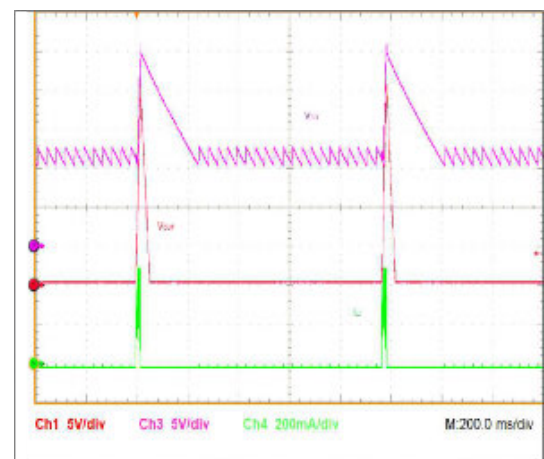
Figure 22. Overload event, t_{SS} and t_{OVL}

Figure 23. Overload event, fault removed and autorestart


4.2 Feedback loop failure protection

As the loop fails (R5 open or R6 shorted), the output voltage increases and the **VIPER265KDTR** runs at its maximum current limitation. The voltage on V_{DD} pin also increases as it is linked to the V_{OUT} voltage through diode D5.

If voltage V_{DD} increases up to the internal V_{DD} clamp threshold (23.5 V minimum) with a clamp current injected on the pin greater than the latch threshold I_{DDol} (4 mA minimum), and the **VIPER265KDTR** operates at its drain current limitation, a fault signal is internally generated and the device stops switching even if t_{OVL} hasn't elapsed yet.

The failure of the loop is simulated by opening the high-side resistor of the output voltage divider (R5). The same behavior can be induced by shorting the low-side resistor (R6).

Figure 24. Feedback loop failure protection - tripping

Figure 25. Feedback loop failure protection - steady-state


5 Conducted noise measurements

The **VIPER265KDTR** frequency jittering feature allows the spectrum to be spread over frequency bands rather than being concentrated on single frequency value. Especially when measuring conducted emission with the average detection method, the level reduction can be several dB μ V.

A pre-compliance test for the EN55022 (Class B) European normative was performed and average measurements of the conducted noise emissions at full load and nominal mains voltages are shown in the following figures.

Figure 26. CE average measurement at 115V_{AC} full load

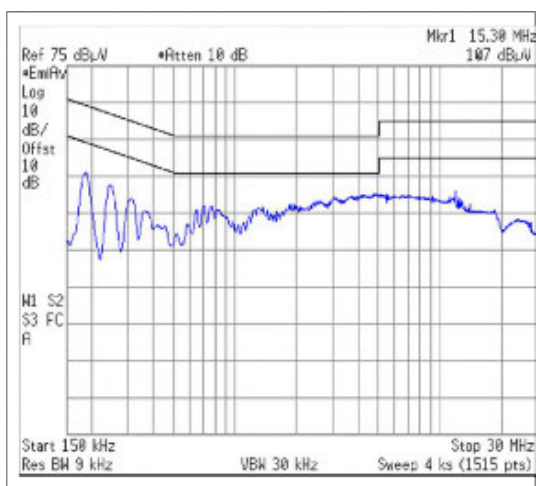
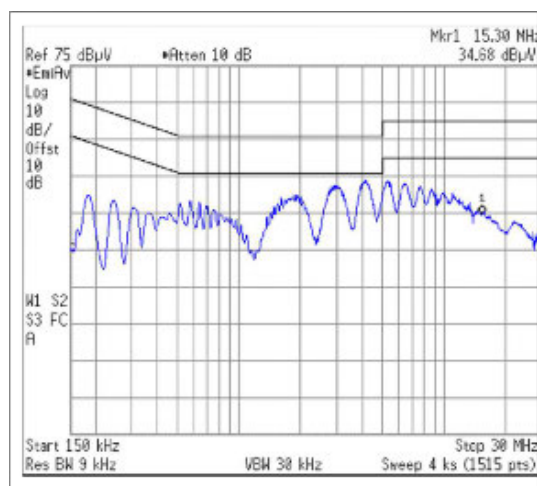


Figure 27. CE average measurement at 230V_{AC} full load



6 Thermal measurements

A thermal analysis of the board has been performed using an IR camera for the two nominal input voltages (115V_{AC} and 230V_{AC}) and at minimum and maximum AC input voltage, in full load condition. The results are shown below.

Figure 28. Thermal map at 90V_{AC}

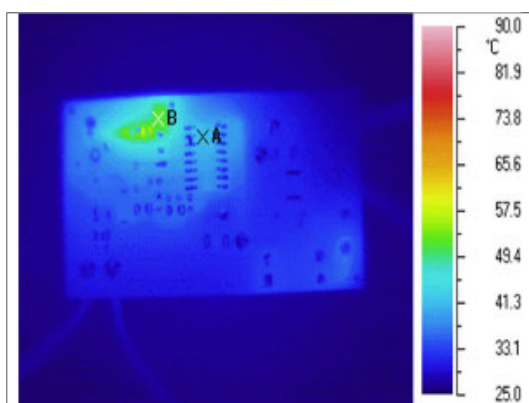


Figure 29. Thermal map at 115V_{AC}

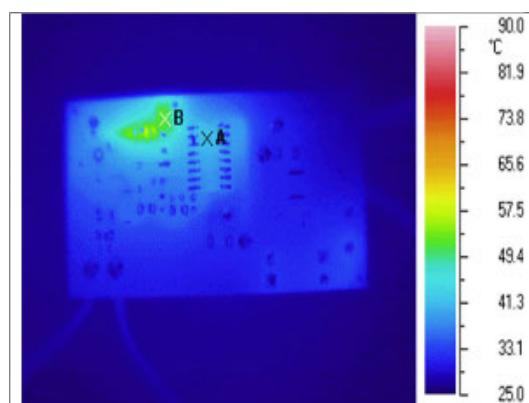


Figure 30. Thermal map at 230V_{AC}

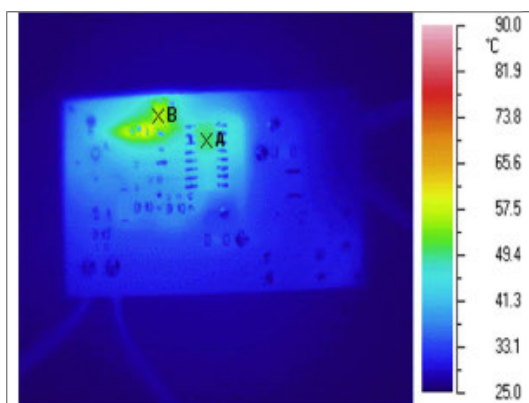


Figure 31. Thermal map at 600V_{AC}

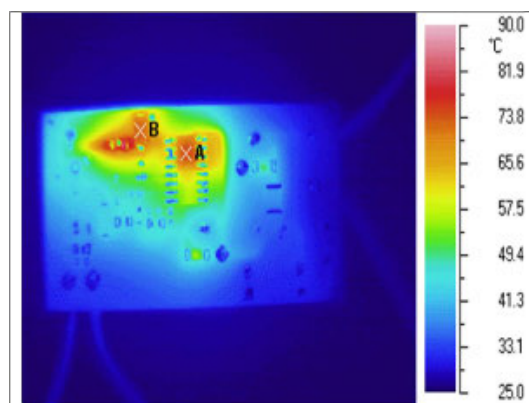


Table 3. Temperature at points A and B at different loads

Reference	Point	Temperature (°C)			
		90V _{AC}	115V _{AC}	230V _{AC}	600V _{AC}
VIPER265KDTR	A	41.9	41.9	50.2	74.6
Buck diode	B	52.4	52.2	56.8	73.4

7 Conclusions

An ultra-wide input range buck converter has been described and characterized, with the bench results showing good performance in terms of line and load regulation.

The [STEVAL-VP26K01B](#) reference design meets the EN55022 – Class B EMI regulation standard using a simple and low-cost LC input filter.

Appendix A Feedback loop calculation guidelines

A.1 CCM buck converter transfer function

The control-to-output transfer function of the buck converter in CCM, $G_{VC}(s)$, is given by:

$$G_{VC}(s) = H_0 \cdot \frac{1 + \frac{s}{\omega_{Z1}}}{1 + \frac{s}{\omega_{P1}}} \cdot G_{HF}(s) \quad (2)$$

Gain, poles and zero are defined below:

$$H_0 = \frac{R_0}{H_{COMP}} \cdot \frac{1}{1 + \frac{R_0 \cdot T_S}{L} \cdot (0.5 - D)} \quad (3)$$

$$\omega_{Z1} = \frac{1}{R_C \cdot C_0} \quad (4)$$

$$\omega_{P1} = \frac{1}{R_0 \cdot C_0} + \frac{T_S}{L \cdot C_0} \cdot (0.5 - D) \quad (5)$$

$$G_{HF}(s) = \frac{1}{1 + \frac{s}{Q_0 \cdot \omega_0} + \frac{s^2}{\omega_0^2}} \quad (6)$$

$$\omega_0 = \frac{\pi}{T_S} \quad (7)$$

$$Q_0 = \frac{1}{\pi \cdot (0.5 - D)} \quad (8)$$

The term $G_{HF}(s)$ defines the high frequency characteristic, which is represented by a double pole located at half the switching frequency and is described by a second order system equation. It can also model the effect of the instability for the CCM buck with duty-cycle higher than 50%.

When the crossover frequency of the loop gain is low, $G_{HF}(s)$ is usually negligible.

A.2 Compensation design

To compensate the CCM buck, we use a type-2 compensator with the integrator effect to provide the high DC gain to minimize static error, and a pole-zero pair to boost the phase according the phase margin target.

The compensator is determined using a manual pole-zero placement technique where the zero is placed in the vicinity of the power stage dominant pole to cancel its effect, and the pole position is adjusted to achieve the required phase margin.

Follow the procedure below to design the compensation with a type 2 compensator:

Step 1. Select the crossover frequency f_C and the phase margin Φ_m .

Step 2. Evaluate the gain and phase of the plant at crossover frequency.

$$G_{VC}(f_C) = |G_{VC} \cdot (2 \cdot \pi \cdot f_C)| \quad (9)$$

$$\Phi_{VC}(f_C) = \arg[G_{VC} \cdot (2 \cdot \pi \cdot f_C)] \quad (10)$$

Step 3. The compensated open-loop gain must attain the unit gain at f_C with the required phase margin, so the compensator must be designed in order to have following gain and phase (at f_C):

$$G_C(f_C) = |G_C \cdot (2 \cdot \pi \cdot f_C)| = \frac{1}{G_{VC}(f_C)} \quad (11)$$

$$\Phi_C(f_C) = \arg[G_C \cdot (2 \cdot \pi \cdot f_C)] = 90 - 180 + \Phi_m - \Phi_{VC}(f_C) \quad (12)$$

Step 4. Cancel the pole of the plant, $f_{P(p)}$, by placing the zero of the compensator $f_{Z(c)}$ in the region $\alpha = 1$ to 5

$$f_{Z(c)} = \frac{\omega_{Z(c)}}{2 \cdot \pi} = \alpha \cdot f_{P(p)} \quad (13)$$

Step 5. Place the pole of the compensator to boost the phase and to obtain the desired phase margin

$$f_{P(C)} = \frac{f_C}{\tan \left[\tan^{-1} \left(\frac{f_C}{f_{Z(C)}} \right) - \Phi_C(f_C) \right]} \quad (14)$$

Step 6. Calculate the gain G_{C0}

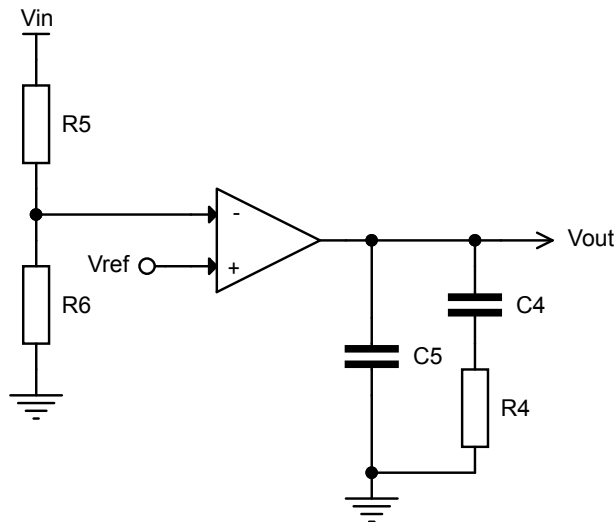
$$G_{C0} = G_C(f_C) \frac{\omega_C \cdot \sqrt{1 + \left(\frac{f_C}{f_{P(C)}} \right)^2}}{\sqrt{1 + \left(\frac{f_C}{f_{Z(C)}} \right)^2}} \quad (15)$$

The design of $G_C(s)$ is complete.

A.3 Summary of the compensator

The following figure shows the schematic of the Type 2 amplifier used in the VIPER265KDTR.

Figure 32. Type 2 compensator with OTA



The transfer function of this compensator can be expressed as the following:

$$G_C(s) = \frac{R_6 \cdot g_m}{(R_5 + R_6) \cdot (C_5 + C_4)} \cdot \frac{1 + s \cdot R_4 \cdot C_4}{s \cdot \left[1 + s \cdot R_4 \cdot \left(\frac{C_4 \cdot C_5}{C_4 + C_5} \right) \right]} \quad (16)$$

The first component to be chosen is resistor R_5 , which must be high enough to render the current offset entering in the inverting pin negligible, but low enough to ensure that other compensation components do not have to be too large. Resistor R_6 is fixed to set the DC operating point of the loop. Of course, both R_5 and R_6 play a role in determining the gain of the compensator.

Step 1. Set the values for R_5 and R_6 .

$$R_5 = 100 \text{ k}\Omega \quad (17)$$

$$R_6 = 27 \text{ k}\Omega \quad (18)$$

Step 2. Calculate the value for C_5

$$C_5 = \frac{f_{Z1}}{f_{P1}} \cdot \frac{R_6 \cdot g_m}{G_{C0} \cdot (R_5 + R_6)} \approx 1.9 \text{ nF} \quad (19)$$

The selected value for C_5 is:

$$C_5 = 1.5 \text{ nF} \quad (20)$$

Step 3. Calculate C_4

$$C_4 = \frac{R_6 \cdot g_m}{G_{C0} \cdot (R_5 + R_6)} - C_5 \approx 992 \text{ nF} \quad (21)$$

The selected value for C_4 is:

$$C_4 = 680 \text{ nF} \quad (22)$$

Step 4. Calculate R_4

$$R_4 = \frac{1}{2 \cdot \pi \cdot f_{Z1} \cdot C_4} \approx 18 \text{ k}\Omega \quad (23)$$

The selected value for R_4 is:

$$R_4 = 15 \text{ k}\Omega \quad (24)$$

The resulting crossover frequency f_C and the phase margin Φ_m are:

$$f_C \approx 2.4 \text{ kHz} \quad (25)$$

$$\Phi_m \approx 74 \quad (26)$$

Appendix B Layout guidelines and design recommendations

An appropriate PCB layout is essential for the correct operation of any switch-mode converter. It ensures the delivery of clean signals to the IC and higher immunity to external and switching noise, as well as reducing radiated and conducted electromagnetic interference, all of which help a given solution satisfy EMC requirements. Below are some general concepts to keep in mind when designing SMPS circuit layouts.

Separate signal and power tracks:

- Traces carrying signal currents should generally be run at a distance from other tracks carrying pulsed currents or with rapidly changing voltages.
- Signal ground traces should be connected to the IC signal ground, GND, using a single "star point", placed close to the IC.
- Power ground traces should be connected to the IC power ground, GND.
- The compensation network should be connected to the COMP, maintaining the trace to GND as short as possible.
- In two-layer PCBs, it is a good practice to route signal traces on one PCB side and power traces on the other side.

Filter sensitive pins and crucial points on the circuit:

- A small high-frequency bypass capacitor to GND might be useful to get a clean bias voltage for the signal part of the IC and protect the IC itself during EFT/ESD tests.
- A low ESL ceramic capacitor (a few hundred pF up to 0.1 μ F) should be connected across VCC and GND, placed as close as possible to the IC.
- With flyback topologies, when the auxiliary winding is used, it is suggested to connect the VCC capacitor on the auxiliary return and then to the main GND using a single track.

Keep power loops as confined as possible:

- Minimize the area circumscribed by current loops where highly pulsed currents flow in order to reduce its parasitic self-inductance and the radiated electromagnetic field; this will greatly reduce the electromagnetic interferences produced by the power supply during the switching.
- In a flyback converter the most critical loops are:
 - The one with the input bulk capacitor, the power switch and the power transformer
 - the one with the snubber.
 - the one with the secondary winding, the output rectifier and the output capacitor.
- In a buck converter the most critical loop is:
 - The one with the input bulk capacitor, the power switch, the power inductor, the output capacitor and the free-wheeling diode.

Reduce line lengths as any wire will act as an antenna:

- With the very short rise times exhibited by EFT pulses, any antenna has the capability of receiving high voltage spikes. Shorter lines reduce the level of radiated energy received and lower the spikes resulting from electrostatic discharges. This will also keep both resistive and inductive effects to a minimum.
- All traces carrying high currents, especially if pulsed (tracks of the power loops), should be as short and wide as possible.

Optimize track routing:

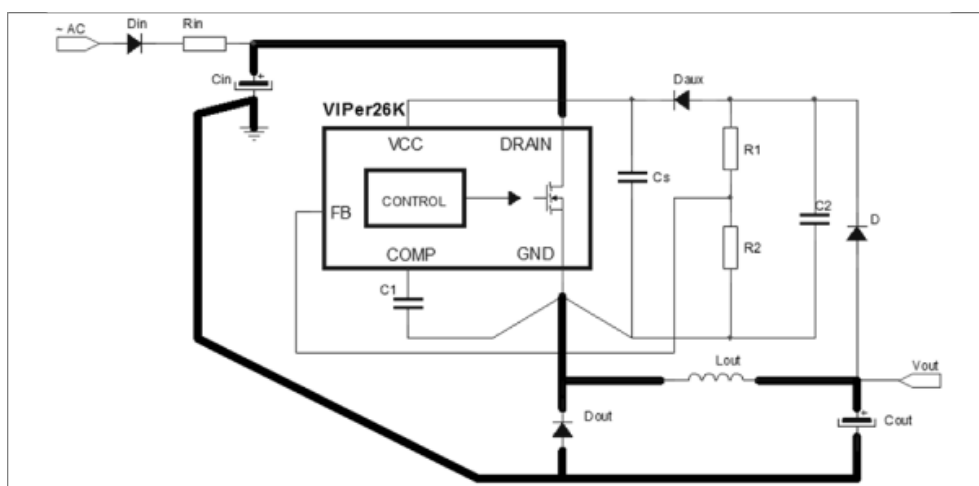
- as levels of pickup from static discharges are likely to be greater closer to the extremities of the board, it is wise to keep any sensitive lines away from these areas.
- Input and output lines will often need to reach the PCB edge at some stage, but they can be routed away from the edge as soon as possible where applicable.
- Since vias are considered inductive elements, they should be kept to a minimum in signal paths and avoided in power paths.

Improve thermal dissipation:

- An adequate copper area must be provided under the DRAIN pins to dissipate heat
- It is not recommended to place large copper areas on the GND.

Finally, in order to improve immunity against fast transient and capacitive noise injection, since pin number 4 is mechanically connected to the controller die pad of the frame, it is highly recommended to connect it to GND.

Figure 33. Recommended routing for buck converter



Revision history

Table 4. Document revision history

Date	Version	Changes
05-Sep-2019	1	Initial release.
20-Sep-2019	2	Minor text edits. Updated Eq. (12)

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