Introduction

The microcontrollers (MCUs) from the STM32WB Series can support an external power amplifier (PA) to provide higher output power.

This document details the modifications to implement in the Cortex®-M4 firmware, to allow the external PA to be driven by the MCU.

This application note is based on the SKY66118-11 PA from Skyworks Solutions (max output power = 20 dBm).
1 Hardware

This document applies to the STM32WB Series Arm® Cortex® core-based microcontrollers.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

The following SKY66118-11 pins must be managed (see the figure and the table below):
- CTX pin to switch the PA in transmission or reception
- CSD pin to enable or disable the PA
- VCTRL pin to control the output power (1.6 V < V_{CTRL} < 3.6 V, not represented in the figure below)

![Figure 1. SKY66118-11 block diagram](image)

Refer to the SKY66118-11 datasheet available on Skyworks web site for more details.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Description</th>
<th>CSD</th>
<th>CTX</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>All off (Sleep mode)</td>
<td>0</td>
<td>0 or 1</td>
</tr>
<tr>
<td>1</td>
<td>Transmit mode</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>Bypass mode</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

The CTX pin must be connected to GPIO PB0 (Port B, pin 0) of the STM32WB Series MCU. The CSD pin is connected to another GPIO.
**CTX pin**

For the CTX pin, the code below must be added in the Cortex-M4 firmware, in the initialization section of the GPIOs:

```c
GPIO_InitTypeDef GPIO_InitStruct;

// Enable GPIOB clock for CTX pin
__HAL_RCC_GPIOB_CLK_ENABLE();

// configure the GPIO PB0 in AF6 to be used as RF_TX_MOD_EXT_PA
GPIO_InitStruct.Pull = GPIO_NOPULL;
GPIO_InitStruct.Mode = GPIO_MODE_AF_PP;
GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_HIGH;
GPIO_InitStruct.Alternate = GPIO_AF6_RF_DTB0;
GPIO_InitStruct.Pin = GPIO_PIN_0;
HAL_GPIO_Init(GPIOB, &GPIO_InitStruct);
```

The CTX signal is managed by the BLE stack (transmission/reception), so there is nothing to add for this functionality.

Check that, in the Cortex-M4 firmware, PB0 is not used by another resource (for example, on the Nucleo board in the P-NUCLEO-WB55 pack, PB0 is used by LED2). If this occurs, this resource must be disabled.

**CSD pin**

The GPIO chosen to be connected to the CSD pin must be configured in the Cortex-M4 firmware, in the initialization section of the GPIOs (PA0 example):

```c
// Enable GPIOA clock for CSD pin */
__HAL_RCC_C2GPIOA_CLK_ENABLE();
__HAL_RCC_GPIOA_CLK_ENABLE();

// configure the GPIO which will be managed by M0 stack to enable Ext PA
GPIO_InitStruct.Pull = GPIO_NOPULL;
GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_PP;
GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_HIGH;
GPIO_InitStruct.Pin = GPIO_PIN_0;
HAL_GPIO_Init(GPIOA, &GPIO_InitStruct);
```

The Cortex-M4 firmware has also to inform the Cortex-M0+ firmware on which GPIO must be managed with the function:

- `SHCI_C2_ExtpaConfig((uint32_t)GPIOA, GPIO_PIN_0, EXT_PA_ENABLED_HIGH, EXT_PA_ENABLED);` when the PA is used.
- `SHCI_C2_ExtpaConfig((uint32_t)GPIOA, GPIO_PIN_0, EXT_PA, EXT_PA_ENABLED_HIGH, EXT_PA_DISABLED);` when the PA is not used.

**Note:** The selected PA must have a turn-on time lower than 300 μs.
### Revision history

#### Table 2. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>30-Sep-2019</td>
<td>1</td>
<td>Initial release.</td>
</tr>
<tr>
<td>16-Apr-2020</td>
<td>2</td>
<td>Updated:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Section 1 Hardware</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Section 2 Firmware</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Classification of the document</td>
</tr>
</tbody>
</table>
Contents

1 Hardware ................................................................. 2
2 Firmware ............................................................... 3
Revision history ........................................................ 4
Contents ................................................................... 5