5 V/100 mA high voltage optimized buck-converter based on VIPER013BLSTR

Introduction

The STEVAL-VP013B1B is an AC-DC power supply in buck topology featuring the VIPER013BLSTR off-line high voltage converter, specifically developed for non-isolated SMPS to perform voltage conversion from the main line down to 5 V output voltage.

The VIPER013BLSTR low current consumption and low V_{CC} supply voltage allows extremely low input power consumption under no load and light load conditions.

The IC pulse skip feature eliminates the inductor flux-runaway typical of a buck converter startup phase.

The VIPER013BLSTR features:

- 800 V avalanche rugged power section
- integrated HV-startup current generator
- on-board soft-start
- PWM operation at 60 kHz with frequency jittering for lower EMI
- transconductance error amplifier with 1.2 V ± 2% reference voltage
- self-supply option to avoid auxiliary winding and bias components

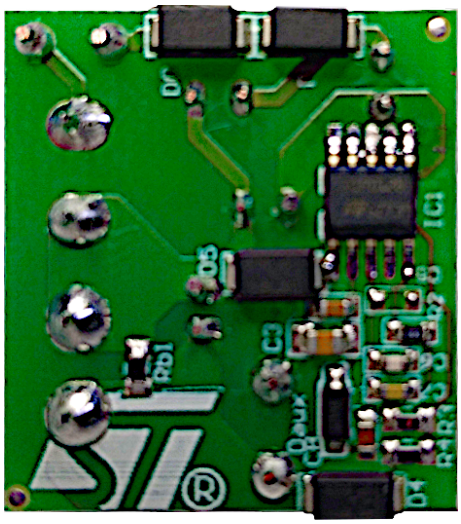
Thanks to the VIPER013BLSTR advanced light load management and ultra-low consumption, the STEVAL-VP013B1B input power consumption can be reduced under no load condition to less than 20 mW at 230 V_{AC}, meeting the most stringent energy saving regulations for active mode and light load efficiency.

The IC protection includes:

- pulse skip mode to avoid flux-runaway during start-up
- delayed overload shutdown for safe fault condition management
- max. duty cycle counter
- thermal shutdown
- input overvoltage

All protections are in auto-restart mode.

Figure 1. STEVAL-VP013B1B evaluation board



1 Features and specifications

Table 1. STEVAL-VP013B1B electrical specifications

Parameter	Min.	Typ.	Max.
Operative AC main input voltage	60 V_{AC}		300 V_{AC}
Mains frequency	47 Hz		65 Hz
Output voltage – V_{OUT}	4.75 V	5 V	5.25 V
Output current – I_{OUT} at Vin ≥ 80 V_{AC}	1 mA(1)		100 mA
Output current – I_{OUT} at Vin ≥ 60 V_{AC}	1 mA (1)		75 mA
Maximum peak power			0.75 W
Maximum rms power			0.5 W
Precision of output regulation - Δ_{VOUT_LF}		±5%	
High frequency output voltage ripple - Δ_{VOUT_HF}		50 mV	
Switching frequency - F_{OSC}		60 kHz	
Efficiency at full load		62%	
Ambient operating temperature	-40 °C		85 °C

1. *Ensured by bleeder resistor Rbl1.*

The switch mode power supply (SMPS) is set in buck topology.

It draws energy from the main AC line through the input section formed by R1 resistor for inrush current limiting, the two diodes in series (D0 and D1) to strengthen the application against surge occurrence and the LC filter formed by L2 and C9 for rectification and EMC suppression.

The converter output voltage is compared (through the R3 and R4 voltage dividers) to the internal 1.2 V voltage reference via the FB pin, that is the inverting input of the transconductance error amplifier, to define the output voltage set-point according to the following equation:

$$V_{out} = V_{FB\_REF} \cdot \left(1 + \frac{R_4}{R_3}\right) \quad (1)$$

It is possible to set 5 V output voltage and keep the C3 voltage above the V_{CSon} threshold according to $V_{CSonMAX}$ 4.5 V threshold value.

The IC V_{DD} in steady state condition is biased from the output through the D_{AUX} diode and C3 capacitor, while C4 capacitor is useful to get a clean bias voltage for the internal sub-block and protection during EFT/ESD occurrence.

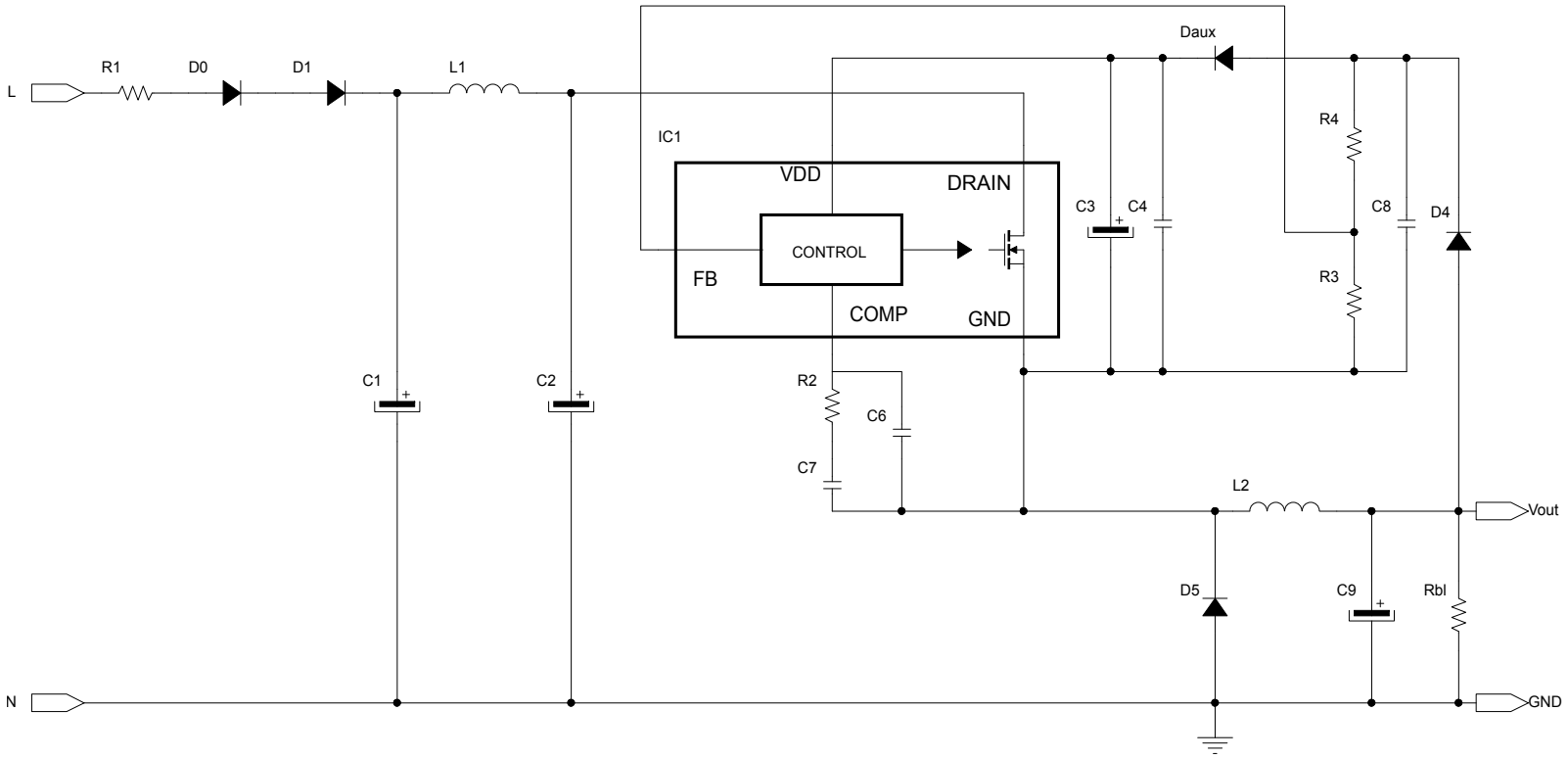
The compensation network, made by R2, C6 and C7, is connected between the COMP pin (output of the error amplifier) and the GND pin (see Section Appendix A Feedback loop calculation guidelines for more details on the compensation).

The Rbl bleeder resistor provides an 1 mA approximate minimum load to avoid overvoltage when the output load is disconnected.

Very low power input consumption at no load (less than 20 mW at 230 V_{AC}) is obtained thanks to the VIPER013BLSTR internal blocks.

1.1 Schematic diagrams

Figure 2. **STEVAL-VP013B1B schematic**



1.2 Bill of materials

Table 2. **STEVAL-VP013B1B bill of materials**

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
1	1	Daux	0.15 A / 100 V	signal Schottky diode, SOD-123	ST	BAT41ZFILM
2	2	D4, D5	1 A / 600 V	ultrafast diode, SMA	ST	STTH1L06A
3	1	IC1		High voltage converter, SO-16N	ST	VIPer013BLS
4	1	D0	1 A / 1000 V	power rectifier diode, SMA	ON SEMICONDUCTOR	MRA4007T3G
5	1	D1	1 A / 1000 V	power rectifier diode, SMA	ON SEMICONDUCTOR	MRA4007T3G
6	1	L1	470 µH, 400 mA	axial inductor	WE	7447462471
7	1	L2	680 µH, 420 mA	axial inductor	WE	744732681
8	2	C1, C2	1 µF, 450 V, ±20%	electrolitic capacitor, Ø6.3mm – p2.5mm - h11mm	RUBYCON	450PK1MEFC
9	1	C3	2.2 µF, 50 V	ceramic multilayer cap, 0805	MURATA	GRM21BR61H225KA73L
10	1	C4	100 nF, 50 V	ceramic multilayer cap, 0603	MURATA	GRM188R71H104KA93D
11	1	C5	not mounted	not mounted		-
12	1	C6	120 pF, 50 V	ceramic multilayer cap, 0603	MURATA	GRM1882C1H121JA01D
13	1	C7	22 nF, 50 V	ceramic multilayer cap, 0603	Vishay	VJ0603Y223KXAAT
14	1	C8	1 µF, 50 V	ceramic multilayer cap, 0603	MURATA	GRM188R61H105KAALD
15	1	C9	100 µF, 16 V, ±20%	ultra-low ESR Electrolitic cap, Ø5mm – p.2mm – h12.5mm	RUBYCON	16ZLH100MEFC5X11
16	1	R1	22 Ω, 1 W, ±1%	Metal Oxide Film Resistor, Ø3m - p9mm	TE Connectivity	ROX1SJ22R
17	1	R2	220 kΩ, ±1%	SMD thick film resistor, 0603	Vishay	CRCW0603220KFKEA
18	1	R3	22 kΩ, 0.25 W, ±1%	SMD thick film resistor, 0603	Panasonic	ERJU03F2202V
19	1	R4	78.7 kΩ, 0.1 W, ±1%	SMD thick film resistor, 0603	Panasonic	ERA3AEB7872V
20	1	Rbl	5.6 kΩ, 0.25 W, ±1%	SMD resistor, 0603	Panasonic	ERJPA3F5601V
21	2	IN, OUT		2-way output connector	TE Connectivity	282837-2

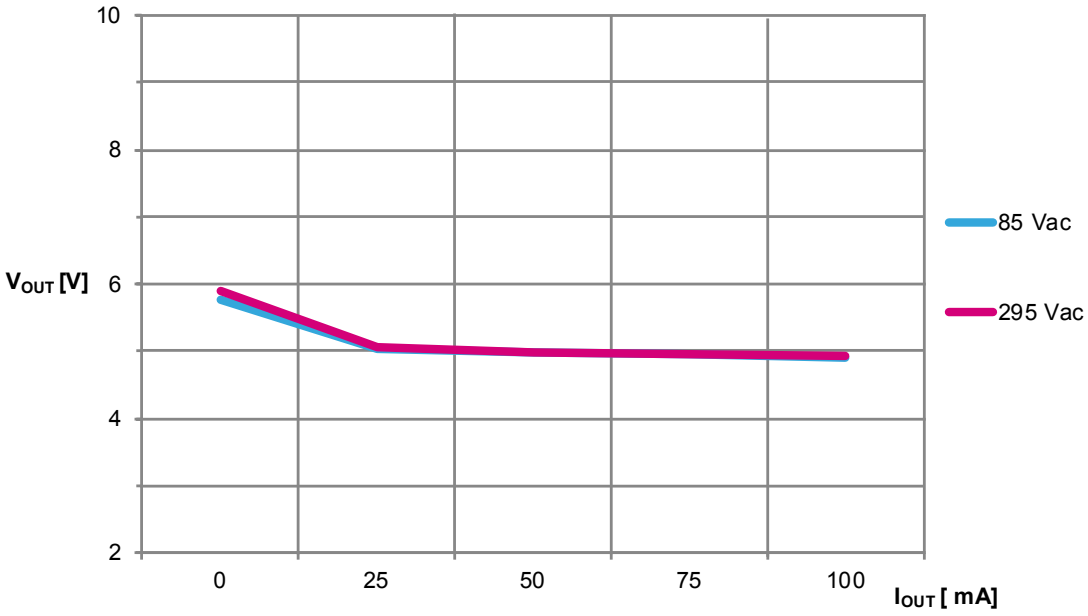
1.3 Output voltage characteristics

The STEVAL-VP013B1B output voltage is measured in different line and load conditions. The table below shows the results: the output voltage variation is within an acceptable range with load and line variation.

Table 3. Output voltage regulation with no load and at nominal V_{IN}

V_{IN} [V_{AC}]	V_{OUT} (V) at no load
115	5.77
230	5.91

Figure 3. Output voltage load regulation at minimum and maximum DC input voltage



2 Typical waveforms

Drain voltage and current waveforms in full load condition are shown for minimum and maximum AC input voltage in Figure 4 and for the two nominal input voltages in Figure 5 and Figure 6.

Figure 4. Drain current and voltage at full load at 60 V_{AC}

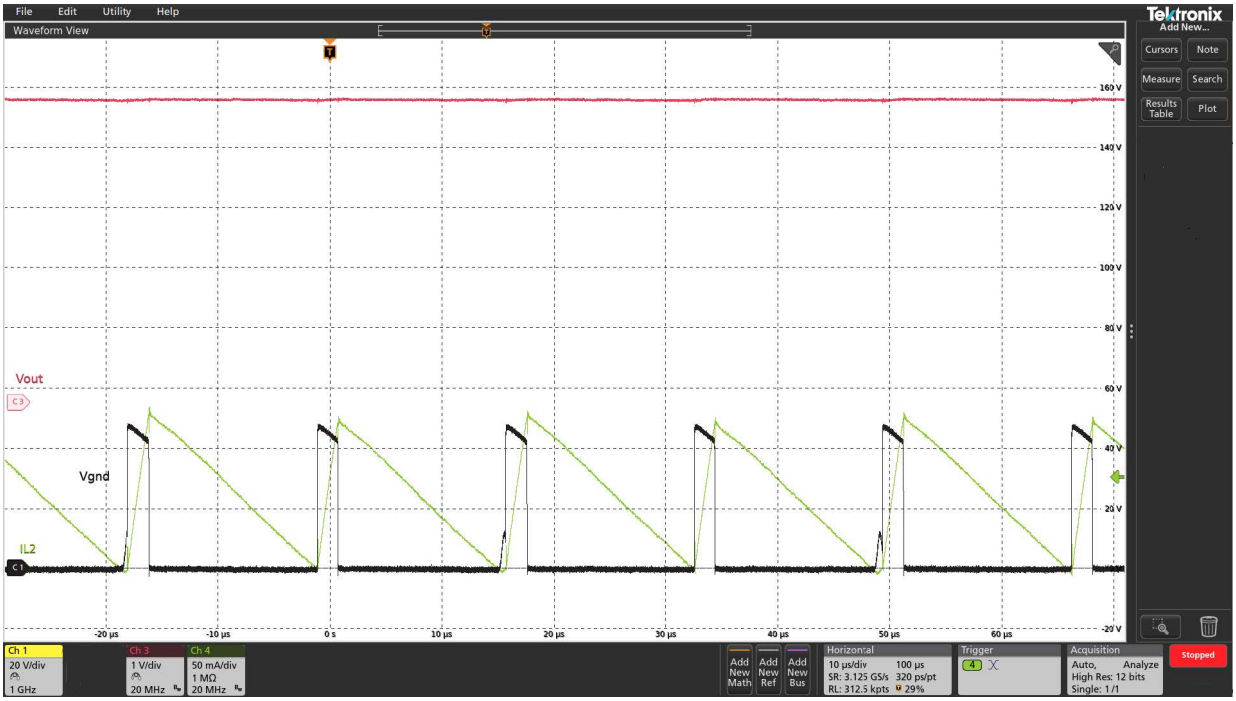


Figure 5. Drain current and voltage at full load at 115 V_{AC}

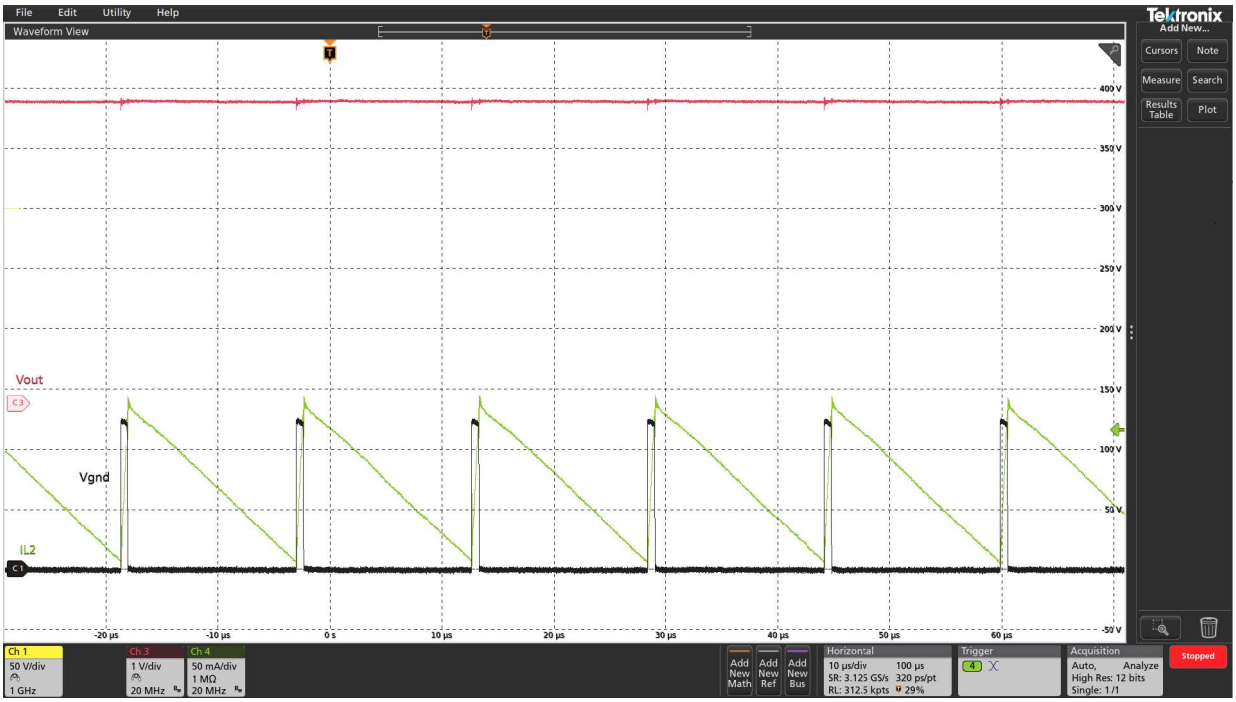


Figure 6. **Drain current and voltage at full load at 230 V_{AC}**

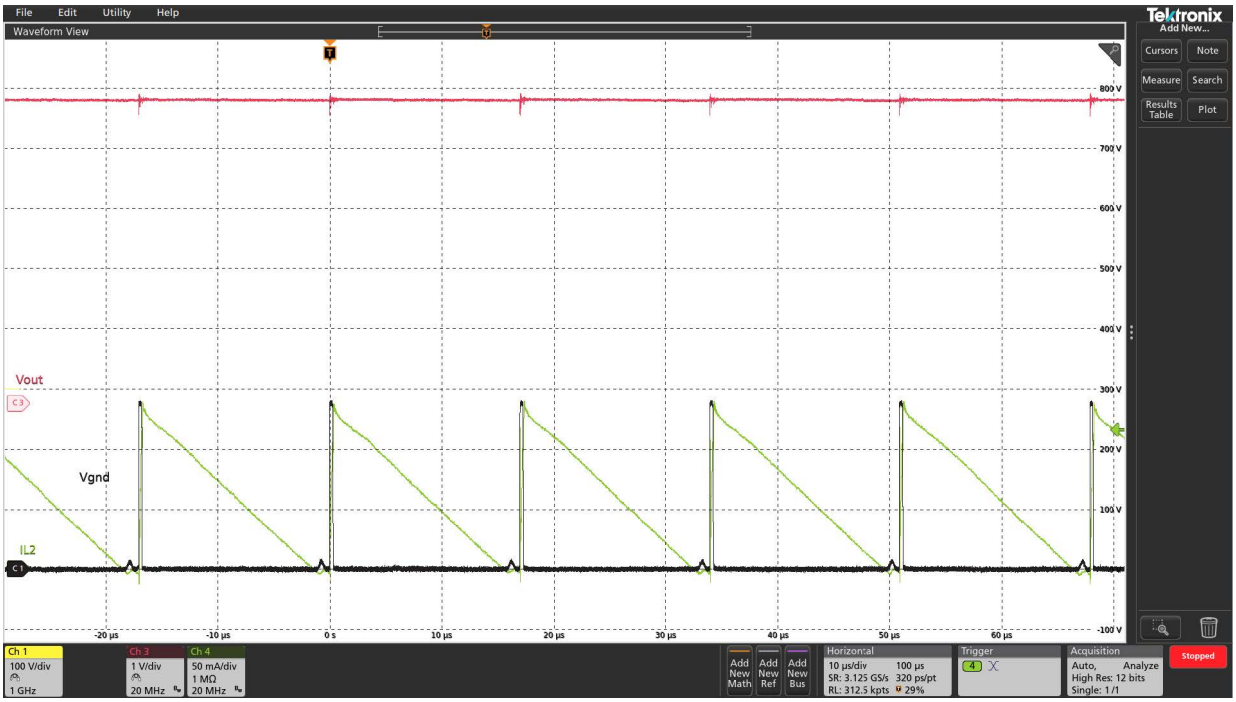
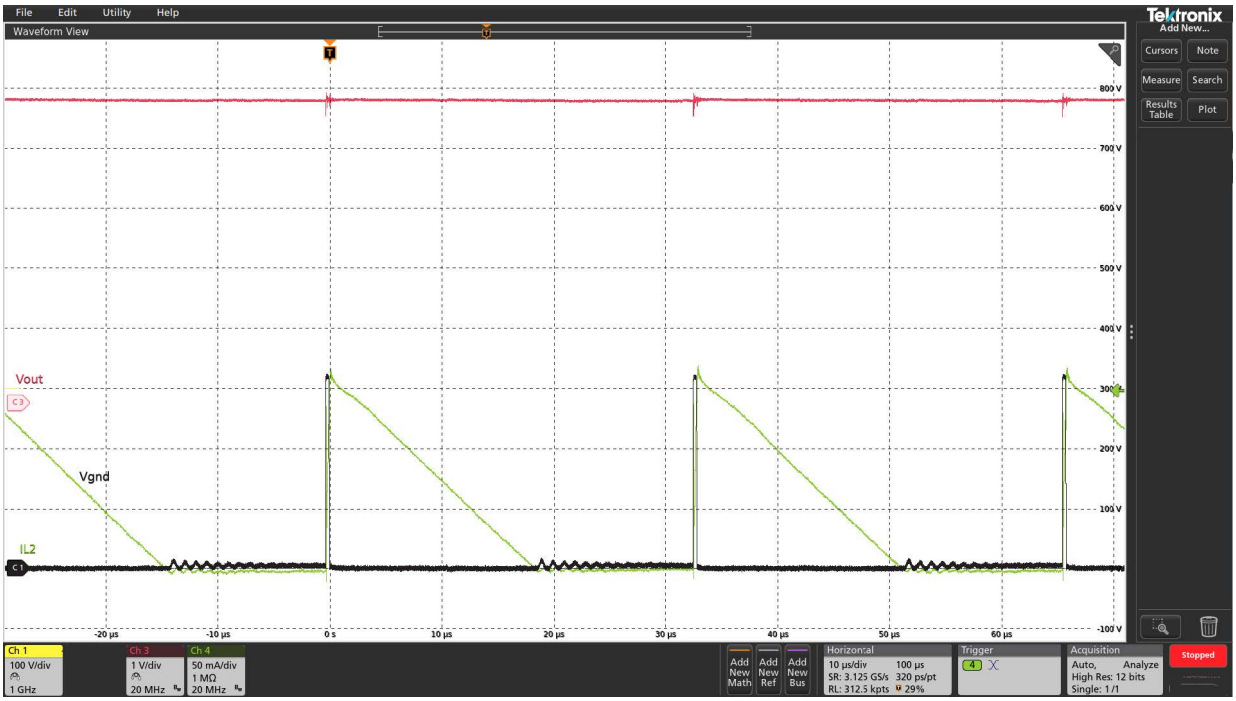


Figure 7. **Drain current and voltage at full load at 265 V_{AC}**



The output voltage ripple, at the switching frequency, was also measured at full load and no load conditions, at 115 $V_{AC}$and at 230 V_{AC}.

Figure 8. **Output voltage ripple at full load at 115 V_{AC}**

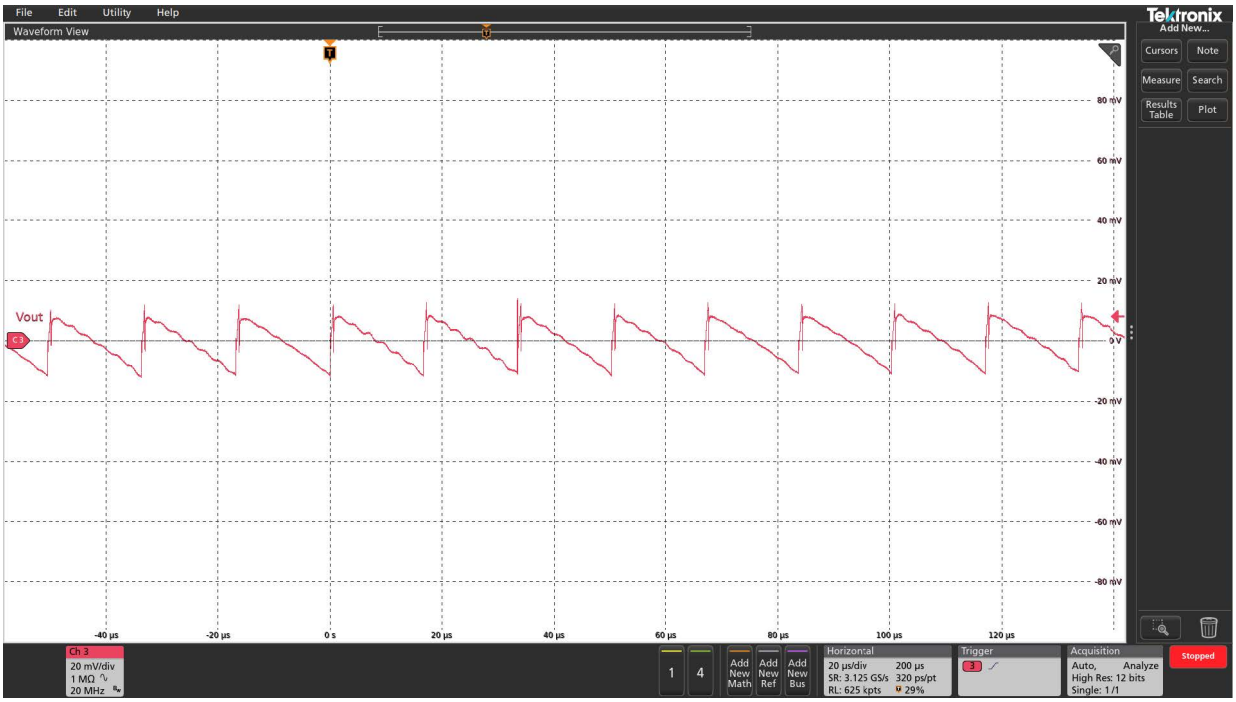


Figure 9. **Output voltage ripple at full load at 230 V_{AC}**

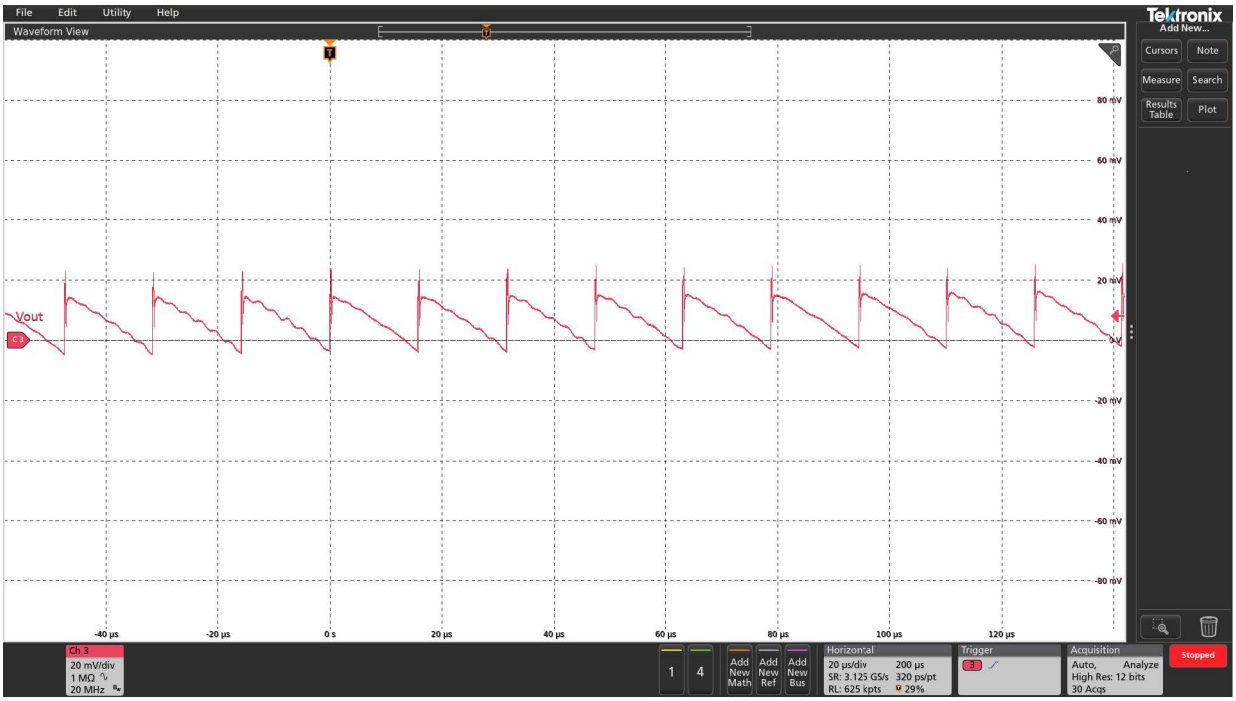


Figure 10. **Output voltage ripple at no load at 115 V_{AC}**

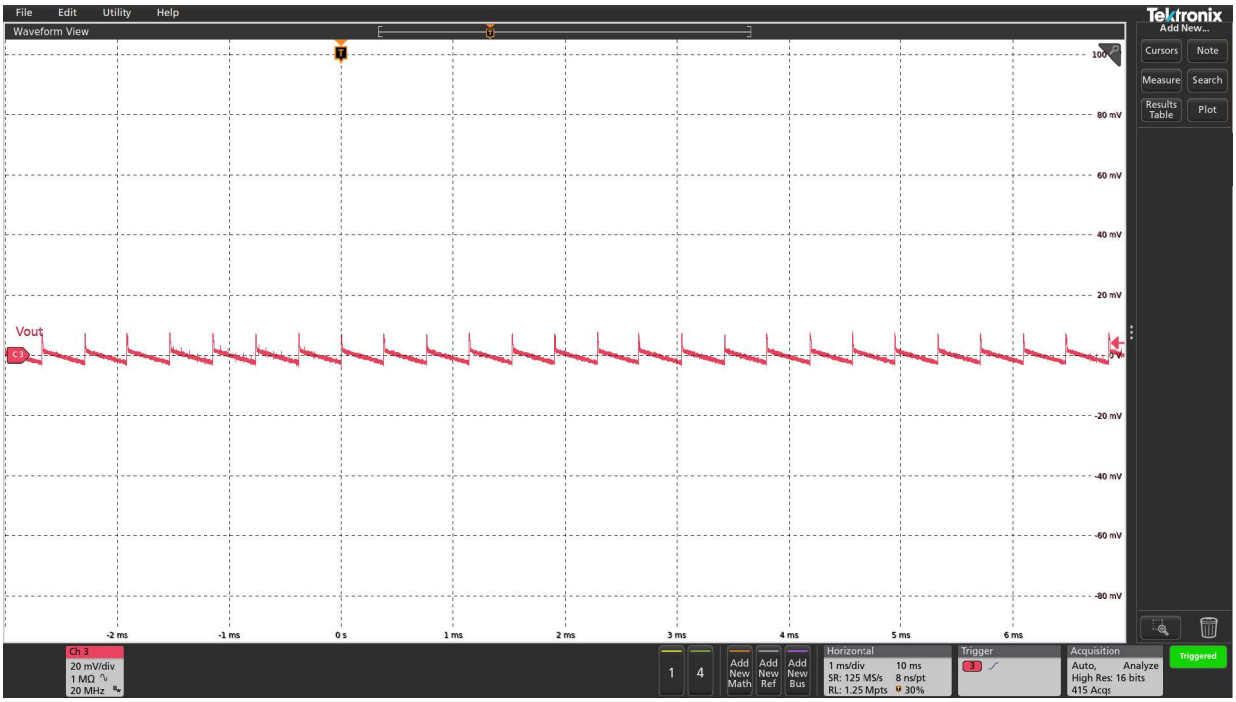
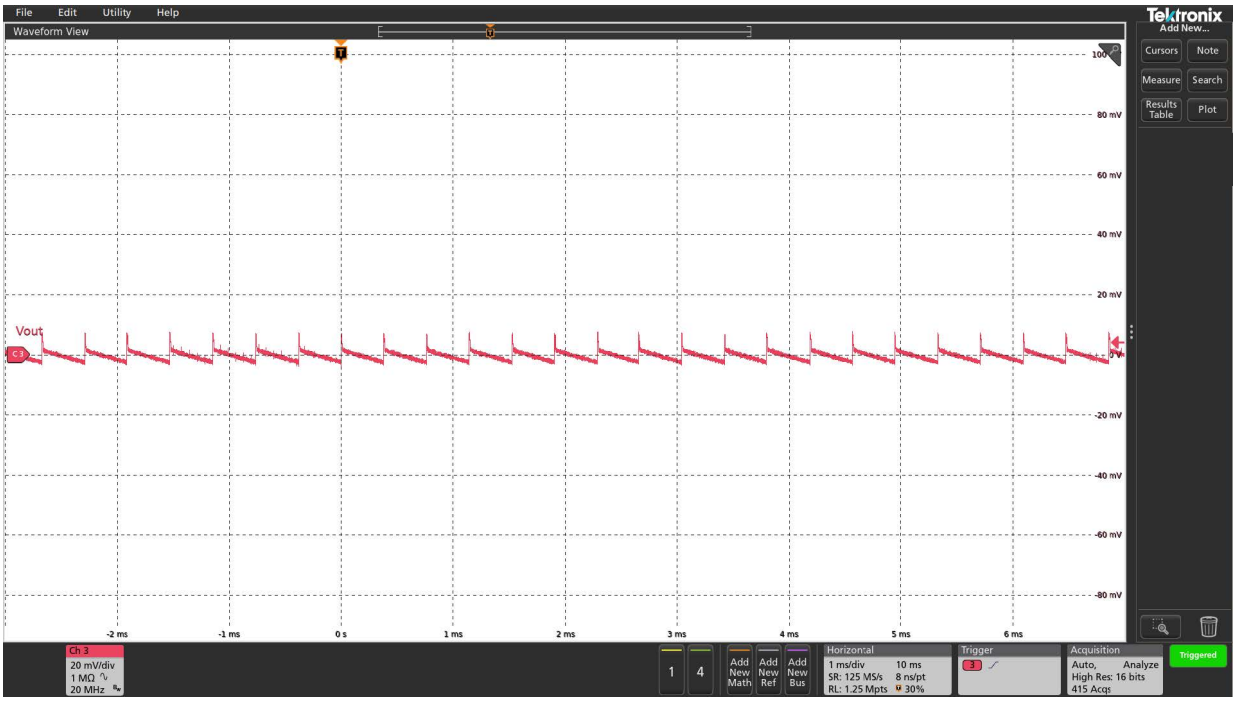


Figure 11. **Output voltage ripple at no load at 230 V_{AC}**



2.1 Dynamic step load regulation

In any power supply, it is important to measure the output voltage when the converter is subjected to dynamic load variations in order to ensure appropriate stability free of overvoltage and undervoltage events.

The test is performed by varying the output load from 0 to 0.1 A (100% of nominal value) for both nominal input voltages.

In the tested conditions, no abnormal oscillations were observed on the output, and over- and under-shoot were well within acceptable values.

Figure 12. Dynamic step load (I_{OUT} from 0 to 0.1 A) at 115 V_{AC}

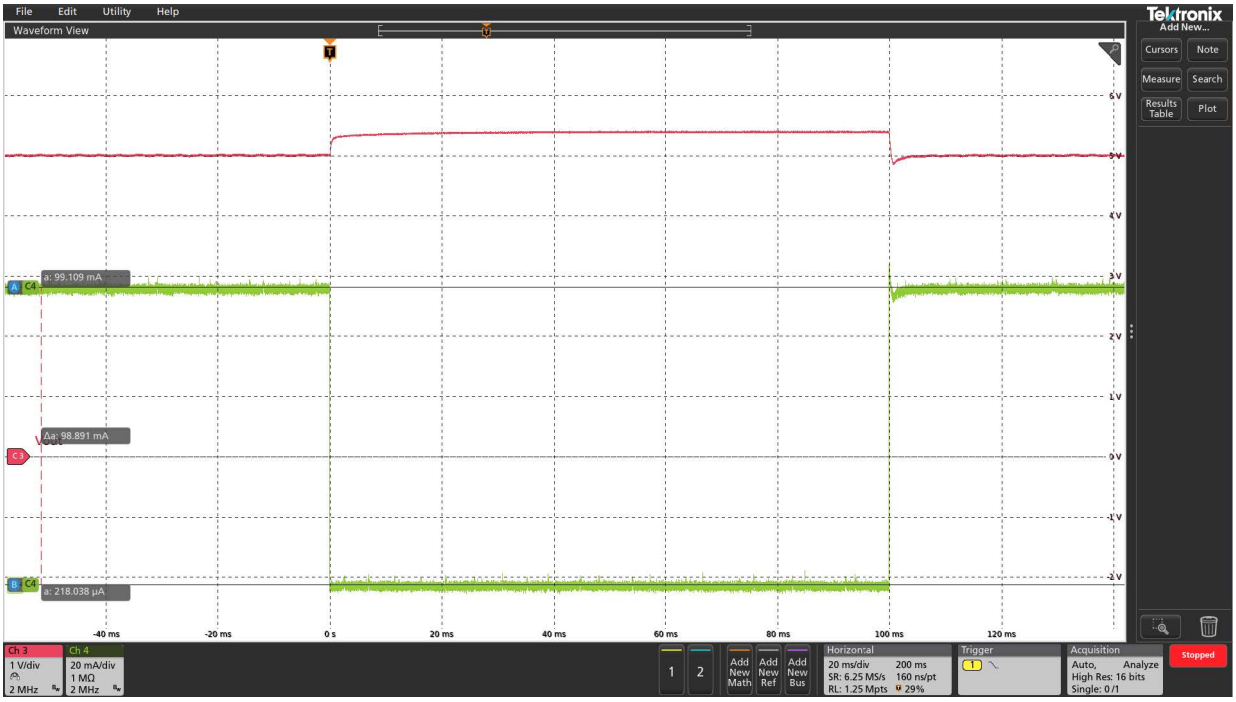
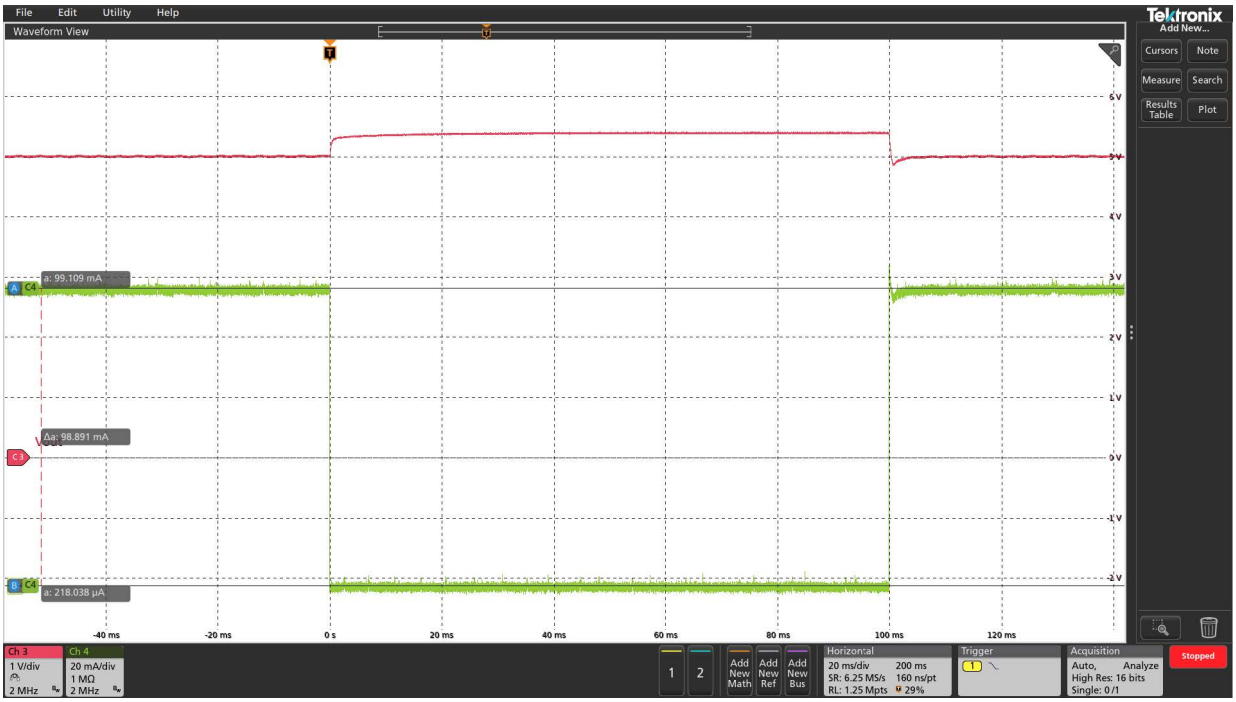


Figure 13. Dynamic step load (I_{OUT} from 0 to 0.1 A) at 230 V_{AC}



3 Startup

When the converter starts, the output capacitor is discharged and needs time to reach the steady state condition. During this time, the power demand from the control loop is at its maximum, leading to a deep continuous operating mode of the converter.

Another consideration is that when the MOSFET is switched on, it cannot be switched off before the minimum on time (T_{ON_MIN}) has elapsed. Because of the deep continuous working mode of the converter, an excessive drain current during T_{ON_MIN} can stress the component of the converter, the device itself, and the output inductor. Output inductor saturation may also occur under these conditions.

To avoid these negative effects, the VIPER013BLSTR implements an internal soft-start feature. As the device starts to work, the drain current is allowed to increase from zero to the maximum value gradually, regardless of the control loop request.

The internal soft-start function progressively increases the cycle-by-cycle current limitation set point from zero to I_{DLIM} in 8 steps. The soft-start time t_{SS} is internally set at 8 ms and is activated at any attempt of converter startup and at any restart after a fault event. The feature protects the system at the startup when the output load occurs like short-circuit and the converter works at its maximum drain current limitation.

The following figures show the soft-start phase of the present converter at maximum load, for nominal input voltages (115 $V_{AC}$and 230 V_{AC}).

Figure 14. Startup at 115 V_{AC}, full load

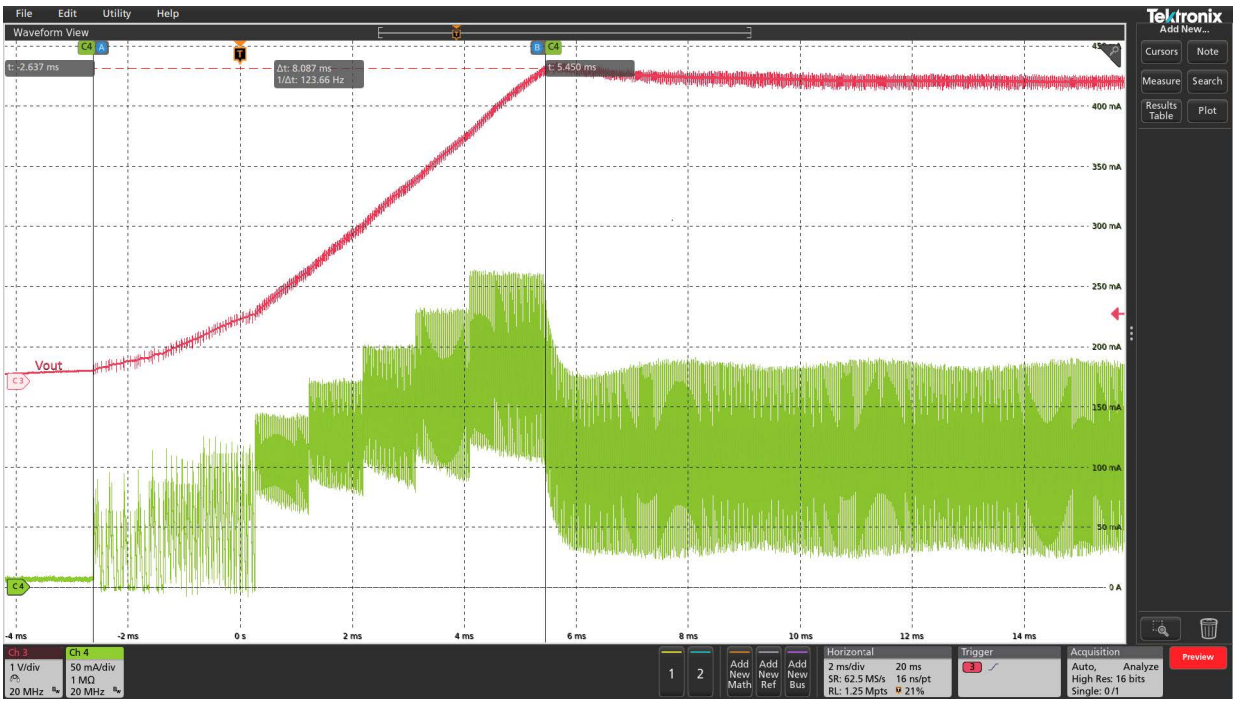


Figure 15. **Startup at 230 V_{AC}, full load - zoom**

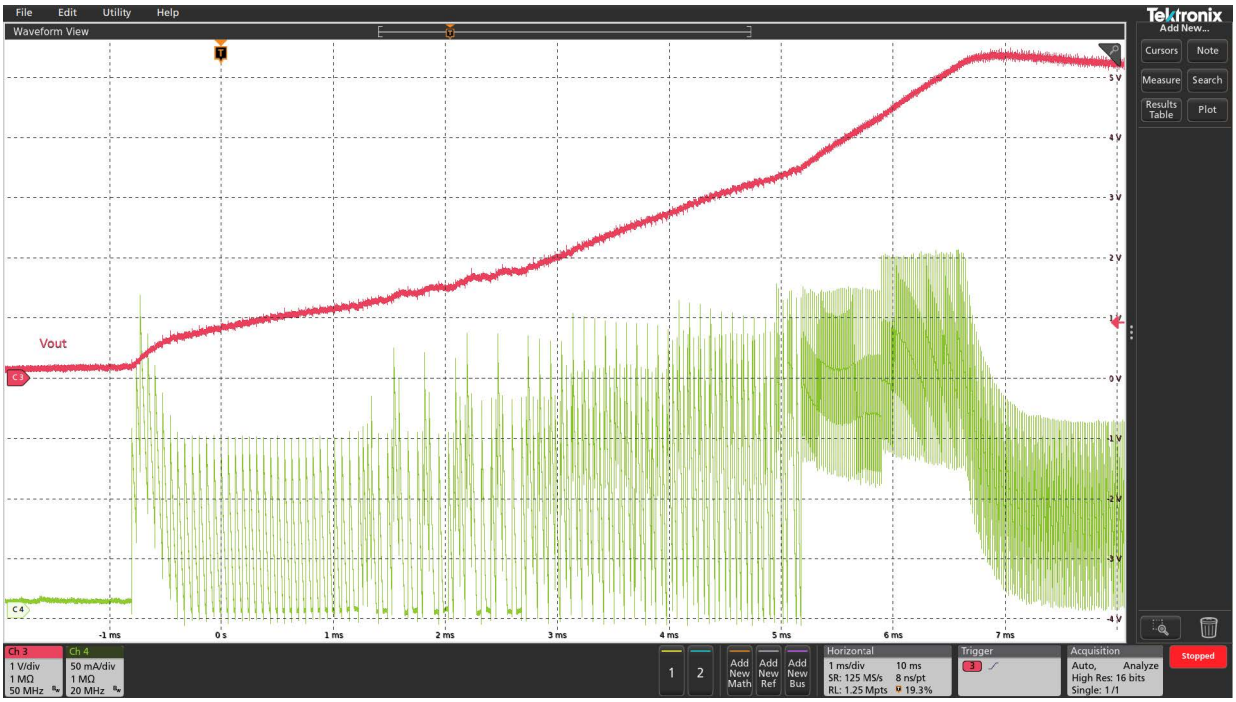


Figure 16. **Startup at 265 V_{AC}, full load**

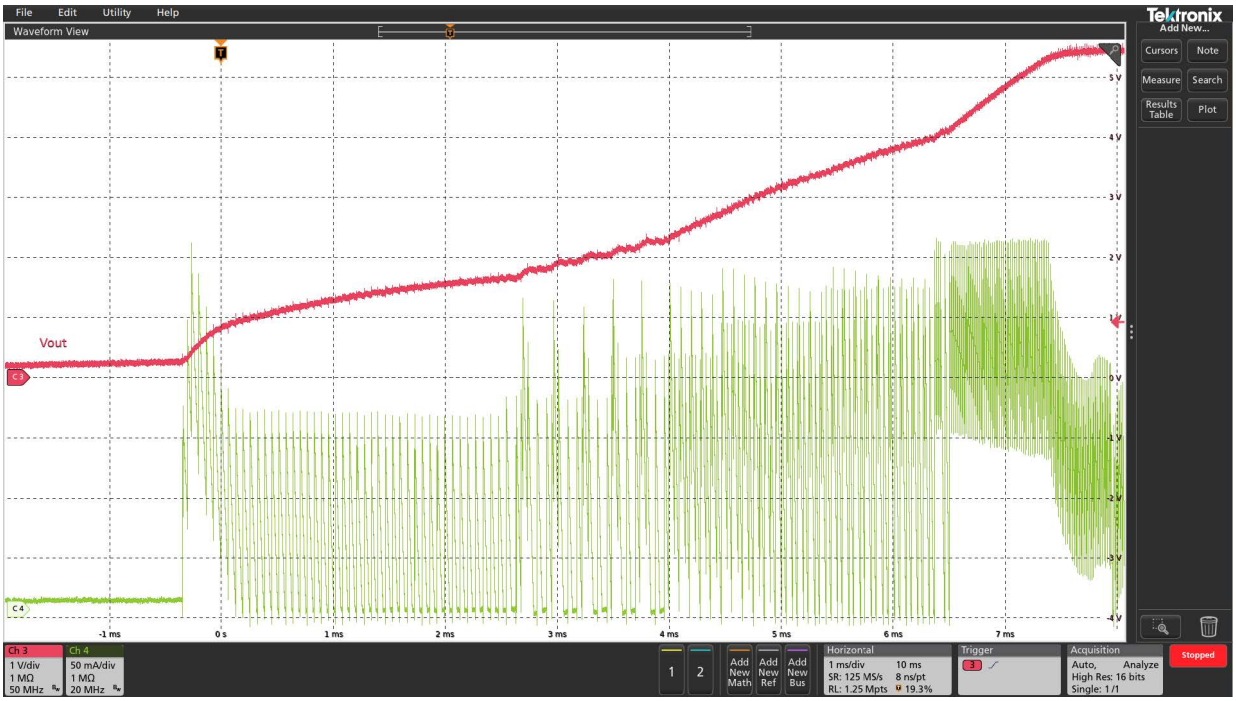
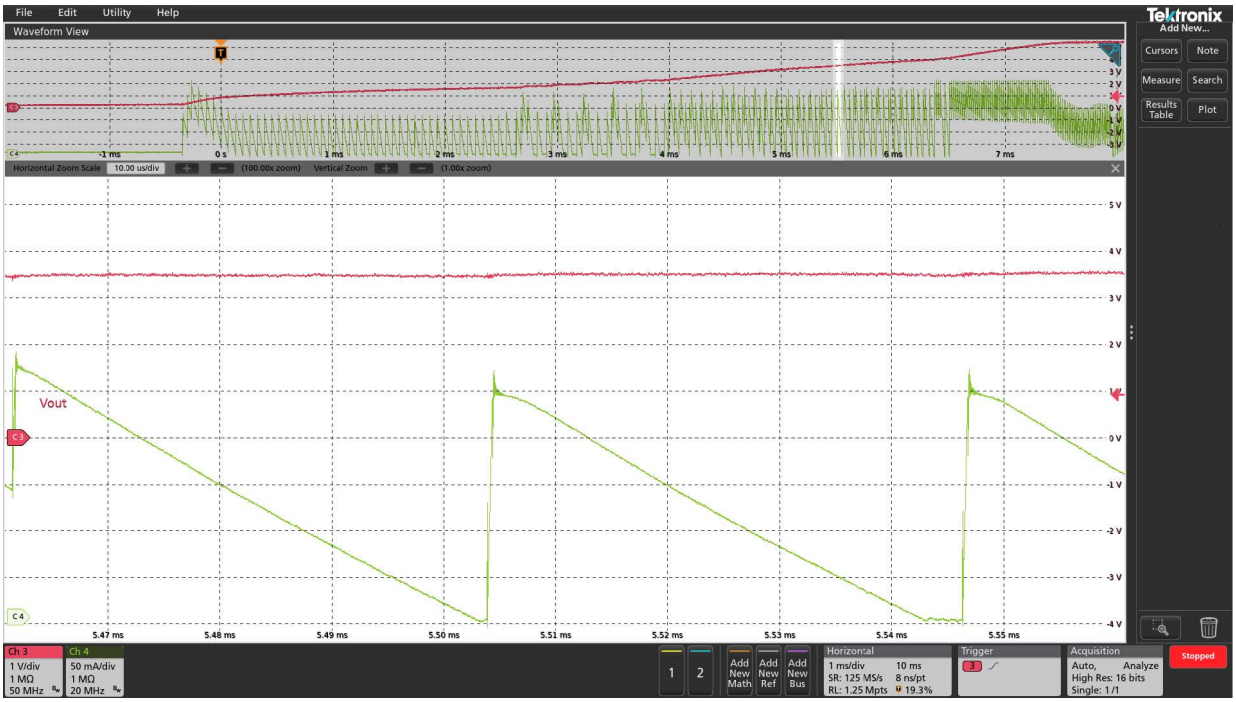


Figure 17. **Startup at 265 V_{AC}, full load - zoom**



4 Protection features

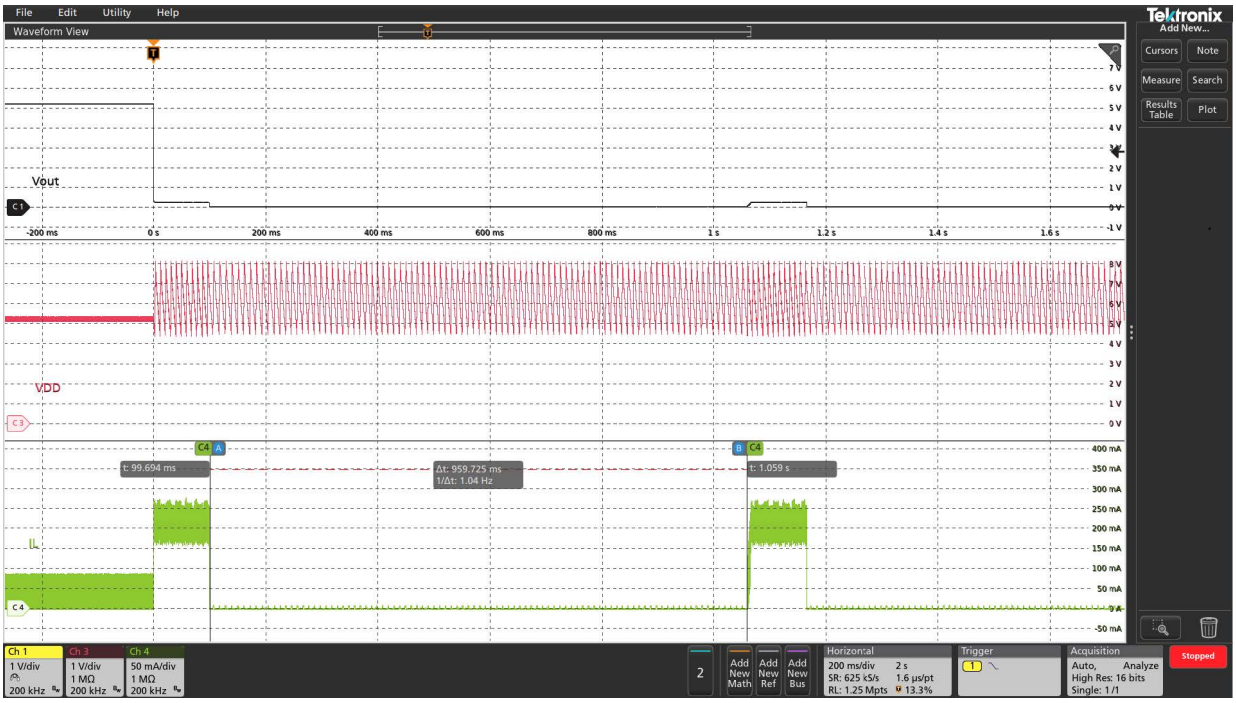
4.1 Overload and short circuit protection

When the load power demand increases, the feedback loop reacts by increasing the voltage on the COMP pin. In this way, the PWM current set point increases and the power delivered to the output rises. This process ends when the delivered power equals the load power request.

In case of overload or output short circuit, the drain current value reaches the I_{DLIM}. For every cycle that this condition is met, an internal OCP counter is incremented and the protection is tripped if the overload condition persists for time t_{OVL} (50 ms typical). The power section is turned off and the converter is disabled for time $t_{RESTART}$ (1s typical). After this time has elapsed, the IC resumes switching and the protection continues to be triggered indefinitely if the fault condition remains. This ensures a low converter restart attempt rate, providing safe operation with extremely low power throughput and avoiding IC overheating in case of repeated overload events.

Figure 18. Overload event, OLP tripping

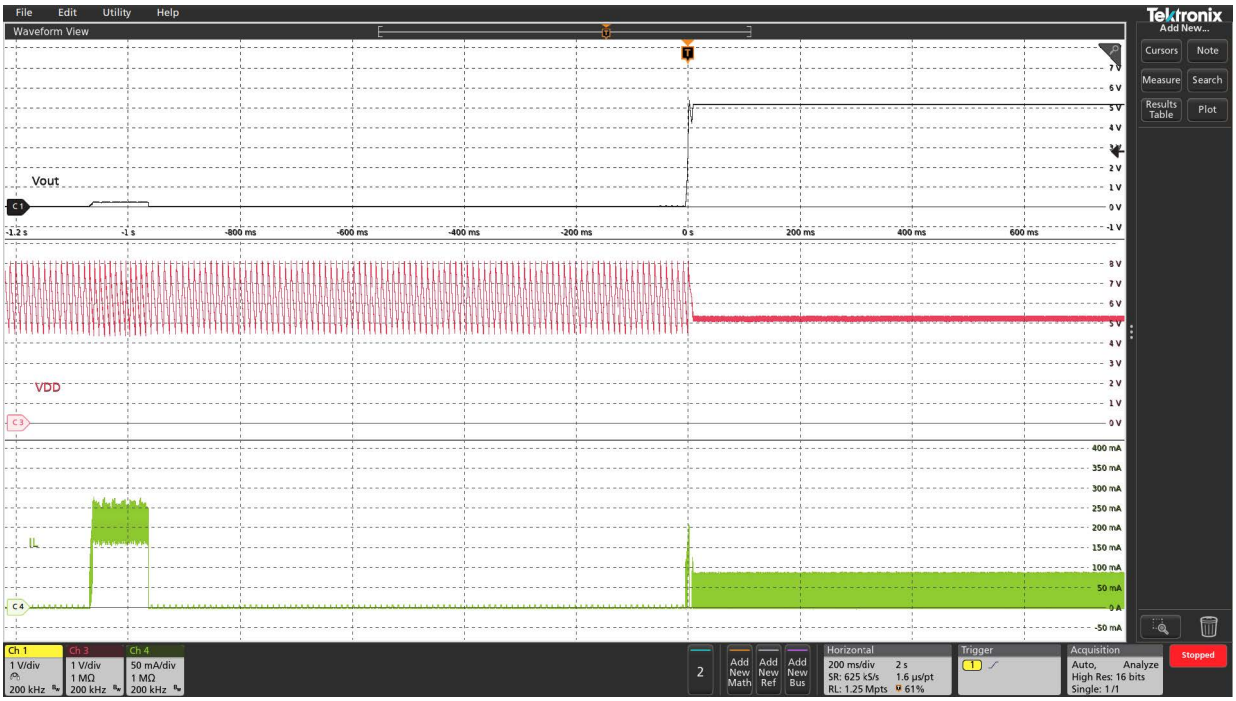
Figure 19. **Overload event, continuous overload**



Furthermore, the internal soft start function is invoked at startup after protection tripping.

After the fault is removed, the IC resumes working normally. If the fault is removed before the protection is triggered during t_{SS} or t_{OVL}, the counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped. If the short circuit is removed during $t_{RESTART}$, the IC waits until $t_{RESTART}$ has elapsed before resuming switching.

Figure 20. **Overload event, fault removed and autorestart**

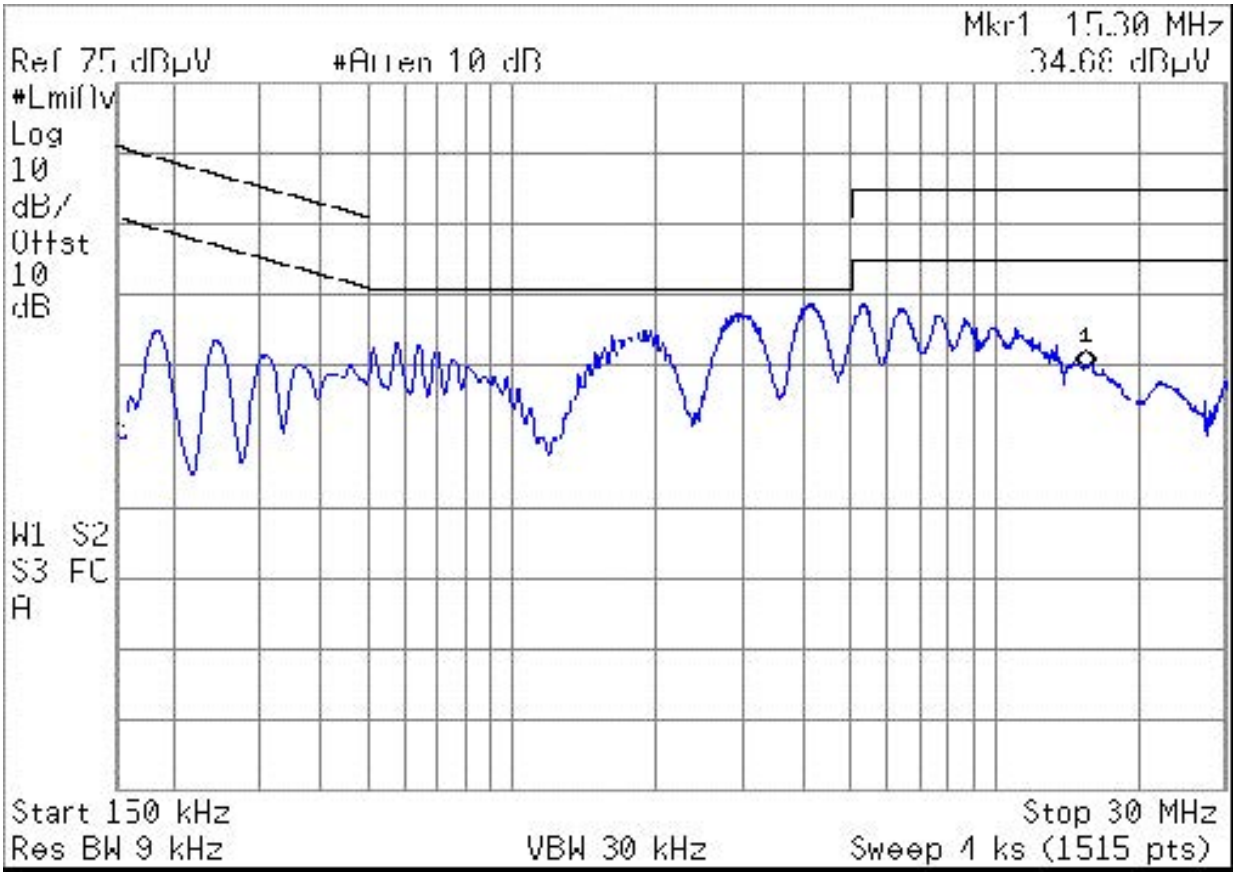


5 Conducted noise measurements

The VIPER013BLSTR frequency jittering feature allows the spectrum to be spread over frequency bands rather than being concentrated on single frequency value. Especially when measuring conducted emission with the average detection method, the level reduction can be several dBµV.

A pre-compliance test for the EN55022 (Class B) European normative was performed and average measurements of the conducted noise emissions at full load and nominal mains voltages are shown in the following figure.

Figure 21. CE average measurement at 230 V_{AC} full load



Appendix A Feedback loop calculation guidelines

A.1 DCM buck converter transfer function

The control-to-output transfer function of the buck converter in DCM, $G_{VC}(s)$, is given by:

$$G_{VC}(s) = H_0 \cdot \frac{1 + \frac{s}{\omega_{Z1}}}{\left(1 + \frac{s}{\omega_{P1}}\right) \cdot \left(1 + \frac{s}{\omega_{P2}}\right)} \quad (2)$$

Gain, poles and zero are defined below:

$$H_0 = \frac{2 \cdot R_0}{H_{COMP}} \cdot \frac{\sqrt{K_0 \cdot (1 - M)}}{2 - 3 \cdot M} \quad (3)$$

$$\omega_{Z1} = \frac{1}{R_C \cdot C_0} \quad (4)$$

$$\omega_{P1} = \frac{1}{R_0 \cdot C_0} \cdot \frac{2 - 3 \cdot M}{1 - M} \quad (5)$$

$$\omega_{P2} = \frac{2}{T_S} \cdot \left(\frac{M}{D}\right)^2 \quad (6)$$

In most of practical cases the pole ω_{P2} is placed at high frequency and can be neglected. As a result, most of times, the DCM buck converter can be treated as a dominant-pole system, hence very easy to compensate.

In the above equations, some characteristic parameters are defined as follows:

$$M = \frac{V_0}{V_{IN}} \quad (7)$$

$$K_0 = \frac{2 \cdot L}{R_0 \cdot T_S} \quad (8)$$

A.2 Compensation design

To compensate the DCM buck, we use a type-2 compensator with the integrator effect to provide the high DC gain to minimize static error, and a pole-zero pair to boost the phase according the phase margin target.

The compensator is determined using a manual pole-zero placement technique where the zero is placed in the vicinity of the power stage dominant pole to cancel its effect, and the pole position is adjusted to achieve the required phase margin.

Follow the procedure below to design the compensation with a type 2 compensator:

Step 1. Select the crossover frequency f_C and the phase margin Φ_m .

Step 2. Evaluate the gain and phase of the plant at crossover frequency.

$$G_{VC(f_C)} = |G_{VC} \cdot (2 \cdot \pi \cdot f_C)| \quad (9)$$

$$\Phi_{VC(f_C)} = \arg[G_{VC} \cdot (2 \cdot \pi \cdot f_C)] \quad (10)$$

Step 3. The compensated open-loop gain must attain the unit gain at f_C with the required phase margin, so the compensator must be designed in order to have following gain and phase (at f_C):

$$G_{C(f_C)} = |G_C \cdot (2 \cdot \pi \cdot f_C)| = \frac{1}{G_{VC(f_C)}} \quad (11)$$

$$\Phi_{C(f_C)} = \arg[G_C \cdot (2 \cdot \pi \cdot f_C)] = 90 - 180 + \Phi_m - \Phi_{VC(f_C)} \quad (12)$$

Step 4. Cancel the pole of the plant, $f_{P(p)}$, by placing the zero of the compensator $f_{Z(C)}$ in the region $\alpha = 1$ to 5

$$f_{Z(C)} = \frac{\omega_{Z(C)}}{2 \cdot \pi} = \alpha \cdot f_{P(p)} \quad (13)$$

Step 5. Place the pole of the compensator to boost the phase and to obtain the desired phase margin

$$f_{P(C)} = \frac{f_C}{\tan\left[\tan^{-1}\left(\frac{f_C}{f_{Z(C)}}\right) - \Phi_{C(f_C)}\right]} \quad (14)$$

Step 6. Calculate the gain G_{C0}

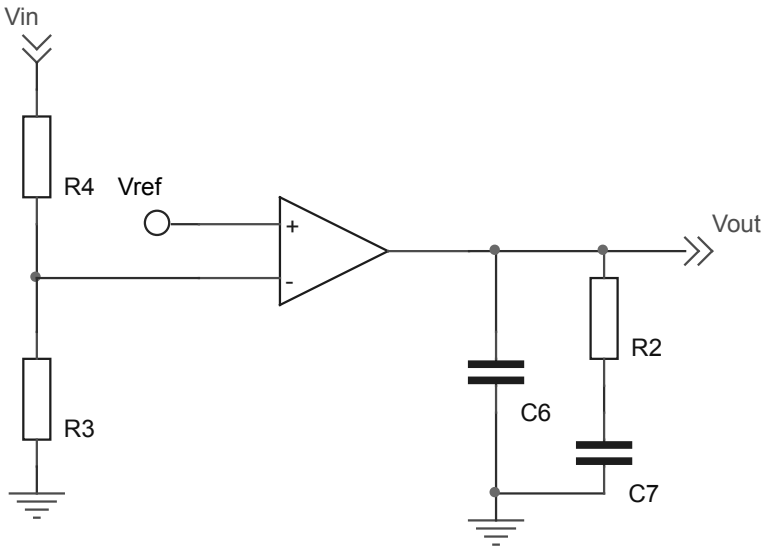
$$G_{C0} = G_{C(f_C)} \frac{\omega_C \cdot \sqrt{1 + \left(\frac{f_C}{f_{P(C)}}\right)^2}}{\sqrt{1 + \left(\frac{f_C}{f_{Z(C)}}\right)^2}} \quad (15)$$

The design of $G_C(s)$ is complete.

A.3 Summary of the compensator

The following figure shows the schematic of the Type 2 amplifier used in the VIPER013BLSTR.

Figure 22. Type 2 compensator with OTA



The transfer function of this compensator can be expressed as the following:

$$G_C(s) = \frac{R_3 \cdot g_m}{(R_3 + R_4) \cdot (C_6 + C_7)} \cdot \frac{1 + s \cdot R_2 \cdot C_7}{s \cdot \left[1 + s \cdot R_2 \cdot \left(\frac{C_7 \cdot C_6}{C_7 + C_6}\right)\right]} \quad (16)$$

The first component to be chosen is resistor R_4, which must be high enough to render the current offset entering in the inverting pin negligible, but low enough to ensure that other compensation components do not have to be too large. Resistor R_3 is fixed to set the DC operating point of the loop. Of course, both R_4 and R_3 play a role in determining the gain of the compensator.

Step 1. Set the values for R_4 and R_3.

$$R_4 = 78.7\,k\Omega \quad (17)$$

$$R_3 = 22\,k\Omega \quad (18)$$

Step 2. Calculate the value for C_6

$$C_6 = \frac{f_{Z1}}{f_{P1}} \cdot \frac{R_3 \cdot g_m}{G_{C0} \cdot (R_4 + R_3)} \approx 137pF \quad (19)$$

The selected value for C_6 is:

$$C_6 = 120pF \quad (20)$$

Step 3. Calculate C_7

$$C_7 = \frac{R_3 \cdot g_m}{G_{C0} \cdot (R_4 + R_3)} - C_6 \approx 23.4\,\text{nF} \quad (21)$$

The selected value for C_7 is:

$$C_7 = 22\,\text{nF} \quad (22)$$

Step 4. Calculate R_2

$$R_2 = \frac{1}{2 \cdot \pi \cdot f_{Z1} \cdot C_7} \approx 207\,\text{k}\Omega \quad (23)$$

The selected value for R_2 is:

$$R_2 = 220\,\text{k}\Omega \quad (24)$$

The resulting crossover frequency f_C and the phase margin Φ_m are:

$$f_C \approx 2.1\,\text{kHz} \quad (25)$$

$$\Phi_m \approx 72° \quad (26)$$

Appendix B Layout guidelines and design recommendations

An appropriate PCB layout is essential for the correct operation of any switch-mode converter. It ensures the delivery of clean signals to the IC and higher immunity to external and switching noise, as well as reducing radiated and conducted electromagnetic interference, all of which help a given solution satisfy EMC requirements.

Below are some general concepts to keep in mind when designing SMPS circuit layouts.

Separate signal and power tracks:

- Traces carrying signal currents should generally be run at a distance from other tracks carrying pulsed currents or with rapidly changing voltages.
- Signal ground traces should be connected to the IC signal ground, GND, using a single "star point", placed close to the IC.
- Power ground traces should be connected to the IC power ground, GND.
- The compensation network should be connected to the COMP, maintaining the trace to GND as short as possible.
- In two-layer PCBs, it is a good practice to route signal traces on one PCB side and power traces on the other side.

Filter sensitive pins and crucial points on the circuit:

- A small high-frequency bypass capacitor to GND might be useful to get a clean bias voltage for the signal part of the IC and protect the IC itself during EFT/ESD tests.
- A low ESL ceramic capacitor (a few hundred pF up to 0.1 µF) should be connected across VCC and GND, placed as close as possible to the IC.
- With flyback topologies, when the auxiliary winding is used, it is suggested to connect the VCC capacitor on the auxiliary return and then to the main GND using a single track.

Keep power loops as confined as possible:

- Minimize the area circumscribed by current loops where highly pulsed currents flow in order to reduce its parasitic self-inductance and the radiated electromagnetic field; this will greatly reduce the electromagnetic interferences produced by the power supply during the switching.
- In a flyback converter the most critical loops are:
  - The one with the input bulk capacitor, the power switch and the power transformer
  - the one with the snubber.
  - the one with the secondary winding, the output rectifier and the output capacitor.
- In a buck converter the most critical loop is:
  - The one with the input bulk capacitor, the power switch, the power inductor, the output capacitor and the free-wheeling diode.

Reduce line lengths as any wire will act as an antenna:

- With the very short rise times exhibited by EFT pulses, any antenna has the capability of receiving high voltage spikes. Shorter lines reduce the level of radiated energy received and lower the spikes resulting from electrostatic discharges. This will also keep both resistive and inductive effects to a minimum.
- All traces carrying high currents, especially if pulsed (tracks of the power loops), should be as short and wide as possible.

Optimize track routing:

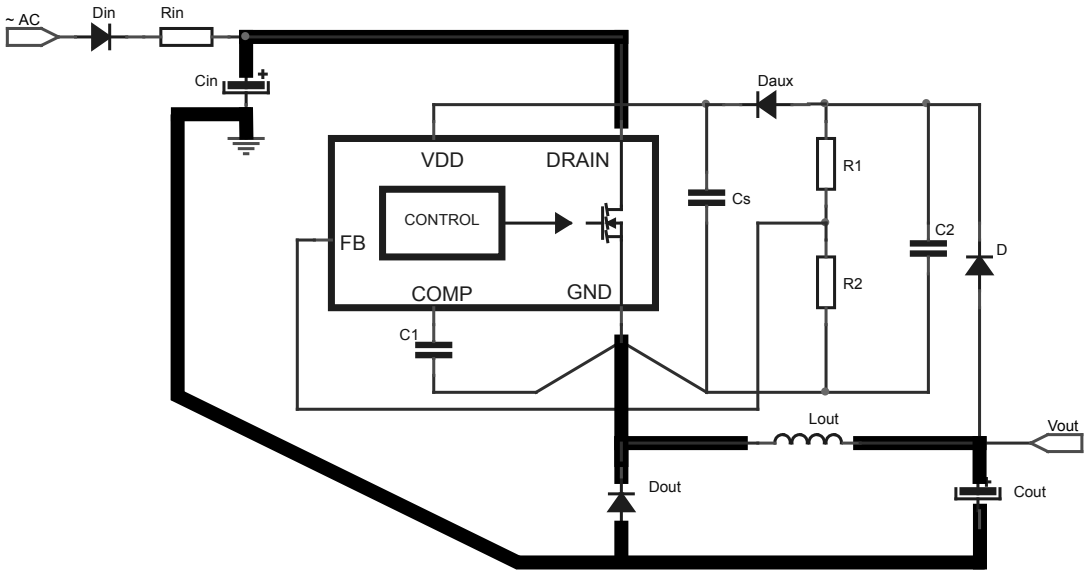
- as levels of pickup from static discharges are likely to be greater closer to the extremities of the board, it is wise to keep any sensitive lines away from these areas.
- Input and output lines will often need to reach the PCB edge at some stage, but they can be routed away from the edge as soon as possible where applicable.
- Since vias are considered inductive elements, they should be kept to a minimum in signal paths and avoided in power paths.

Improve thermal dissipation:

- An adequate copper area must be provided under the DRAIN pins to dissipate heat
- It is not recommended to place large copper areas on the GND.

Finally, in order to improve immunity against fast transient and capacitive noise injection, since pin number 4 is mechanically connected to the controller die pad of the frame, it is highly recommended to connect it to GND.

Figure 23. Recommended routing for buck converter



Revision history

Table 4. **Document revision history**

Date	Version	Changes
10-Oct-2019	1	Initial release.

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