15 V, 3 W buck converter based on VIPER122

Introduction

The STEVAL-VP12201B is a 15 V – 3 W power supply in buck topology featuring the VIPER122 offline high voltage converter.

The evaluation board has the following characteristics:

- Wide input range: 85 - 265 V_{AC}
- Meets IEC55022 Class B conducted EMI even with a reduced EMI filter, thanks to the frequency jittering feature
- RoHS compliant

Some of the main features of the VIPER122 include:

- 730 V avalanche rugged Power MOSFET
- Embedded HV start-up
- 60 kHz fixed switching frequency with jittering
- Embedded error amplifier internally referenced to 3.3 V
- Current mode PWM controller with drain current limit protection for easy compensation
- Several protection mechanisms:
  - delayed overload protection (OLP)
  - V_{CC} clamp protection
  - thermal shutdown with hysteresis

All protections are in auto restart mode

Figure 1. STEVAL-VP12201B evaluation board

1 Features and specifications

Table 1. STEVAL-VP12201B electrical specifications

Parameter	Min.	Typ.	Max.	Unit
AC main input voltage	85	-	265	V_{AC}
Main frequency (fL)	47	-	63	Hz
Output voltage	13.5	15	16.5	V
Output current	-	-	0.2	A
Rated output power	-	3	-	W
Output ripple voltage	-	-	100	mV
Standby input power at 230 V_{AC}	-	-	30	mW
Active mode efficiency	74.46	-	-	%
Active mode efficiency at 10% nameplate O/P	64.46	-	-	%
Ambient operating temperature	-	-	60	ºC

The power supply is set in buck topology. The input section includes resistor R1 for inrush current limiting, two diodes in series (D0 and D1) and an LC filter (L1, C1) for rectification and EMC suppression.

The EA-IN pin is the inverting input of the internal transconductance error amplifier, internally referenced to 3.3 V, which allows the straightforward setting output voltage value through the R4a-R4b-R3 voltage divider between the output terminal and the EA-IN pin, according to the following equation:

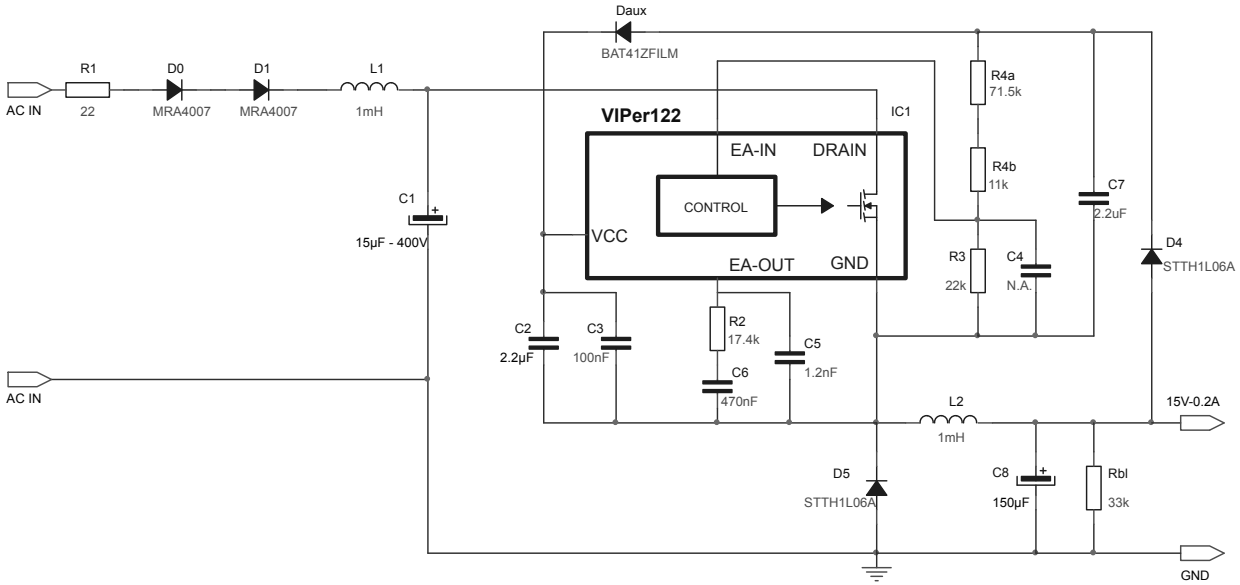
$$V_{OUT} = 3.3V \cdot \left(1 + \frac{R_{4a} + R_{4b}}{R_3}\right) \quad (1)$$

The R2, C5 and C6 compensation network is connected between the EA-OUT pin (which is the output of the error amplifier) and the GND pin.

The bleeder resistor Rbl provides about 0.45 mA minimum load in order to avoid overvoltage when the output load is disconnected. This value is a trade-off between output voltage increase and the extra power consumption under no load conditions.

1.1 Schematic diagram

Figure 2. **STEVAL-VP12201B circuit schematic**



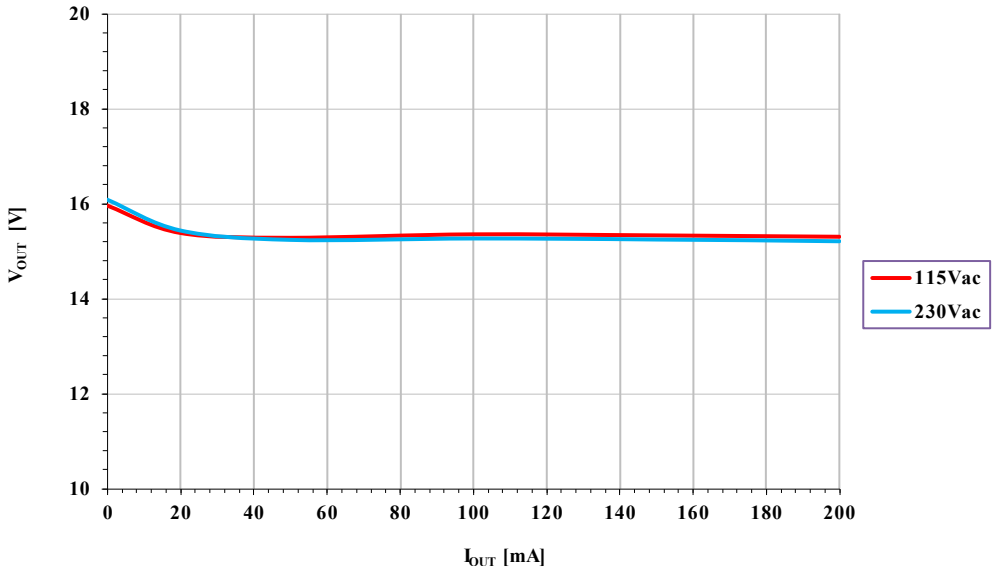
1.2 Bill of materials

Table 2. **STEVAL-VP12201B bill of materials**

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
1	1	C1	15µF,400V, ±20%	ELCAP, Dia 10mm x H 18mm Pitch 5mm	Rubycon	400AX15MEFC10X16
2	2	C2, C7	2.2µF,50V, ±10%	Ceramic Capacitor X5R, 0805	Murata	GRM21BR61H225KA73L
3	1	C3	100nF, 50V, ±10%	Ceramic Capacitor X7R, 0603	Wurth Elektronik	885012206095
4	1	C4	not mounted	Ceramic Capacitor, 0603	-	-
5	1	C5	1.2nF, 50V,±5%	Ceramic Capacitor C0G, 0603	Murata	GRM1885C1H122JA01D
6	1	C6	470nF, 50V, ±10%	Ceramic Capacitor X5R, 0603	Murata	GRM188R61H474KA12D
7	1	C8	150µF,25V, ±20%	ELCAP, Dia 6.3mm x H 12.5mm Pitch 2.5mm	Rubycon	25ZLH150MEFC6.3X11
8	2	D0, D1	1000V, 1A	Power Rectifier Diode, SMA	ON Semiconductor	MRA4007T3G
9	2	D4, D5	600V	Ultrafast Rectifier Diode, SMA	ST	STTH1L06A
10	1	Daux	100V	Schottky Diode, SOD-123	ST	BAT41ZFILM
11	1	IC1	- Offline HV Converter, SSOP		ST	VIPER122LSTR
12	1	L1	1mH,±5%	Axial Inductor, Through Hole	EPCOS	B82144A2105J000
13	1	L2	1mH,±10%	Radial Inductor, Dia 9mm x H 12.2mm	Bourns	RLB9012-102KL
14	2	M1, M2	250Vca, 13.5A	Input Connector, Output Connector, Through Hole 5.08mm pitch	TE Connectivity	282837-2
15	1	R1	22Ω, 1W,±5%	Power Metal Oxide Film Resistor 300ppm/°C, Through Hole	TE Connectivity	ROX1SJ22R
16	1	R2	17.4kΩ,0.1W, ±1%	Stand. Film Resistor 100ppm/°C, 0603	Panasonic	ERJ3EKF1742V
17	1	R3	22kΩ, 0.1W,±1%	Stand. Film Resistor 100ppm/°C, 0603	Panasonic	ERJ3EKF2202V
18	1	R4a	71.5kΩ,0.1W, ±1%	Stand. Film Resistor 100ppm/°C, 0603	Panasonic	ERJ3EKF7152V
19	1	R4b	11kΩ, 0.1W,±1%	Stand. Film Resistor 100ppm/°C, 0603	Panasonic	ERJ3EKF1102V
20	1	Rbl	33kΩ, 0.1W,±1%	Stand. Film Resistor 100ppm/°C, 0603	Panasonic	ERJU03F3302V

1.3 Output voltage characteristics

Figure 3. **Output voltage load regulation at nominal AC input voltages**



1.4 Efficiency measurements

Any external power supply (EPS) has to meet the international regulation agency limits.
The European code of conduct (EC CoC version 5) limit is taken as reference for our measurements.

Table 3. **EC CoC version 5 energy-efficiency criteria for active mode (excluding low voltage external power supplies), Tier2**

Nameplate output power (Pno)	Minimum average efficiency (expressed as a decimal)
0 to ≤ 1 watt	≥ 0.5 *Pno + 0.169
> 1 to ≤ 49 watts	≥[0.071* ln (Pno)] - 0.00115*Pno + 0.670
> 49 watts	≥0.890

According to the table above, the minimum average efficiency is 74.46%, measured as the average of the efficiencies at 25%, 50%, 75% and 100% of the rated output power at nominal input voltages (V_{IN} =115 V_{AC} and V_{IN} = 230 V_{AC}).
Another requirement is the efficiency measured at 10% of the rated output power, according to the table below.

Table 4. **EC CoC version 5 energy-efficiency criteria for active mode (excluding low voltage external power supplies) at 10% maximum output load, Tier 2**

Nameplate output power (Pno)	Minimum average efficiency (expressed as a decimal)
0 to ≤ 1 watt	≥ 0.5 *Pno + 0.060
> 1 to ≤ 49 watts	≥[0.071 * ln (Pno)] – 0.00115 * Pno + 0.570
> 49 watts	≥0.790

For the considered application the minimum efficiency is 64.46%. The following tables show all the efficiency measurement results.

Table 5. Average efficiency at 115 V_{AC}

Load (%)	I_{OUT}(A)	V_{OUT}(V)	P_{IN}(W)	P_{OUT}(W)	Efficiency (%)
25%	0.05	15.27	0.936	0.764	81.62
50%	0.10	15.34	1.858	1.534	82.56
75%	0.15	15.32	2.865	2.298	80.21
100%	0.20	15.28	3.948	3.056	77.41
Average efficiency					80.45

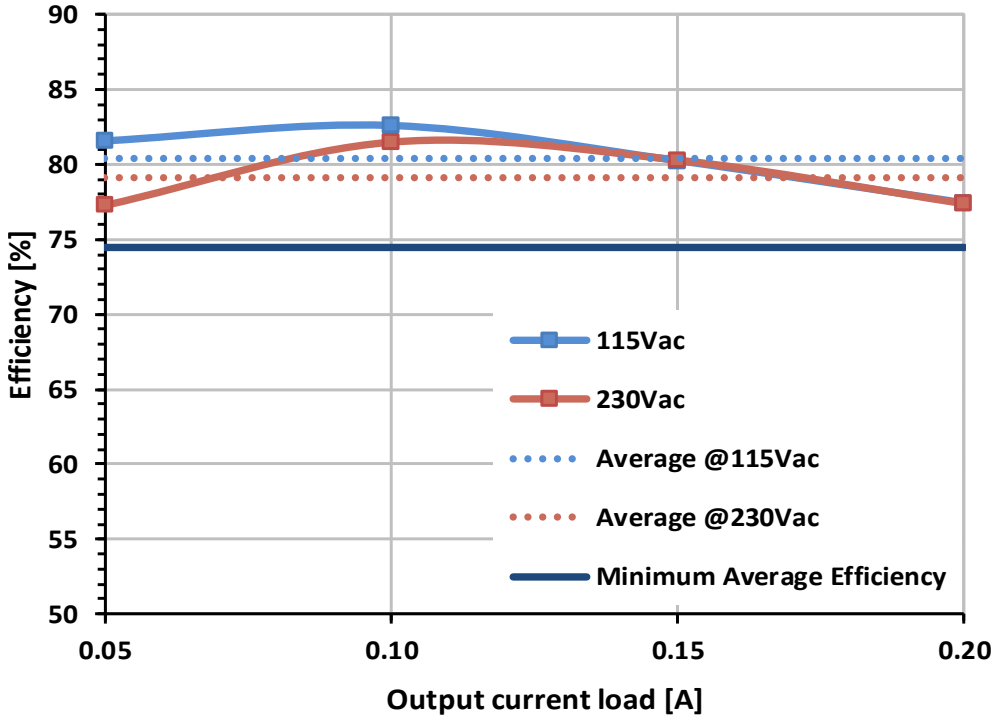
Table 6. Average efficiency at 230 V_{AC}

Load (%)	I_{OUT}(A)	V_{OUT}(V)	P_{IN}(W)	P_{OUT}(W)	Efficiency (%)
25%	0.05	15.12	0.978	0.756	77.30
50%	0.10	15.15	1.860	1.515	81.45
75%	0.15	15.15	2.831	2.273	80.29
100%	0.2	15.10	3.901	3.020	77.42
Average efficiency					79.12

Table 7. Average efficiency at 10% of the max. output load

V_{IN}[V_{AC}]	I_{OUT}(A)	V_{OUT}(V)	P_{IN}(W)	P_{OUT}(W)	Efficiency (%)
115	0.02	15.38	0.405	0.308	76.05
230	0.02	15.31	0.432	0.306	70.83

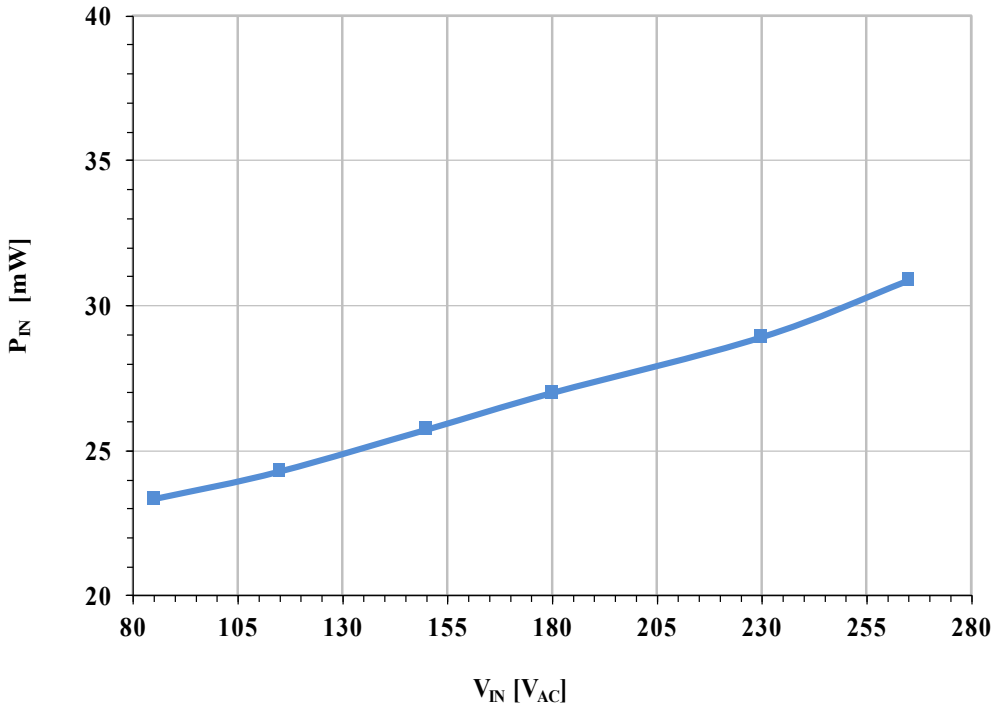
Figure 4. Efficiency vs. output current load



1.5 No load consumption

The input power of the converter has been measured in no load condition: as the converter works in burst mode, the average switching frequency is reduced, minimizing the frequency related losses.

Figure 5. No load consumption vs. input voltage

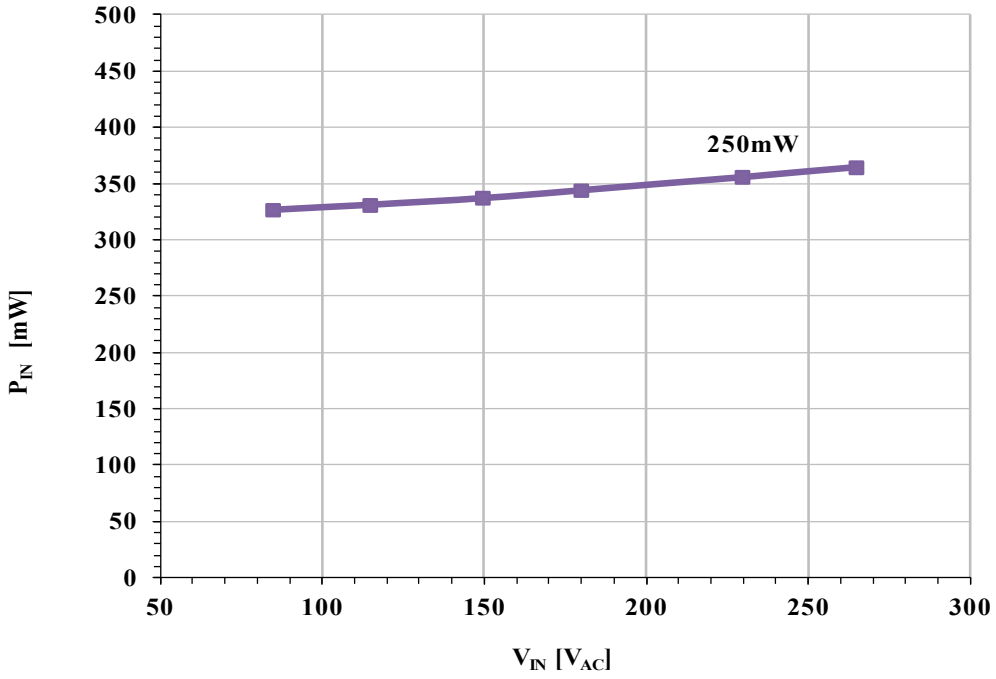


1.6 Light load consumption

The STEVAL-VP12201B input power under light load conditions is also shown.

The board is compliant with EuP Lot 6, with an efficiency higher than 50% when the output load is 250 mW, as required by the EPS.

Figure 6. Light load consumption at P_{OUT} = 250 mW



2 Typical waveforms

The GND voltage and output inductor current waveforms in full load condition are shown in the following images for minimum and maximum AC input voltages.

Figure 7. Output inductor current and GND voltage at full load at 85 V_{AC}

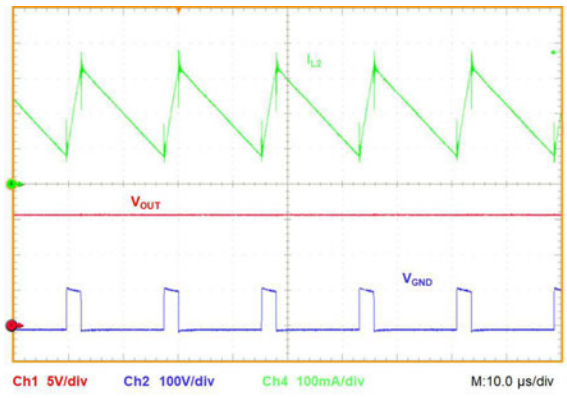
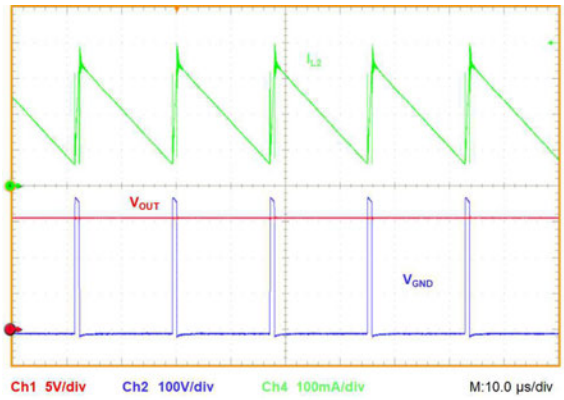


Figure 8. Output inductor current and GND voltage at full load at 265 V_{AC}



The GND voltage and output inductor current waveforms in full load condition are shown in the following images for the two nominal input voltages.

Figure 9. Output inductor current and GND voltage at full load at 115 V_{AC}

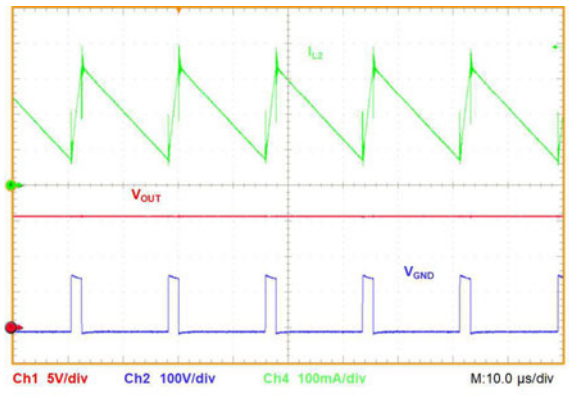
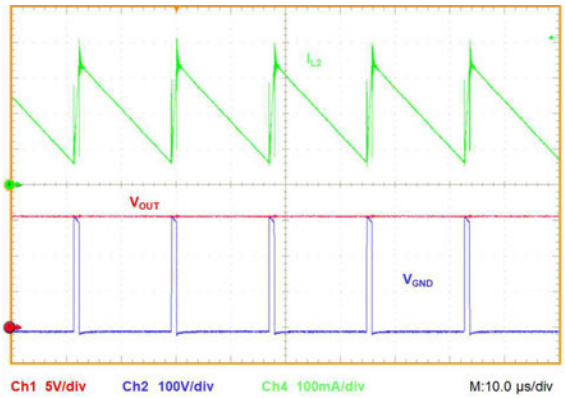


Figure 10. Output inductor current and GND voltage at full load at 230 V_{AC}



The output voltage ripple at the switching frequency is shown in the following images for full load at nominal voltages.

Figure 11. Output voltage ripple at full load at 115 V_{AC}

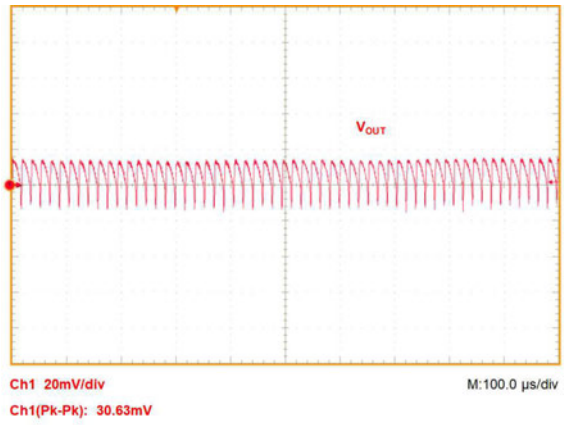
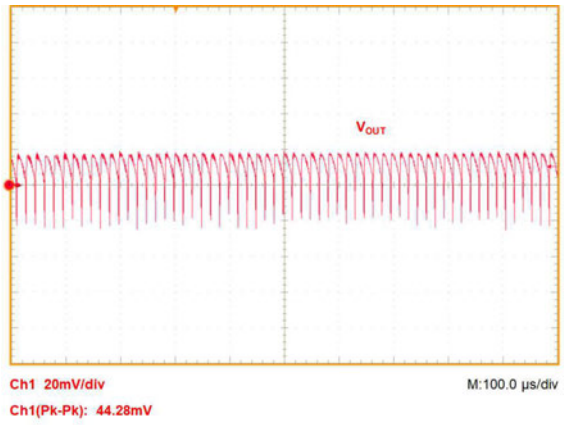


Figure 12. Output voltage ripple at full load at 230 V_{AC}



The output voltage ripple at the switching frequency is shown in the following images for no load at nominal voltages.

Figure 13. Output voltage ripple at no load at 115 V_{AC}

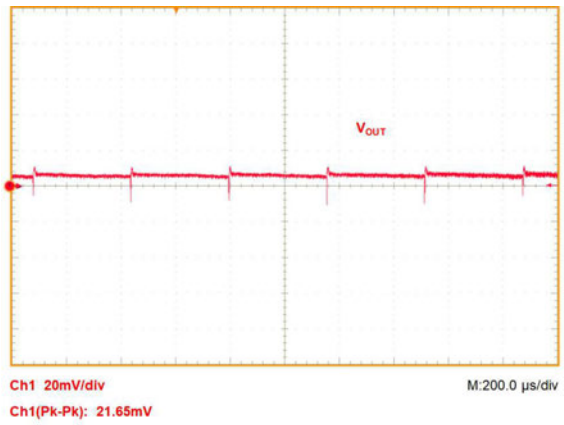
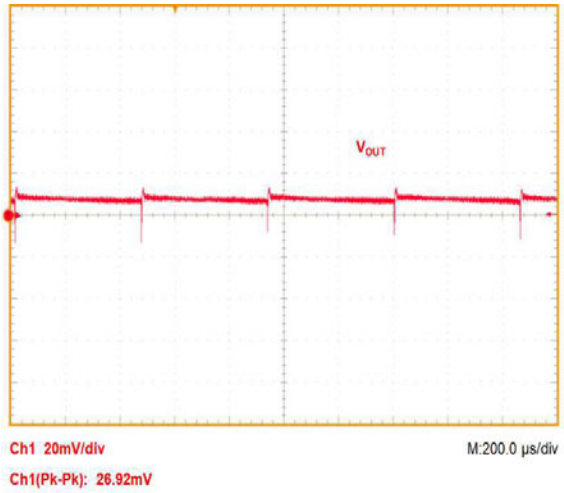


Figure 14. Output voltage ripple at no load at 230 V_{AC}



2.1 Dynamic step load regulation

In any power supply, it is important to measure the output voltage when the converter is subjected to dynamic load variations in order to ensure appropriate stability free of overvoltage and undervoltage events.

The test is performed by varying the output load from 0 to 0.2 A (100% of nominal value) for both nominal input voltages.

In the tested conditions, no abnormal oscillations were observed on the output, and over- and under-shoot were well within acceptable values.

Figure 15. Dynamic step load (I_{OUT} from 0 to 0.2 A) at 115 V_{AC}

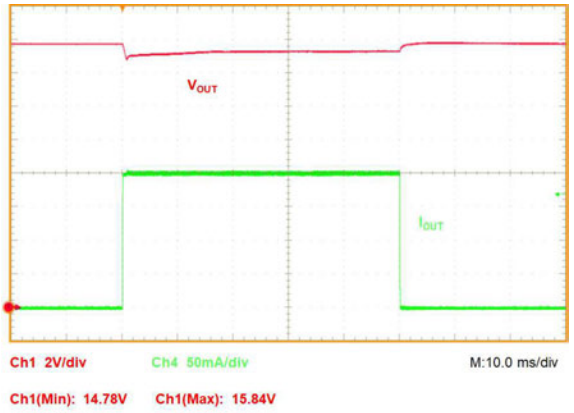
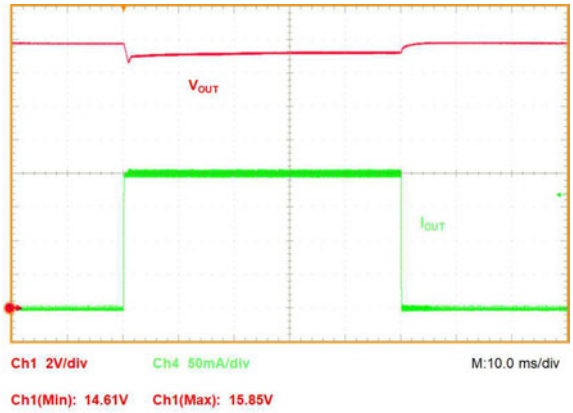


Figure 16. Dynamic step load (I_{OUT} from 0 to 0.2 A) at 230 V_{AC}



3 Startup

When the converter starts, the output capacitor is discharged and needs time to reach the steady state condition. During this time, the power demand from the control loop is at its maximum, leading to a deep continuous operating mode of the converter.

Another consideration is that when the MOSFET is switched on, it cannot be switched off before the minimum on time (T_{ON_MIN}) has elapsed. Because of the deep continuous working mode of the converter, an excessive drain current during T_{ON_MIN} can stress the component of the converter, the device itself, and the output inductor. Output inductor saturation may also occur under these conditions.

To avoid these negative effects, the VIPER122 implements an internal soft-start feature. As the device starts to work, the drain current is allowed to increase from zero to the maximum value gradually, regardless of the control loop request.

The soft-start time t_{SS} is internally set at 8.5 ms (typical value).

The following figures show the soft-start phase of the present converter at maximum load, for nominal input voltages (115 $V_{AC}$and 230 V_{AC}).

Figure 17. Startup at 115 V_{AC}, full load

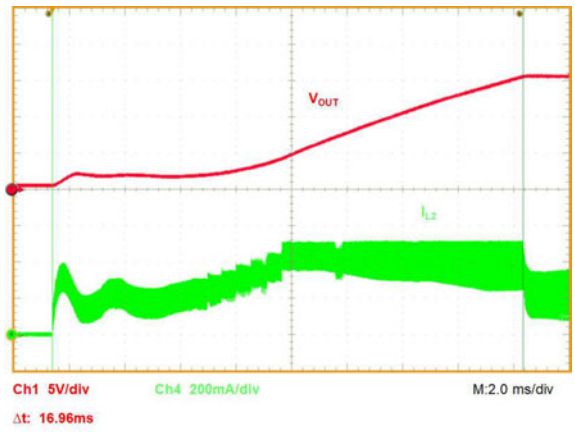


Figure 18. Startup at 115 V_{AC}, full load - zoom

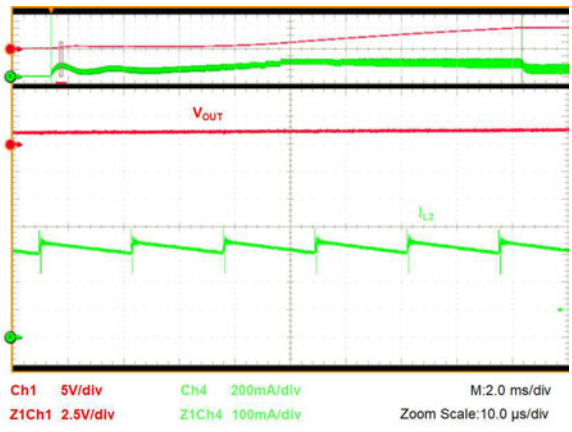


Figure 19. Startup at 230 V_{AC}, full load

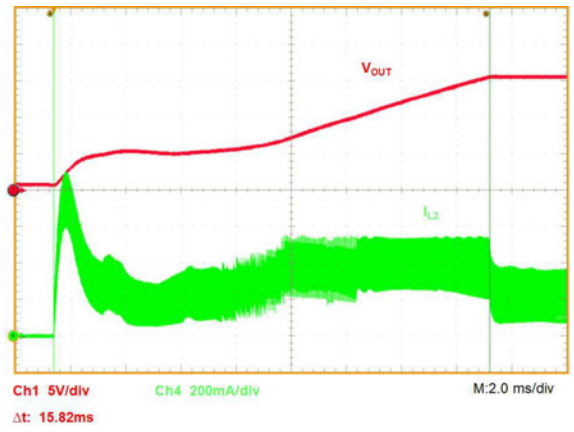
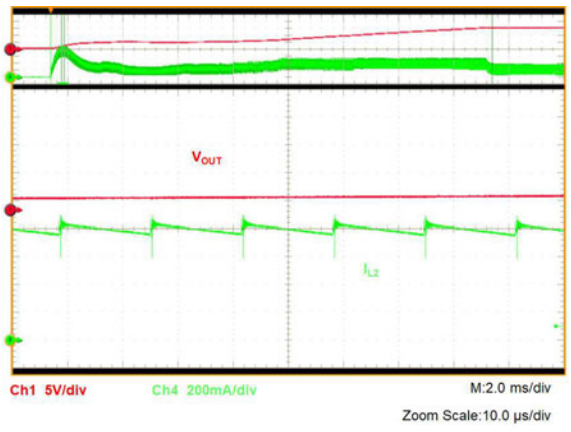


Figure 20. Startup at 230 V_{AC}, full load - zoom



4 Protection features

4.1 Overload and short circuit protection

When the load power demand increases, the feedback loop reacts by increasing the voltage on the EA-OUT pin. In this way, the PWM current set point increases and the power delivered to the output rises. This process ends when the delivered power equals the load power request.

In case of overload or output short circuit, the drain current value reaches the I_{DLIM}. For every cycle that this condition is met, an internal OCP counter is incremented and the protection is tripped if the overload condition persists for 50 ms. The power section is turned off and the converter is disabled for 1s. After this time has elapsed, the IC resumes switching and the protection continues to be triggered indefinitely if the fault condition remains. This ensures a low converter restart attempt rate, providing safe operation with extremely low power throughput and avoiding IC overheating in case of repeated overload events.

Furthermore, the internal soft start function is invoked at startup after protection tripping. After the fault is removed, the IC resumes working normally. If the fault is removed before the protection is triggered, the counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped. If the short circuit is removed during the 1s time, the IC waits until this time has elapsed before resuming to switch.

Figure 21. Overload event, OLP tripping

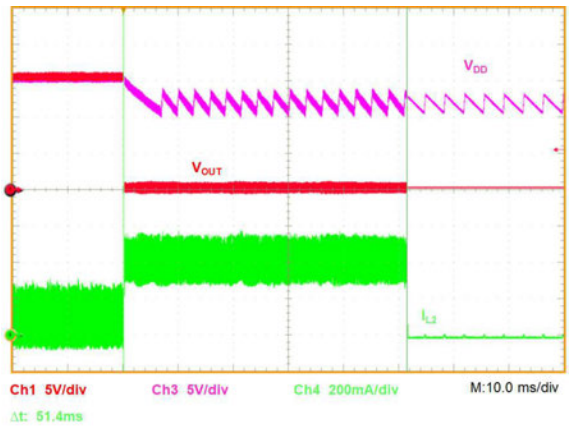


Figure 22. Overload event, continuous overload

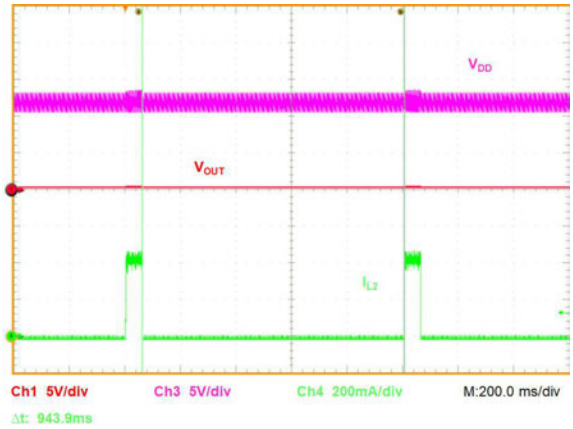


Figure 23. Overload event, steady state - zoom

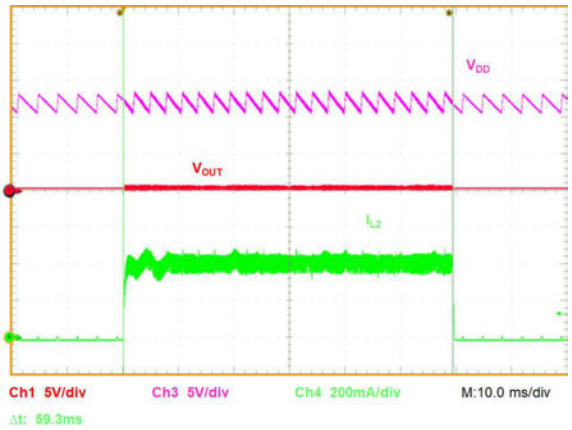
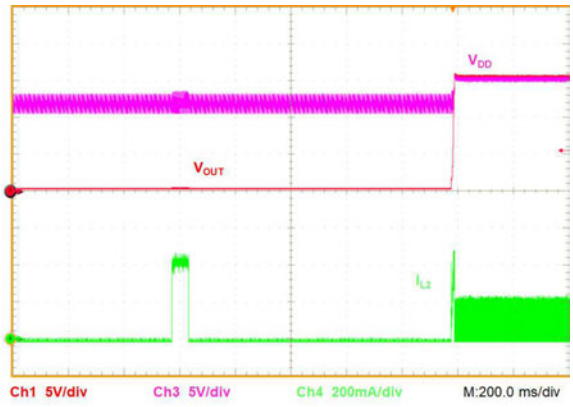


Figure 24. Overload event, fault removed and autorestart



4.2 V_{CC} clamp protection

As the loop fails (R4a and R4b open or R3 shorted), the output voltage increases and the VIPER122 runs at its maximum current limitation. The voltage on V_{CC} pin also increases as it is linked to the V_{OUT} voltage through diode D_{aux}.

If voltage V_{CC} increases up to the internal V_{CC} clamp threshold (23.5 V minimum) with a clamp current injected on the pin greater than the latch threshold I_{CC_FAIL} (4 mA minimum), and the VIPER122 operates at its drain current limitation, a fault signal is internally generated and the device stops switching.

The failure of the loop is simulated by opening the high-side resistor of the output voltage divider (R4a and R4b). The same behavior can be induced by shorting the low-side resistor (R3).

Figure 25. V_{CC} clamp protection - tripping

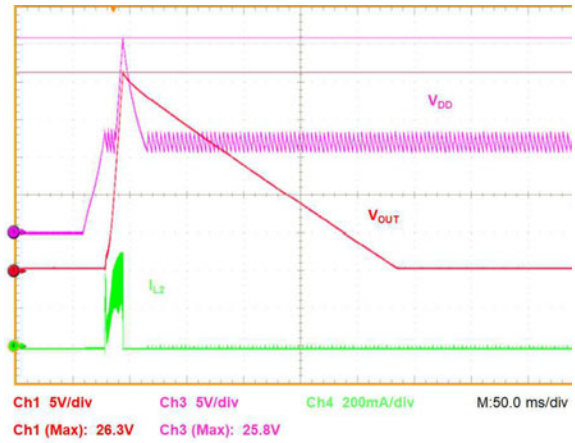
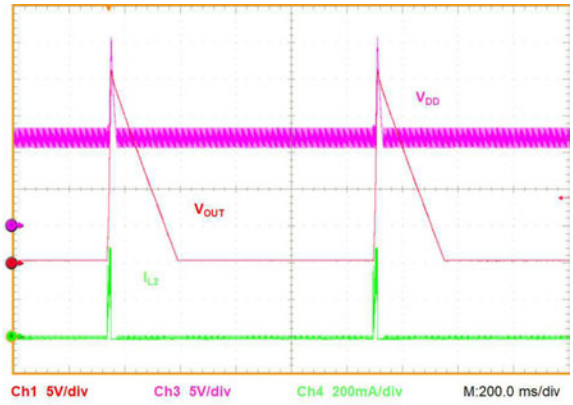


Figure 26. V_{CC} clamp protection - steady-state



5 Conducted noise measurements

The VIPER122 frequency jittering feature allows the spectrum to be spread over frequency bands rather than being concentrated on single frequency value. Especially when measuring conducted emission with the average detection method, the level reduction can be several dBµV.

A pre-compliance test for the EN55022 (Class B) European normative was performed and average measurements of the conducted noise emissions at full load and nominal mains voltages are shown in the following figures.

Figure 27. CE average measurement at 115 V_{AC} full load

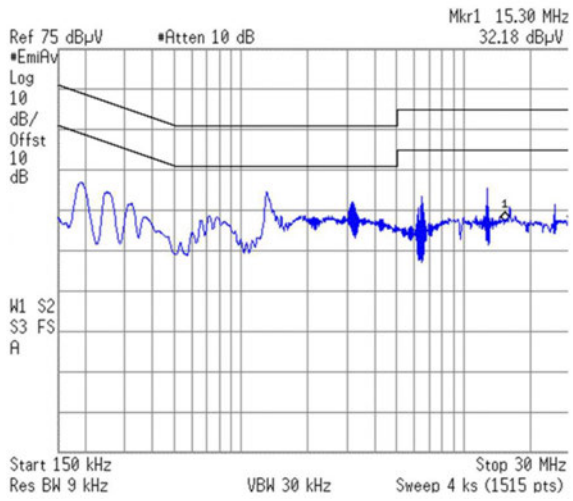
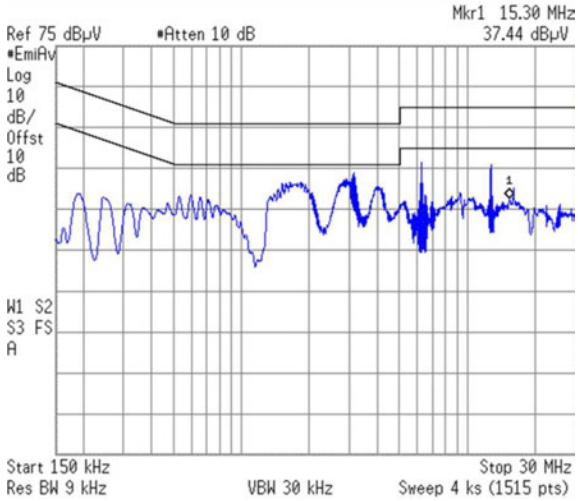


Figure 28. CE average measurement at 230 V_{AC} full load



6 Thermal measurements

A thermal analysis of the board has been performed using an IR camera for the two nominal input voltages (115 V_{AC} and 230 V_{AC}) in full load condition. The results are shown below.

Figure 29. **Thermal map at 115 V_{AC}, full load**

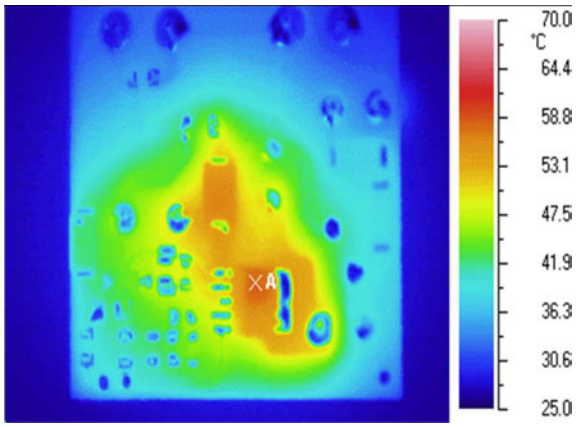


Figure 30. **Thermal map at 230 V_{AC}, full load**

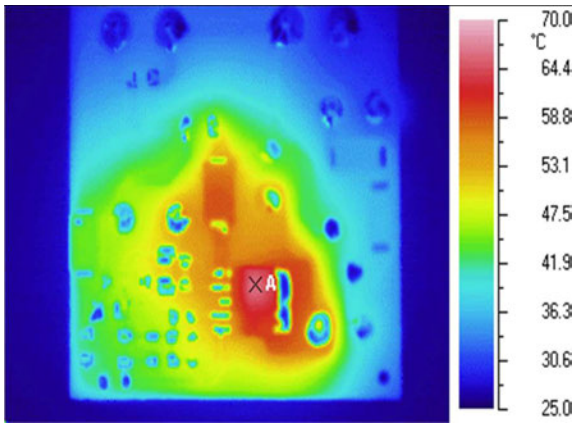


Table 8. **Temperature of VIPER122 (T_{AMB} = 25 °C, emissivity = 0.95 for all points**

Reference	Point	Temperature (°C)	
		115 V_{AC}	230 V_{AC}
VIPER122	A	58.5	68.2

7 Conclusions

A buck converter has been described and characterized, with the bench results showing good performance in terms of line and load regulation.

The efficiency performance has been compared with the requirements of the EC CoC and DoE regulation programs for external AC-DC adapters with highly positive results, where the measured active mode efficiency is always higher than the required minimum.

The STEVAL-VP12201B reference design meets the EN55022 – Class B EMI regulation standard using a simple and low-cost LC input filter.

Appendix A Feedback loop calculation guidelines

A.1 CCM buck converter transfer function

The control-to-output transfer function of the buck converter in CCM, $G_{VC}(s)$, is given by:

$$G_{VC}(s) = H_0 \cdot \frac{1 + \frac{s}{\omega_{Z1}}}{1 + \frac{s}{\omega_{P1}}} \cdot G_{HF}(s) \quad (2)$$

Gain, poles and zero are defined below:

$$H_0 = \frac{R_0}{H_{COMP}} \cdot \frac{1}{1 + \frac{R_0 \cdot T_S}{L} \cdot (0.5 - D)} \quad (3)$$

$$\omega_{Z1} = \frac{1}{R_C \cdot C_0} \quad (4)$$

$$\omega_{P1} = \frac{1}{R_0 \cdot C_0} + \frac{T_S}{L \cdot C_0} \cdot (0.5 - D) \quad (5)$$

$$G_{HF}(s) = \frac{1}{1 + \frac{s}{Q_0 \cdot \omega_0} + \frac{s^2}{\omega_0^2}} \quad (6)$$

$$\omega_0 = \frac{\pi}{T_S} \quad (7)$$

$$Q_0 = \frac{1}{\pi \cdot (0.5 - D)} \quad (8)$$

The term $G_{HF}(s)$ defines the high frequency characteristic, which is represented by a double pole located at half the switching frequency and is described by a second order system equation. It can also model the effect of the instability for the CCM buck with duty-cycle higher than 50%.

When the crossover frequency of the loop gain is low, $G_{HF}(s)$ is usually negligible.

A.2 Compensation design

To compensate the CCM buck, we use a type-2 compensator with the integrator effect to provide the high DC gain to minimize static error, and a pole-zero pair to boost the phase according the phase margin target.

The compensator is determined using a manual pole-zero placement technique where the zero is placed in the vicinity of the power stage dominant pole to cancel its effect, and the pole position is adjusted to achieve the required phase margin.

Follow the procedure below to design the compensation with a type 2 compensator:

Step 1. Select the crossover frequency f_C and the phase margin Φ_m .

Step 2. Evaluate the gain and phase of the plant at crossover frequency.

$$G_{VC}(f_C) = |G_{VC} \cdot (2 \cdot \pi \cdot f_C)| \quad (9)$$

$$\Phi_{VC}(f_C) = \arg[G_{VC} \cdot (2 \cdot \pi \cdot f_C)] \quad (10)$$

Step 3. The compensated open-loop gain must attain the unit gain at f_C with the required phase margin, so the compensator must be designed in order to have following gain and phase (at f_C):

$$G_{C(f_C)} = |G_C \cdot (2 \cdot \pi \cdot f_C)| = \frac{1}{G_{VC(f_C)}} \quad (11)$$

$$\Phi_{C(f_C)} = \arg[G_C \cdot (2 \cdot \pi \cdot f_C)] = 90 - 180 + \Phi_m - \Phi_{VC(f_C)} \quad (12)$$

Step 4. Cancel the pole of the plant, $f_{P(p)}$, by placing the zero of the compensator $f_{Z(C)}$ in the region $\alpha = 1$ to 5

$$f_{Z(C)} = \frac{\omega_{Z(C)}}{2 \cdot \pi} = \alpha \cdot f_{P(p)} \quad (13)$$

Step 5. Place the pole of the compensator to boost the phase and to obtain the desired phase margin

$$f_{P(C)} = \frac{f_C}{\tan\left[\tan^{-1}\left(\frac{f_C}{f_{Z(C)}}\right) - \Phi_{C(f_C)}\right]} \quad (14)$$

Step 6. Calculate the gain G_{C0}

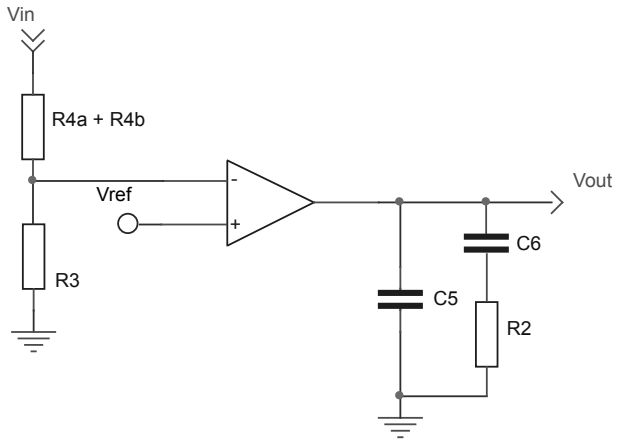
$$G_{C0} = G_{C(f_C)} \frac{\omega_C \cdot \sqrt{1 + \left(\frac{f_C}{f_{P(C)}}\right)^2}}{\sqrt{1 + \left(\frac{f_C}{f_{Z(C)}}\right)^2}} \quad (15)$$

The design of $G_C(s)$ is complete.

A.3 Synthesis of the compensator

The following figure shows the schematic of the Type 2 amplifier used in the VIPER122.

Figure 31. Type 2 compensator with OTA



The transfer function of this compensator can be expressed as the following:

$$G_C(s) = \frac{R_3 \cdot g_m}{(R_{4a} + R_{4b} + R_3) \cdot (C_5 + C_6)} \cdot \frac{1 + s \cdot R_2 \cdot C_6}{s \cdot \left[1 + s \cdot R_2 \cdot \left(\frac{C_6 \cdot C_5}{C_6 + C_5}\right)\right]} \quad (16)$$

The first component to be chosen are resistors R_{4a} and R_{4b}, which must be high enough to render the current offset entering in the inverting pin negligible, but low enough to ensure that other compensation components do not have to be too large. Resistor R_3 is fixed to set the DC operating point of the loop. Of course, R_{4a}, R_{4b} and R_3 play a role in determining the gain of the compensator.

Step 1. Set the values for R_{4a}, R_{4b} and R_3.

$$R_{4a} = 71.5\ k\Omega \quad (17)$$

$$R_{4b} = 11\ k\Omega \quad (18)$$

$$R_3 = 22\ k\Omega \quad (19)$$

Step 2. Calculate the value for C_5

$$C_5 = \frac{f_{Z1}}{f_{P1}} \cdot \frac{R_3 \cdot g_m}{G_{C0} \cdot (R_{4a} + R_{4b} + R_3)} \approx 1.1\ nF \quad (20)$$

The selected value for C_5 is:

$$C_5 = 1.2\ nF \quad (21)$$

Step 3. Calculate C_6

$$C_6 = \frac{R_3 \cdot g_m}{G_{C0} \cdot (R_{4a} + R_{4b} + R_3)} - C_5 \approx 387\ \text{nF} \quad (22)$$

The selected value for C_6 is:

$$C_6 = 470\ \text{nF} \quad (23)$$

Step 4. Calculate R_2

$$R_2 = \frac{1}{2 \cdot \pi \cdot f_{Z1} \cdot C_6} \approx 17\ \text{k}\Omega \quad (24)$$

The selected value for R_2 is:

$$R_2 = 17.4\ \text{k}\Omega \quad (25)$$

The resulting crossover frequency f_C and the phase margin Φ_m are:

$$f_C \approx 1.7\ \text{kHz} \quad (26)$$

$$\Phi_m \approx 79 \quad (27)$$

Appendix B Layout guidelines and design recommendations

An appropriate PCB layout is essential for the correct operation of any switch-mode converter. It ensures the delivery of clean signals to the IC and higher immunity to external and switching noise, as well as reducing radiated and conducted electromagnetic interference, all of which help a given solution satisfy EMC requirements.

Below are some general concepts to keep in mind when designing SMPS circuit layouts.

Separate signal and power tracks:

- Traces carrying signal currents should generally be run at a distance from other tracks carrying pulsed currents or with rapidly changing voltages.
- Signal ground traces should be connected to the IC signal ground, GND, using a single "star point", placed close to the IC.
- Power ground traces should be connected to the IC power ground, GND.
- The compensation network should be connected to the EA-OUT, maintaining the trace to GND as short as possible.
- In two-layer PCBs, it is a good practice to route signal traces on one PCB side and power traces on the other side.

Filter sensitive pins and crucial points on the circuit:

- A small high-frequency bypass capacitor to GND might be useful to get a clean bias voltage for the signal part of the IC and protect the IC itself during EFT/ESD tests.
- A low ESL ceramic capacitor (a few hundred pF up to 0.1 µF) should be connected across VCC and GND, placed as close as possible to the IC.
- With flyback topologies, when the auxiliary winding is used, it is suggested to connect the VCC capacitor on the auxiliary return and then to the main GND using a single track.

Keep power loops as confined as possible:

- Minimize the area circumscribed by current loops where highly pulsed currents flow in order to reduce its parasitic self-inductance and the radiated electromagnetic field; this will greatly reduce the electromagnetic interferences produced by the power supply during the switching.
- In a flyback converter the most critical loops are:
  - The one with the input bulk capacitor, the power switch and the power transformer
  - the one with the snubber.
  - the one with the secondary winding, the output rectifier and the output capacitor.
- In a buck converter the most critical loop is:
  - The one with the input bulk capacitor, the power switch, the power inductor, the output capacitor and the free-wheeling diode.

Reduce line lengths as any wire will act as an antenna:

- With the very short rise times exhibited by EFT pulses, any antenna has the capability of receiving high voltage spikes. Shorter lines reduce the level of radiated energy received and lower the spikes resulting from electrostatic discharges. This will also keep both resistive and inductive effects to a minimum.
- All traces carrying high currents, especially if pulsed (tracks of the power loops), should be as short and wide as possible.

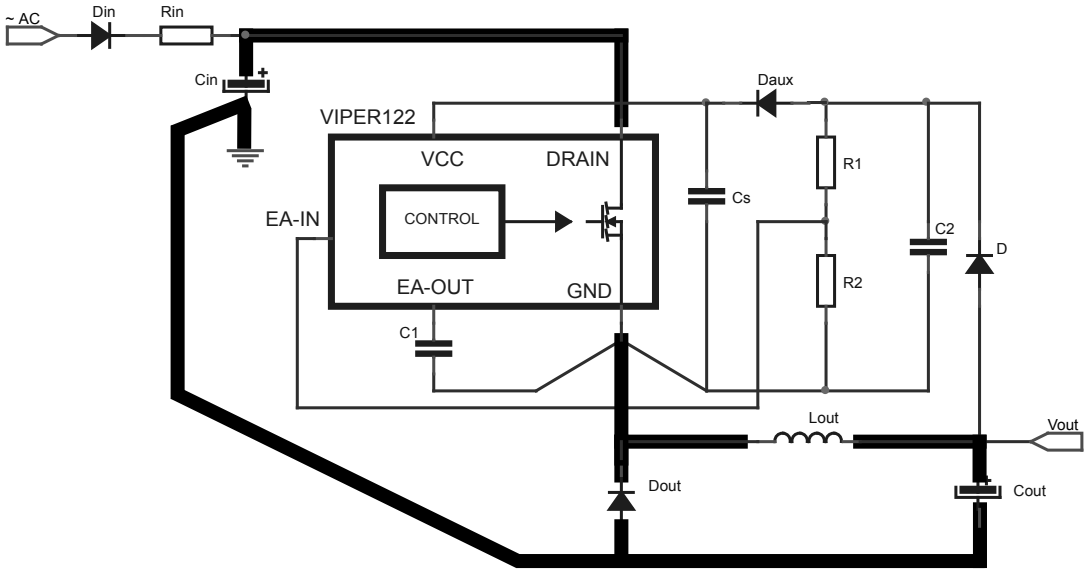
Optimize track routing:

- as levels of pickup from static discharges are likely to be greater closer to the extremities of the board, it is wise to keep any sensitive lines away from these areas.
- Input and output lines will often need to reach the PCB edge at some stage, but they can be routed away from the edge as soon as possible where applicable.
- Since vias are considered inductive elements, they should be kept to a minimum in signal paths and avoided in power paths.

Improve thermal dissipation:

- An adequate copper area must be provided under the DRAIN pins to dissipate heat
- It is not recommended to place large copper areas on the GND.

Figure 32. **Recommended routing for buck converter**



Revision history

Table 9. **Document revision history**

Date	Version	Changes
09-Oct-2019	1	Initial release.
02-Apr-2020	2	Updated Section 1 Characteristics and specifications.

Contents

1 **Features and specifications** 2
1.1 Schematic diagram 3
1.2 Bill of materials 4
1.3 Output voltage characteristics 5
1.4 Efficiency measurements 5
1.5 No load consumption 7
1.6 Light load consumption 7
2 **Typical waveforms** 9
2.1 Dynamic step load regulation 10
3 **Startup** 12
4 **Protection features** 13
4.1 Overload and short circuit protection 13
4.2 V_{CC} clamp protection 14
5 **Conducted noise measurements** 15
6 **Thermal measurements** 16
7 **Conclusions** 17
Appendix A **Feedback loop calculation guidelines** 18
A.1 CCM buck converter transfer function 18
A.2 Compensation design 18
A.3 Synthesis of the compensator 19
Appendix B **Layout guidelines and design recommendations** 21
Revision history 23

List of figures

Figure 1. STEVAL-VP12201B evaluation board . . . 1
Figure 2. STEVAL-VP12201B circuit schematic . . . 3
Figure 3. Output voltage load regulation at nominal AC input voltages . . . 5
Figure 4. Efficiency vs. output current load . . . 6
Figure 5. No load consumption vs. input voltage . . . 7
Figure 6. Light load consumption at P_{OUT} = 250 mW . . . 8
Figure 7. Output inductor current and GND voltage at full load at 85 V_{AC} . . . 9
Figure 8. Output inductor current and GND voltage at full load at 265 V_{AC} . . . 9
Figure 9. Output inductor current and GND voltage at full load at 115 V_{AC} . . . 9
Figure 10. Output inductor current and GND voltage at full load at 230 V_{AC} . . . 9
Figure 11. Output voltage ripple at full load at 115 V_{AC} . . . 10
Figure 12. Output voltage ripple at full load at 230 V_{AC} . . . 10
Figure 13. Output voltage ripple at no load at 115 V_{AC} . . . 10
Figure 14. Output voltage ripple at no load at 230 V_{AC} . . . 10
Figure 15. Dynamic step load (I_{OUT} from 0 to 0.2 A) at 115 V_{AC} . . . 11
Figure 16. Dynamic step load (I_{OUT} from 0 to 0.2 A) at 230 V_{AC} . . . 11
Figure 17. Startup at 115 V_{AC}, full load . . . 12
Figure 18. Startup at 115 V_{AC}, full load - zoom . . . 12
Figure 19. Startup at 230 V_{AC}, full load . . . 12
Figure 20. Startup at 230 V_{AC}, full load - zoom . . . 12
Figure 21. Overload event, OLP tripping . . . 13
Figure 22. Overload event, continuous overload . . . 13
Figure 23. Overload event, steady state - zoom . . . 13
Figure 24. Overload event, fault removed and autorestart . . . 13
Figure 25. V_{CC} clamp protection - tripping . . . 14
Figure 26. V_{CC} clamp protection - steady-state . . . 14
Figure 27. CE average measurement at 115 V_{AC} full load . . . 15
Figure 28. CE average measurement at 230 V_{AC} full load . . . 15
Figure 29. Thermal map at 115 V_{AC}, full load . . . 16
Figure 30. Thermal map at 230 V_{AC}, full load . . . 16
Figure 31. Type 2 compensator with OTA . . . 19
Figure 32. Recommended routing for buck converter . . . 22

List of tables

Table 1. STEVAL-VP12201B electrical specifications . . . 2
Table 2. STEVAL-VP12201B bill of materials . . . 4
Table 3. EC CoC version 5 energy-efficiency criteria for active mode (excluding low voltage external power supplies), Tier2 5
Table 4. EC CoC version 5 energy-efficiency criteria for active mode (excluding low voltage external power supplies) at 10% maximum output load, Tier 2 . . . 5
Table 5. Average efficiency at 115 V_{AC} . . . 6
Table 6. Average efficiency at 230 V_{AC} . . . 6
Table 7. Average efficiency at 10% of the max. output load . . . 6
Table 8. Temperature of VIPER122 (T_{AMB} = 25 °C, emissivity = 0.95 for all points . . . 16
Table 9. Document revision history . . . 23