Getting started with STM32H723/733, STM32H725/735 and STM32H730 Value Line hardware development

Introduction

This application note is intended for system designers who develop applications based on STM32H723/33, STM32H725/35 and STM32H730 microcontroller lines, and need an implementation overview of the following hardware features:

- Power supply
- Package selection
- Clock management
- Reset control
- Boot mode settings
- Debug management.

This document describes the minimum hardware resources required to develop an application based on STM32H723/33, STM32H725/35 and STM32H730 microcontrollers.

Reference documents

- *STM32H72x and STM32H73x datasheets*
- *STM32H723/733, STM32H725/735 and STM32H730 advanced Arm®-based 32-bit MCUs* (RM0468)
- *STM32H723/733, STM32H725/735 and STM32H730 errata sheet* (ES0491)

The following documents are available on *www.st.com* website.

- *Oscillator design guide for STM8S, STM8A and STM32 microcontrollers application note* (AN2867)
- *STM32 microcontroller system memory boot mode application note* (AN2606).

1 General information

This document applies to STM32H723/33, STM32H725/35 and STM32H730Arm®-based microcontroller lines.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Power supplies

2.1 Introduction

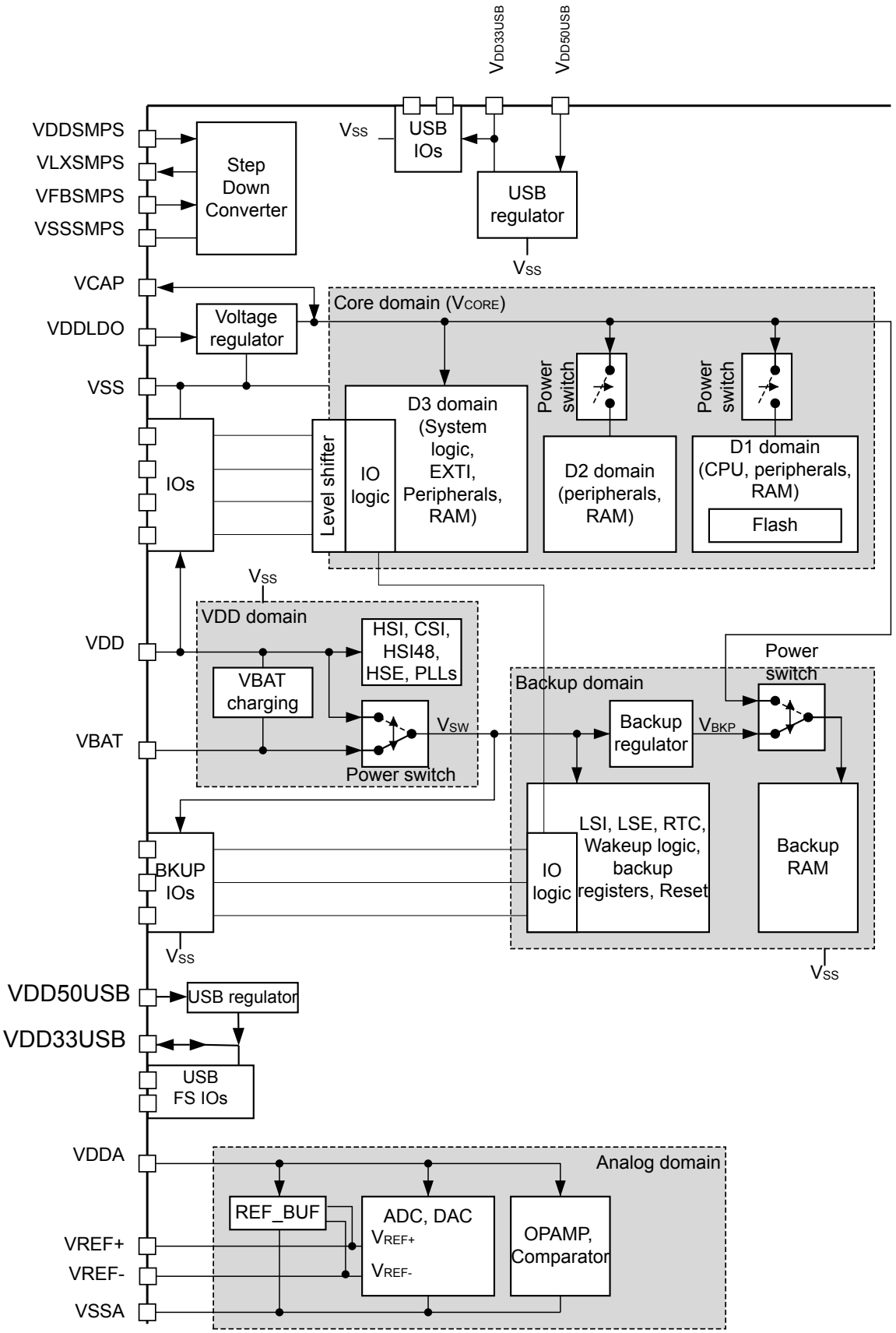
The STM32H723/33, STM32H725/35 and STM32H730 are highly integrated microcontrollers that are based on the Arm® Cortex®-M7 32-bit core (refer to the datasheets/databriefs for details).

The STM32H723/33, STM32H725/35 and STM32H730 microcontrollers require at least one single power supply to be fully operational.

Additional power supplies or voltage references are required for some use cases. The general design guidelines are explained in the following sections. The figure below illustrates the power supply layout.

In all the diagrams, the gray boxes represent power domains.

Figure 1. Power supplies



Note: VDDSMPS, VLXSMPS, VFBSMPS and VSSSMPS are available only on STM32H725/735 and STM32H730 devices.

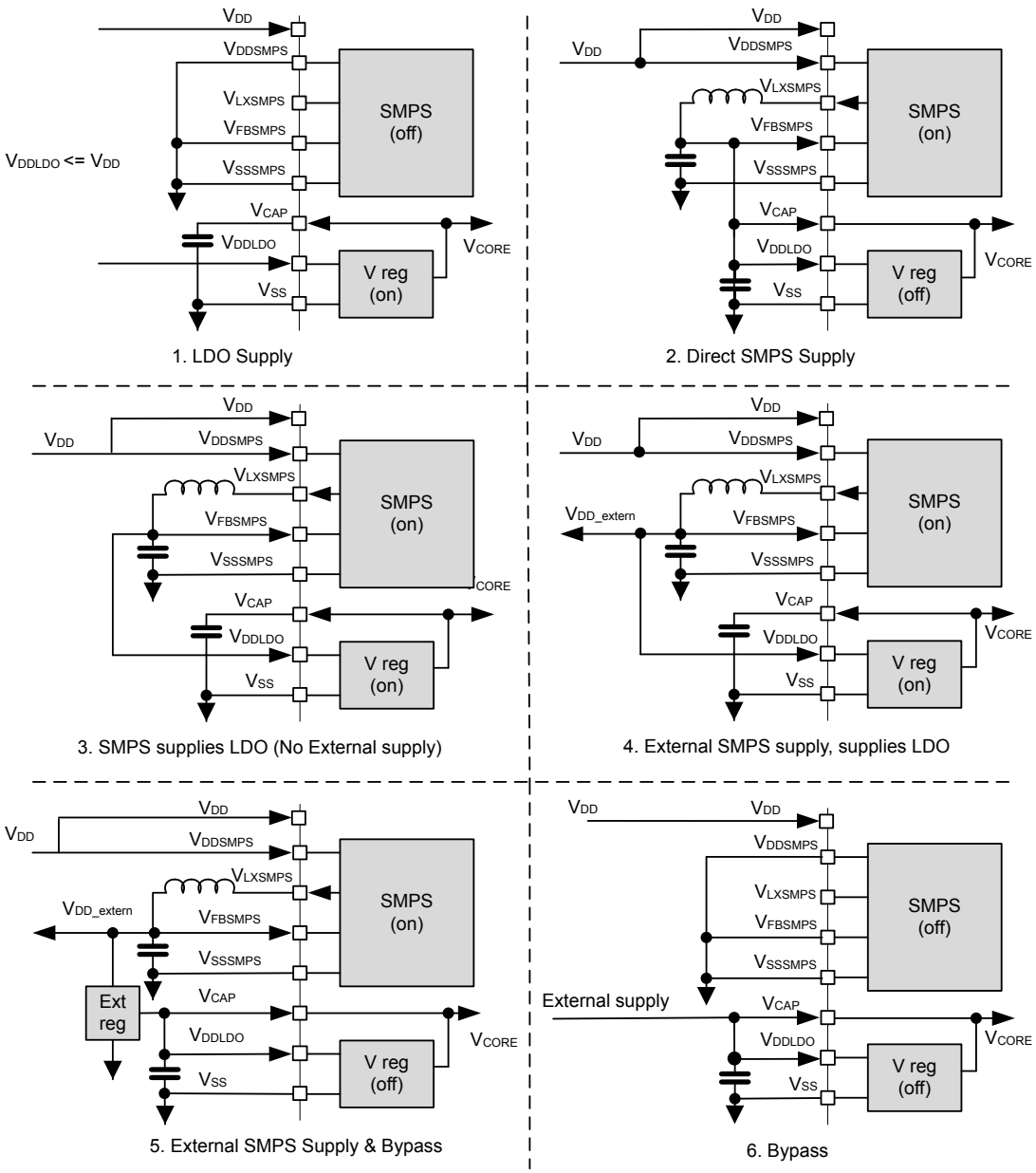
Note: On STM32H723/733, VDDLDO is not available on a pin/ball. It is internally connected to VDD.

Table 1. PWR input/output signals connected to package pins/balls

Pin name	Signal type	Description
VDD	Supply input	Main I/O and V_{DD} domain supply input.
VSS	Supply input	Main ground.
VDDA	Supply input	External analog power supply for analog peripherals.
VSSA	Supply input	Separated isolated ground for analog peripherals.
VBAT	Supply input/output	Backup battery supply: optional external supply for backup domain when V_{DD} is not present. Can also be used to charge the external battery.
VDDSMPS	Supply input	Supply for switch mode power supply (SMPS) step-down converter.
VLXSMPS	Supply output	SMPS step-down converter output.
VFBSMPS	Supply regulation input	SMPS feedback voltage sense.
VSSSMPS	Supply input	Ground for SMPS step-down converter.
VDDLDO	Supply input	Supply for the integrated low drop out regulator.
VCAP	Supply input/output	Figure 2. System supply configuration shows the different possible regulator supply configurations: using one, both or none. Digital Core supply input / output pin. Is either provided by the embedded regulator or from an external source.(1)
VDD50USB	Supply input	Supply for USB regulator.
VDD33USB	Supply input/output	Embedded USB regulator output or external USB supply when the internal regulator is not used.
VREF+	Supply input/output	Reference voltage for ADCs and DACs. Can be generated through the internal VREFBUF or provided by an external source.
VREF-	Supply input	Ground reference for ADCs and DACs.
PDR_ON	Digital input	Control signal to switch the integrated POR/PDR circuitry ON/OFF.

1. *Refer to Figure 2. System supply configuration for the different possible configurations*

Figure 2. System supply configuration



2.1.1 External power supplies and components

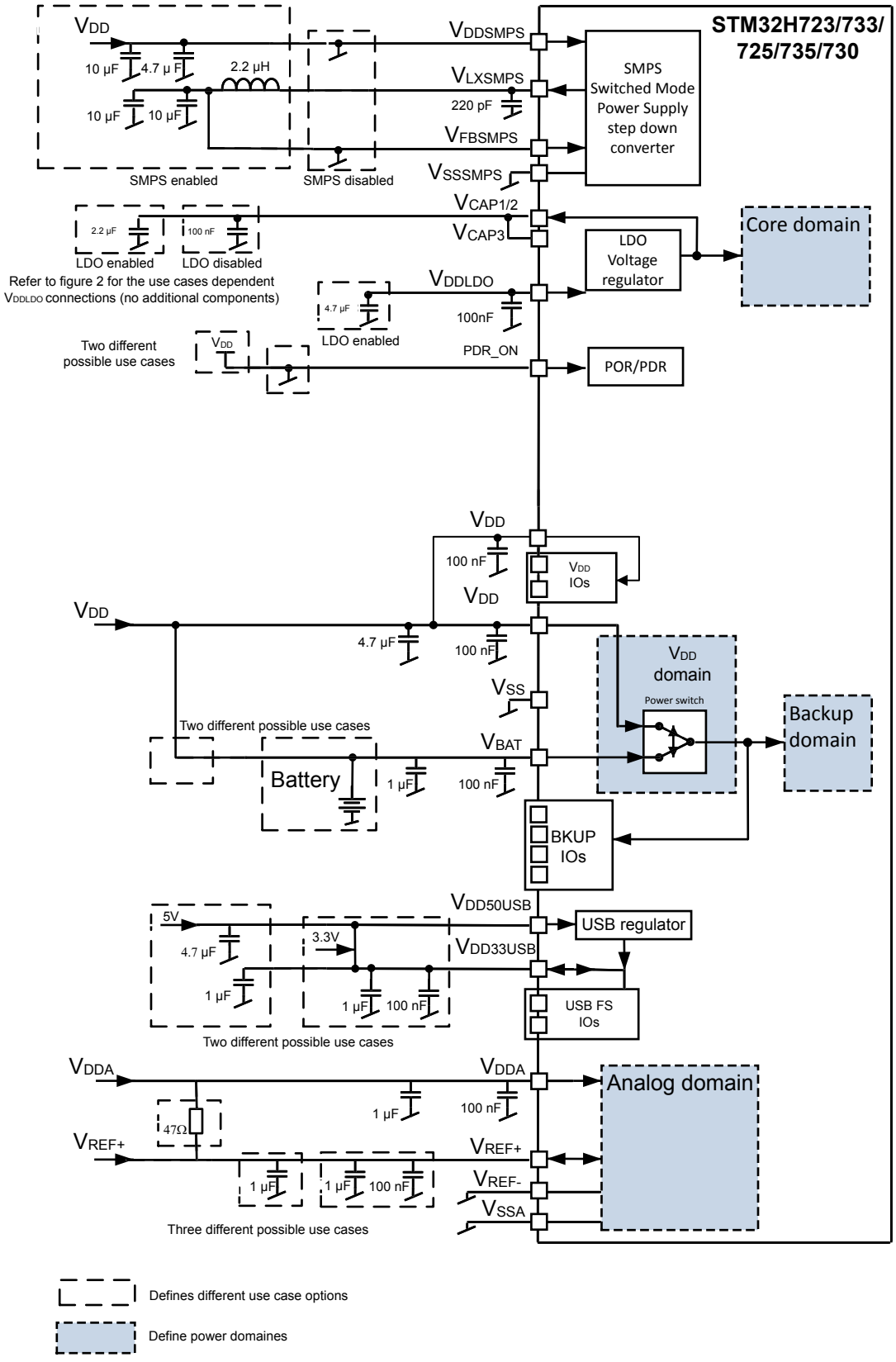
Refer to the *STM32H72x and STM32H73x datasheets* for more details on the electrical characteristics.

Table 2. Power supply connection

Package pin/ ball	Voltage range	External components	Comments
VDD	1.62 to 3.6 V	100 nF ceramic, for each V_{DD} as close as possible of the pins. A 4.7 µF ceramic connected to one of the VDD pin.	For V_{DD} < 1.71 V the PDR must be disabled (see Section 2.2.1 Power-on reset (POR)/power-down reset (PDR))
VDDA	1.62 to 3.6 V	1 µF ceramic and 100 nF as close as possible of the pin	V_{DDA} can be connected to V_{DD} through a ferrite bead.
	1.8 to 3.6 V		Restriction if a DAC or VREFBUF is used.
	2.0 to 3.6 V		Restriction if an OPAMP used.
	0 to 3.6 V		DAC, ADC, OPAMP, COMP, VREFBUF are not used.
VBAT	1.2 to 3.6 V	1 µF ceramic and 100 nF close to the VBAT pin	Can be connected directly to an external battery or supply. The external battery can be charged through the internal 5 kΩ or 1.5 kΩ resistor (see the reference manual *STM32H723/733, STM32H725/735 and STM32H730 advanced Arm®-based 32-bit MCUs* (RM0468). To be connected to V_{DD} when not used. When the PDR_ON pin is set to V_{SS} the VBAT pin must be connected to V_{DD} since this functionality is no longer available.
VDDSMPS	0 V	No capacitor required.	VDDSMPS connected to V_{SS} when the converter is not used.
	1.62 to 3.6 V = V_{DD}	Four different solutions are recommended: • 10 µF (best cost trade-off), ESR 10mΩ • 2x 10 µF (best area/performance trade-off) • 10 µF + 100 nF close from pin (best cost/ performance trade-off) • 10 µF + 4.7 µF (best performance)	For SMPS supplying V_{CORE}.
	2.3 to 3.6 V = V_{DD}		For SMPS output regulated to 1.8 V. The SMPS supplies the LDO regulator or an external regulator.
	3 to 3.6 V = V_{DD}		For SMPS output regulated to 2.5 V. The SMPS supplies the LDO regulator or an external regulator.
VLXSMPS	V_{CORE} or 1.8 V or 2.5 V	When the SMPS is used: • 2.2 µH (DCR 110mΩ, I_{sat} 1.7 A, I_{temp} 1.4 A) as close as possible to V_{LXSMPS}. • LQFP/BGA packages: 220 pF ceramic capacitor on VLXSMPS. • 2x 10 µF (ESR 5 mΩ) close to the inductor on VFBSMPS connection side.	Depending on the use case, the SMPS provides the digital core supply or a supply provided to another regulator (external or internal LDO). See Figure 2. System supply configuration for connection
VFBSMPS	V_{CORE} or 1.8 V or 2.5 V	-	Refer to Figure 2. System supply configuration for the use case dependent of this pin.
VDDLDO	1.62 to 3.6 V	When the LDO is used: 1x 4.7 µF capacitor close to one VDDLDOx pin, all VDDLDOx pins correctly connected together. Otherwise: no capacitor is required. Connect VDDLDOx to VDD.	$V_{DDLDO} \leq V_{DD}$. Up to three VDDLDO pins available depending on the package specification.

Package pin/ ball	Voltage range	External components	Comments
VCAP	VOS0/VOS1/ VOS2/VOS3/ SVOS3/SVOS4/ SVOS5	LDO enabled and SMPS enabled or disabled: 2.2 µF ESR < 100 mΩ for VCAP1 2.2 µF ESR < 100 mΩ for VCAP2 LDO disabled: 100 nF close to each VCAPx pin VCAPx connected together	If the VCAP3 pin is available (depending on the package), it must be connected to the other VCAP pins but no additional capacitance is required. In bypass mode the Vcore supply is externally provided through the VCAPx pins.
VDD50USB	4.0 to 5.5 V	4.7 µF ceramic	Connected to an external supply or USB VBUS for an internal USB regulator use case. Connected to VDD33USB when the internal USB regulator is not used (for packages having this pin available).
VDD33USB	3.0 V to 3.6 V	1 µF ceramic and 100 nF ceramic (USB reg not used) 1 µF max ESR 600 mΩ (USB reg used)	The $V_{DD33USB}$ supply can be provided externally or through the internal USB regulator. When the regulator is enabled its output will be provided directly to the VDD33USB through the internal connection. This pin is internally tied to V_{DD} when it is not present in some specific packages. In consequence, the V_{DD} supply level must be compliant with V_{DD33} if the USB is used for these packages.
	0V to 3.6 V	-	When USB is not used.
VREF+	1.62 V to ≤ V_{DDA}	1 µF ceramic and 100 nF ceramic close to the pin or connected to VDDA through a resistor (typically 47 Ω)	V_{REF+} is provided externally. In some packages, the VREF+ pin is not available (internally connected to V_{DDA}).
	2 V to ≤ V_{DDA}		External V_{REF+} with V_{DDA}>2 V and ADC used.
	VREFBUF reference voltage	1 µF	V_{REF+} is provided by the embedded VREFBUF regulator. Do not activate the internal VREFBUF when V_{REF+} is provided externally
VREF-	V_{SSA}	Tied to VSSA	Only available in some packages Internally tied to V_{SSA} when this pin is not present
PDR_ON	V_{DD} or V_{SS}	Tied to VDD	Power-on reset (POR) and power-down reset (PDR) circuit switched ON Internally tied to V_{DD} when this pin is not present in a specific package. V_{DD}: 1.71 to 3.6 V
		Tied to VSS	POR and PDR circuit switched off V_{DD}: 1.62 to 3.6 V

Figure 3. Power supply component layout



2.1.2 Digital circuit core supply (Vcore)

As shown in Figure 2. System supply configuration, the digital power can be supplied either by the internal linear voltage regulator, the embedded SMPS step-down converter or directly by an external supply voltage (regulator bypass). The SMPS step-down converter can also be cascaded with the linear voltage regulator.

In system Run mode, this digital core voltage can be set dynamically to the required performance (voltage scaling VOS0 to VOS3).

In system Stop mode, the digital core voltage can be reduced to improve the power consumption (voltage scaling SVOS3 to SVOS5).

For a detailed definition on the available power modes please read the power control (PWR) chapter of the reference manual *STM32H723/733, STM32H725/735 and STM32H730 advanced Arm®-based 32-bit MCUs* (RM0468).

2.1.3 Independent analog supply and reference voltage

To improve analog peripheral performance, the analog peripherals feature an independent power supply which can be separately filtered and shielded from noise on the PCB:

- The analog supply voltage input is available on a separate VDDA pin.
- An isolated ground connection is provided on the VSSA pin.

To ensure better ADC and DAC accuracy, the reference voltage can be provided externally through the VREF+ pin, this however is not available in all packages.

The VREF– pin is available on some packages to improve the ground noise immunity.

The V_{DDA} minimum value (V_{DDA_MIN}) depends on the analog peripheral and on whether a reference voltage is provided or not, refer to Table 2. Power supply connection for more details.

2.1.4 Independent USB transceiver power supply

There are different ways to supply the USB transceivers, depending on $V_{DD33USB}$ and $V_{DD50USB}$ availability:

- When the VDD50USB pin is available, it can be used to supply an internal regulator dedicated to the USB transceivers.
- In this case, either the USB VBUS or an external power supply can be used to provide the required voltage.
- The internal regulator output supply is connected to the USB FS PHY and is also available on the VDD33USB pin (see Figure 1. Power supplies).

In this configuration, the $V_{DD50USB}$ voltage can rise either before or after the V_{DD} power supply (see Figure 6. VDD50USB power supply).

An external capacitor must be connected to VDD33USB (see Table 2. Power supply connection).

- When the VDD33USB pin is available, it can be used to supply the internal transceiver. In this case, the VDD33USB pin should receive a voltage ranging between 3.0 to 3.6 V. If the VDD50USB pin is available and the internal USB regulator is not used, $V_{DD50USB}$ must be connected with the VDD33USB pin. As an example, when the device is powered at 1.8 V, an independent 3.3 V power supply can be applied to $V_{DD33USB}$.

When $V_{DD33USB}$ is connected to a separate power supply, it is independent from V_{DD} and V_{DDA}. In this case, it must be the last supply to be turned on and the first supply to be switched off. The following conditions must be respected (see Figure 5. VDD33USB connected to external power supply):

- During the power-on and power-down phases (V_{DD} < V_{DD} minimum value), $V_{DD33USB}$ should always be lower than V_{DD}.
- $V_{DD33USB}$ rising and falling time specifications must be adhered to (refer to table power-up/power-down operating conditions for regulator on and table power-up/power-down operating conditions for regulator off provided in the *STM32H72x and STM32H73x datasheets*).
- In operating mode, $V_{DD33USB}$ can be either lower or higher than V_{DD}:

If a USB interface is used (USB OTG_HS / OTG_FS), the associated GPIOs powered by $V_{DD33USB}$ operate between $V_{DD33USB\_MIN}$ and $V_{DD33USB\_MAX}$(see Figure 5. VDD33USB connected to external power supply).

- On some packages neither the VDD33USB pin, nor the VDD50USB pin are available, it is the VDD pin which supplies the $V_{DD33USB}$ through an internal connection.
- In this case, V_{DD} is constrained by $V_{DD33USB}$ and must range between 3.0V and 3.6V

Figure 4. **VDD33USB connected to V_{DD} power supply**

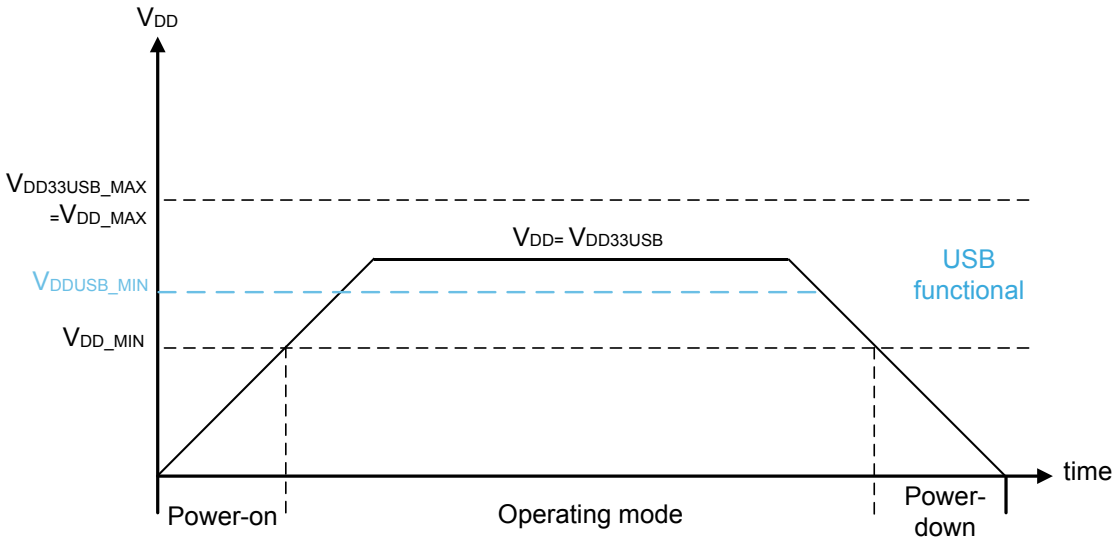


Figure 5. **VDD33USB connected to external power supply**

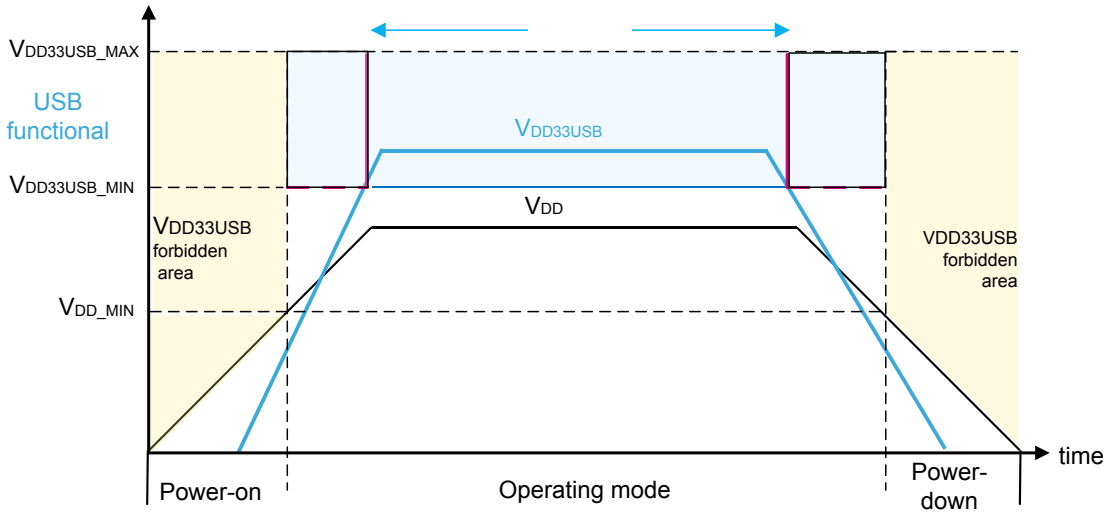
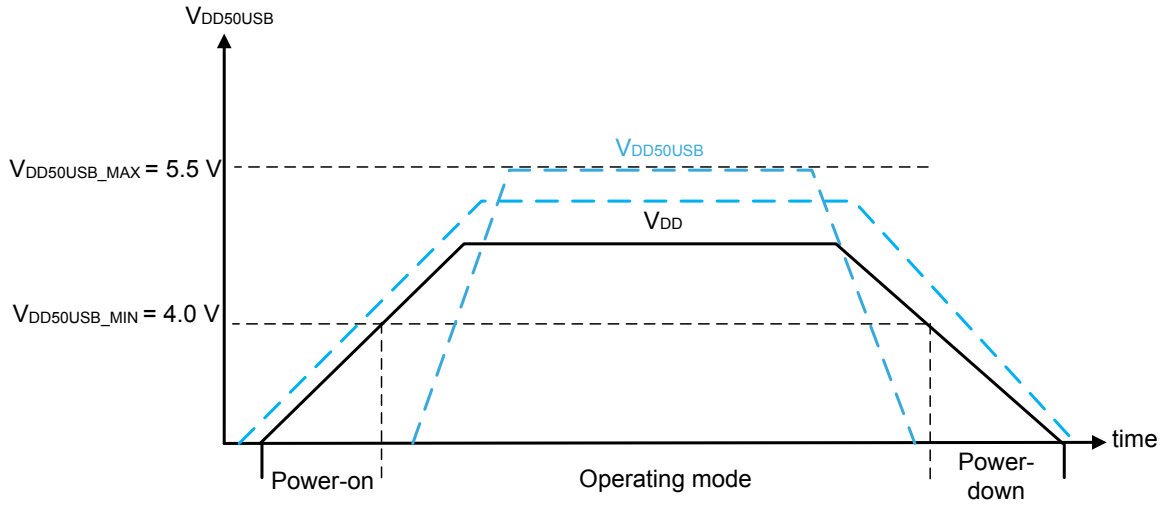


Figure 6. **VDD50USB power supply**



2.1.5 Battery Backup domain

Backup domain description

To retain the content of the RTC Backup registers, Backup SRAM, and supply the RTC when V_{DD} is turned off, the VBAT pin can be connected to an optional 1.2-3.6 V standby voltage supplied by a battery. Otherwise, VBAT must be connected to another source, such as V_{DD}.

When the Backup domain is supplied by V_{BAT} (analog switch connected to V_{BAT} since V_{DD} is not present), the following functions are available:

- PC14 and PC15 can be used for the LSE pins only.
- PC13 can be used as tamper pin (TAMP1).
- PC1 can be used as tamper pin (TAMP3).

During $t_{RSTTEMPO}$ (delay at V_{DD} start-up) or after a Power-Down Reset (PDR) is detected, the power switch between V_{BAT} and V_{DD} remains connected to VBAT.

During the start-up phase, if V_{DD} is established during $t_{RSTTEMPO}$ and is greater than V_{BAT} + 0.6 V, a current may be injected into the VBAT pin through an internal diode connected between V_{DD} and the power switch (V_{BAT}). If the power supply/battery connected to the VBAT pin cannot support this current injection, it is strongly recommended to connect an external low-drop diode between this power supply and the VBAT pin.

Refer to the *STM32H72x/73x datasheets* for the actual value of $t_{RSTTEMPO}$.

Battery charging

When V_{DD} is present, the external battery connected to VBAT can be charged through an internal resistance. This operation can be performed either through an internal 5 kΩ or 1.5 kΩ resistor. The resistor value can be configured by software.

Battery charging is automatically disabled in V_{BAT} mode.

2.1.6 LDO voltage regulator

The low drop out (LDO) voltage regulator is always enabled after Power-on reset. If it is disabled, it remains disabled even after any reset source except for a Power-on reset. For system supply configuration where this regulator is not needed, it will be switched OFF by the user software after system start-up. On some packages, the LDO power supply is available on external VDDLDO pins. When it is not available on an external pin, V_{DDLDO} is connected internally to V_{DD}.

For the configuration where the Vcore is supplied by the LDO, the default output level is set to 1.0V (VOS3). Refer to Figure 2. System supply configuration for more details.

The LDO can be set to one out of four different modes. One mode corresponds to the regulator switched OFF and the three other modes to the regulator switched ON, in which case the mode depends on the application operating modes:

- Switched OFF:
  - The Vcore is supplied externally through the VCAP pin (bypass mode);
  - Or the Vcore is supplied through the SMPS step-down converter (see Section 2.1.7 SMPS step-down converter).
- In Run mode:
  - The LDO regulator supplies the core and the backup domains;
  - The LDO regulator output voltage can be dynamically scaled by programming the voltage scaling (VOS0 to VOS3) depending on the required performance (see the reference manual *STM32H723/733, STM32H725/735 and STM32H730 advanced Arm®-based 32-bit MCUs* (RM0468)).
- In Stop mode
  - The LDO regulator output level is reduced to the state programmed before entering stop mode (SVOS3 to SVOS5). The register and the SRAMs content is kept.
  - For SVOS3, further power reduction can be achieved by setting the regulator in low power deep sleep mode (for SVOS4 and SVOS5 the low power deep sleep mode is set automatically).
- In Standby mode:
  - The regulator is powered down. The registers and SRAM content are lost except for those related to the standby circuitry and the backup domain.

2.1.7 SMPS step-down converter

The embedded switch mode power supply (SMPS) step-down converter has a higher efficiency than the embedded LDO regulator.

By using the SMPS, the overall system power consumption is improved for all power modes at the extra cost of an additional external inductor.

Refer to the *STM32H72x and STM32H73x datasheets* to compare power efficiencies.

See Figure 2. System supply configuration for the possible configurations.

The SMPS step-down converter is always enabled after Power-on reset when its power supply is provided on the VDDSMPS pin. If it is disabled, it remains disabled even after any reset except for Power-on reset.

The regulated output at start-up is 1.36 V.

The three main SMPS configurations are:

- The SMPS is used but the Vcore supply is provided by the internal LDO regulator.

  After start-up the SMPS can be set by software to provide a regulated output of 1.8V or 2.5 V.
- The SMPS is used but the Vcore supply is provided by an external regulator.

  After start-up the SMPS can be set by software to provide a regulated output of 1.8 V or 2.5 V. The external regulator must ensure the correct voltage scaling for the run and stop modes (VOSx and SVOSx).
- The SMPS is directly connected to the VCAP pin and provides the regulated supply to the Vcore.

  In this configuration, the SMPS will run in one of the following modes:
  - Run mode:
    - The converter can be dynamically scaled by programming the voltage scaling (VOS0 to VOS3) to the required performance (see the reference manual *STM32H723/733, STM32H725/735 and STM32H730 advanced Arm®-based 32-bit MCUs* (RM0468)).
  - In Stop mode:
    - The converter output level is reduced to the state programmed before entering stop mode (SVOS3 to SVOS5). The register and SRAM content is kept
    - For SVOS3, a further power reduction can be achieved by setting the converter in low power mode (for SVOS4 and SVOS5 the low-power mode is always set automatically).
  - In Standby mode:
    - The converter is powered down. Both the register and SRAM content is lost except for the content related to the standby circuitry and the backup domain.

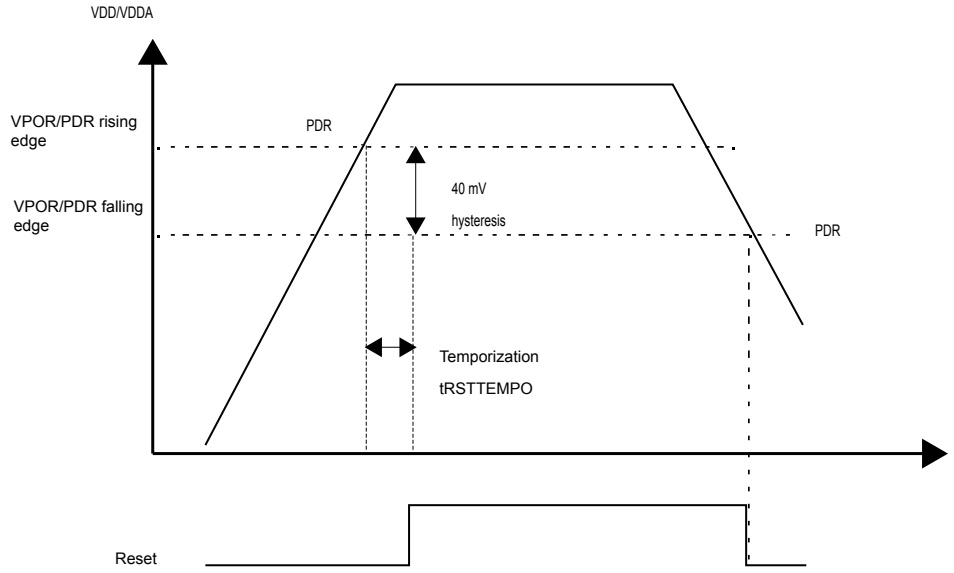
2.2 Reset and power supply supervisor

2.2.1 Power-on reset (POR)/power-down reset (PDR)

The devices have an integrated POR/PDR circuitry which ensures correct operational start-up from 1.71 V.

The device remains in reset mode while V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit as illustrated in Figure 7. Power on reset/power down reset waveform. For more details concerning the POR/PDR threshold, refer to the electrical characteristics of the *STM32H72x and STM32H73x datasheets*.

Figure 7. Power on reset/power down reset waveform



$t_{RSTTEMPO}$ is approximately 377 µs. $V_{POR/PDR}$ rising edge is 1.67 V (typical) and $V_{POR/PDR}$ falling edge is 1.62 V (typical). Refer to the *STM32H72x and STM32H73x datasheets* for the actual values.

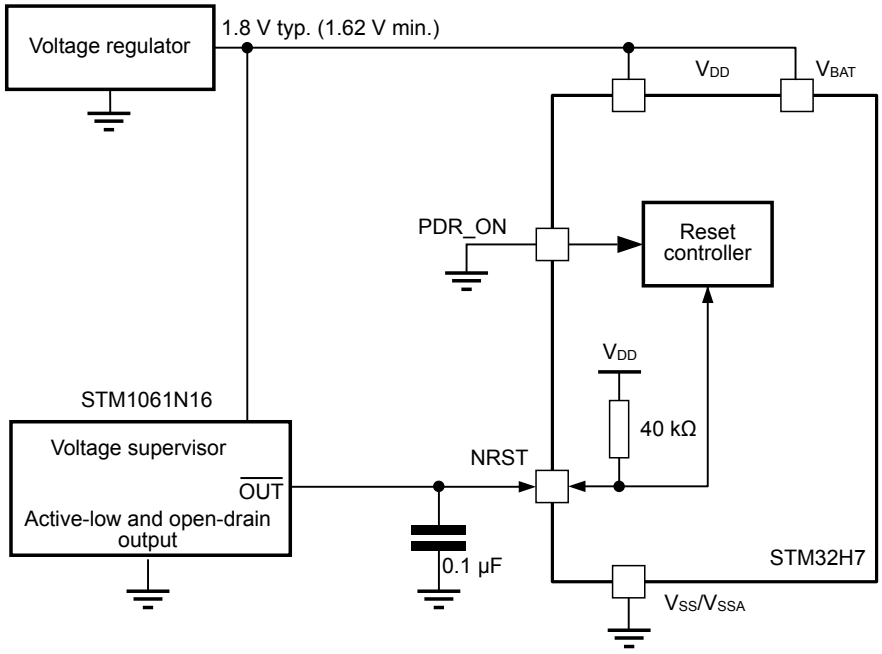
For packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On other packages, the power supply supervisor is always enabled.

The power supply supervisor is switched off by connecting the PDR_ON pin to V_{SS}, required to run the devices at V_{DD} higher than 1.71 V.

In this case, an external power supply supervisor has to monitor V_{DD} and control the NRST pin.

The device must be maintained in reset mode as long as V_{DD} is below 1.62 V. The implemented circuit is illustrated in Figure 8. Power supply supervisor interconnection with internal reset OFF.

Figure 8. Power supply supervisor interconnection with internal reset OFF



The supply ranges which never go below the 1.71 V are managed more effectively using the internal circuitry (no additional components are needed, thanks to the fully embedded reset controller).

When the embedded power supply supervisor is off, the following integrated features are no longer supported:

- The brown out reset (BOR) circuitry must be disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no longer available and VBAT pin must be connected to V_{DD}.

2.2.2 Brownout reset (BOR)

If enabled through the option bytes, the BOR keeps the system under reset until the V_{DD} supply voltage reaches the selected V_{BOR} threshold (also selected through option bytes, see the reference manual *STM32H723/733, STM32H725/735 and STM32H730 advanced Arm®-based 32-bit MCUs* (RM0468))

Three BOR levels are possible (2.1 V, 2.4 V, 2.7 V) (see the *STM32H72x and STM32H73x datasheets* for the electrical characteristics)

2.2.3 Programmable voltage detector (PVD)

The PVD can be used to monitor the V_{DD} power supply by comparing it to a threshold selected by the `PLS[2:0]` bits in the PWR power control register (PWR_CR1).

The PVD is enabled by setting the PVDE bit.

The selectable threshold is between 1.95 V and 2.85 V (see the reference manual *STM32H723/733, STM32H725/735 and STM32H730 advanced Arm®-based 32-bit MCUs* (RM0468)).

A PVDO flag is available in the PWR power control/status register (PWR_CSR1), to indicate if V_{DD} is higher or lower than the PVD threshold. This event is internally connected to the EXTI line16 and can generate an interrupt if enabled through the EXTI registers.

The PVD output interrupt can be generated when V_{DD} drops below the PVD threshold and/or when V_{DD} rises above the PVD threshold depending on EXTI line16 rising/falling edge configuration. As an example, the service routine could perform emergency shutdown tasks.

2.2.4 Analog voltage detector (AVD)

The AVD can be used to monitor V_{DDA} power supply by comparing it to a threshold selected through the ALS[1:0] bits of the PWR power control register (PWR_CR1). The threshold value can be configured to 1.7, 2.1, 2.5 or 2.8 V (refer to the *STM32H72x and STM32H73x datasheets* for the actual values).

The AVD is enabled by setting the AVDEN bit in PWR_CR1 register. An interrupt can be raised when V_{DDA} goes above or below the configured threshold.

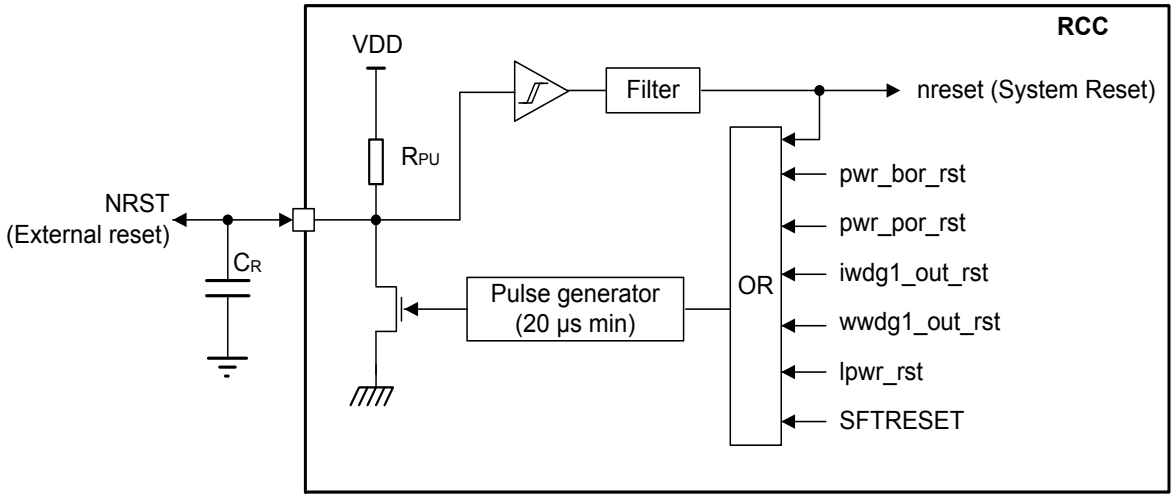
2.2.5 System reset

A system reset sets all the registers to their default values except the reset flags in the clock controller RCC_RSR register and the registers in the backup domain (see Figure 9. Reset circuit).

A system reset is generated when one of the following events occurs:

1. A low level on the NRST pin (external reset)
2. Window watchdog end of count condition (WWDG reset)
3. Independent watchdog end of count condition (IWDG reset)
4. A software reset (Software reset)
5. A low-power management reset.

Figure 9. Reset circuit



2.2.6 Bypass mode

The power management unit is configurable by software with the option to bypass. When bypassed, the core power supply should be provided through VCAPx pins connected together.

In Bypass mode, the internal voltage scaling is not managed internally, and the external voltage value (1.0 to 1.35 V) must be consistent with the targeted maximum frequency (see the *STM32H72x and STM32H73x datasheets* for the actual VOS level).

In Stop mode, it can be lowered to between 0.74 and 1.0 V (see datasheet for the actual SVOS level).

In Standby mode, the external source will be switched off and the V_{CORE} domains powered down. The external source will be switched on when exiting Standby mode.

In Bypass mode, the external voltage must be present before or at the same time as V_{DD}. To avoid conflict with the LDO, the external voltage must be kept above 1.15 V until the LDO is disabled by software.

3 Clocks

3.1 Introduction

The STM32H723/33, STM32H725/35 and STM32H730 microcontrollers support several possible clock sources:

- Two external oscillators (this will require external components):
  - High-speed external oscillator (HSE)
  - Low-speed external oscillator (LSE).
- Four internal oscillators:
  - High speed internal oscillator (HSI)
  - High speed internal 48MHz oscillator (HSI48)
  - Low-power internal oscillator (CSI)
  - Low speed internal oscillator (LSI)
- Three embedded PLLs can be used to generate the high frequency clocks for the system and peripherals.

For both the HSE and LSE, the clock can also be provided from an external source using the OCS_IN and OSC32_IN pins (HSE bypass and LSE bypass modes)

Figure 10. Clock generation and clock tree schematic shows the clock generation and clock tree architecture.

For detail explanation refer to reference manual *STM32H723/733, STM32H725/735 and STM32H730 advanced Arm®-based 32-bit MCUs* (RM0468).

The choice of clocks depends strongly on the application use case .

Refer to the *STM32H72x/ and STM32H73x datasheet* for the electrical characteristics (range and accuracy)

Figure 10. **Clock generation and clock tree**

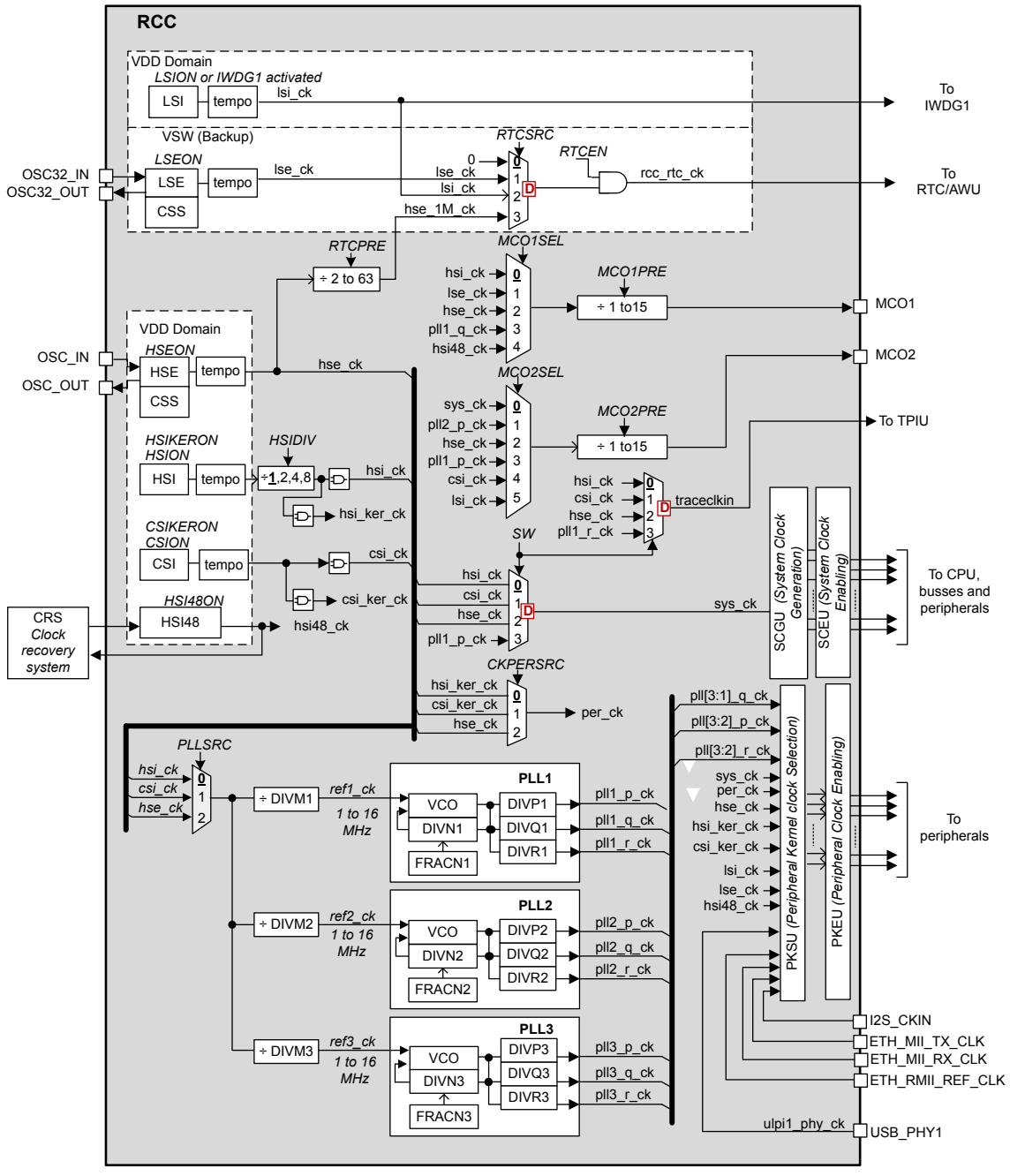


Table 3. **Clock connections**

Pin	External component	Comment
OSC32_IN	External clock input	LSE oscillator LSE bypass input f≤ 1 MHz.

Pin	External component	Comment
OSC32_IN	Typical example[1]: Crystal: 32.768 kHz (6 pF, 50 KΩ) Capacitor: 2x 1.5 pF All components to be placed as close as possible from the pins	LSE oscillator input (see Figure 11. HSE/LSE clock source) .
OSC32_OUT		LSE oscillator output The external cap must be tuned because it is strongly dependent on the PCB design.
	Unconnected in bypass	Not used in bypass mode.
OSC_IN	External clock input	HSE oscillator HSE bypass input 4 MHz ≤ f ≤ 50 MHz.
	Typical example[1]: Crystal: 24 MHz (6 pF, 80 Ω) Capacitor: 2x 33 pF All components to be placed as close as possible from the pins	HSE oscillator input (see Figure 11. HSE/LSE clock source) .
OSC_OUT		HSE oscillator output The external cap must be tuned because it is strongly dependent on the PCB design.
	Unconnected in bypass	Not used in bypass mode.
I2S_CKIN	External clock input	External kernel clock input for audio interface SAI, DFSDM, I2S When an external clock reference is needed.
USB_PHY	External clock input	USB clock provided by the external PHY The embedded PHY supports FS For HS an external PHY needs to be used.
ETH_MII_TX_CLK/ ETH_MII_RX_CLK/ ETH_RMII_REF_CLK	External clock input	Ethernet transmit and receive clock provided from an external Ethernet PHY
MCO1	Internal clock output	Some internal clocks can be provided to MCO1 pin. An embedded divider allows frequency reduction See Figure 10. Clock generation and clock tree.
MCO2	Internal clock output	Some internal clocks can be provided to MCO2 pin. An embedded divider allows frequency reduction See Figure 10. Clock generation and clock tree.
SYNC	External sync signal	Synchronization source for the HSI48MHz embedded oscillator Clock Recovery System (CRS) One of the three possible sync signal, see the reference manual *STM32H723/733, STM32H725/735 and STM32H730 advanced Arm®-based 32-bit MCUs* (RM0468). .

1. *Oscillator design guide for STM8S, STM8A and STM32 microcontrollers application note (AN2867)*

Figure 11. **HSE/LSE clock source**

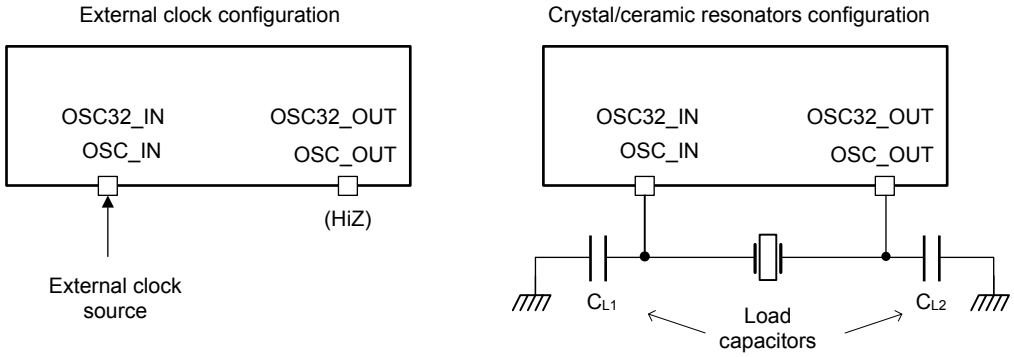


Table 4. **Clock source generation**

Source	Frequency range	External component	Comments
HSE	4 to 50 MHz	Yes	High Speed External clock Used when a very accurate high speed clock is needed.
LSE	32.768 kHz (max 1 MHz)	Yes	Low Speed External clock Used when a very accurate low speed clock is needed. For instance for the real time clock (RTC).
HSI	64 MHz	No	High Speed Internal Clock Default system clock after a reset.
HSI48	48 MHz	No	High Speed Internal 48 MHz clock Kernel clock for some peripherals. High precision clock for USB with Clock Recovery System which can use the USB SOF signal.
CSI	4 MHz	No	Low Power Internal oscillator Faster start-up time than HSI Can be used for wake-up from Stop mode
LSI	32 KHz	No	Low Speed Internal clock, for independent watchdog (IWDG), RTC and auto-wakeup unit (AWU). This clock can run in Stop or Standby modes.
PLL	2 to 16 MHz input	No	Wide-range mode
	1 to 2 MHz input		Low-range mode Some specific frequencies obtained with integer ratio which may be needed for some application (e.g. Audio).
	192 to 836 MHz VCO output		Integer or fractional ratios supported for all PLLs.

To optimize power consumption, each clock source can be switched on or off independently when it is not used.

Refer to the reference manual *STM32H723/733, STM32H725/735 and STM32H730 advanced Arm®-based 32-bit MCUs* (RM0468) for a detailed description of the clock tree. This document provides a complete view of clock usage by peripheral is provided in the Kernel clock distribution overview.

3.1.1 HSE and LSE bypass (external user clock)

In this mode, an external clock source must be provided to OSC_IN/OSC32_IN pins. For LSE bypass, the external source has to be "low swing".The signal (square, sinus or triangle) with ~50% duty cycle drives the OSC_IN/OSC32_IN pin.

3.1.2 External crystal/ceramic resonator (HSE crystal)

The external oscillator has the advantage of producing a very accurate main clock.

Using a 25 MHz oscillator is a good choice for accurate USB OTG high-speed peripheral, I2S and SAI.

The resonator and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize the output distortion and start-up stabilization time. The load capacitance values must be adjusted according to the selected oscillator.

For CL1 and CL2, use high-quality ceramic capacitors in the 5 pF to 25 pF range (typical), designed for high-frequency applications and selected to meet the requirements of the crystal or resonator. CL1 and CL2 are usually the same value. The crystal manufacturer typically specifies a load capacitance that is the series combination of CL1 and CL2. The PCB and MCU pin capacitances must be included when sizing CL1 and CL2 (10 pF can be used as a rough estimate for the combined pin and board capacitance).

The HSERDY flag in the RCC clock control register (RCC_CR) indicates if the high-speed external oscillator is stable or not. At start-up, the clock is not provided until this bit is set by hardware. An interrupt can be generated if enabled in the RCC clock interrupt register (RCC_CIR).

If it is not used as clock source, the HSE oscillator can be switched off using the HSEON bit in the RCC clock control register (RCC_CR).

3.2 LSE oscillator clock

The advantage of using an external oscillator, it provides a low-power highly accurate clock source needed for real-time clock (RTC), clock/calendar and other timing functions.

The LSE crystal oscillator has a configurable driving capability. This capability is chosen according to the external resonator component to insure stable oscillation. It is based on the maximum critical crystal gm provide in the datasheet (refer to *Oscillator design guide for STM8S, STM8A and STM32 microcontrollers application note* (AN2867).

The driving capability is set through the LSEDRV [1:0] in RCC_BDCR register:

- 00: Low drive
- 10: Medium low drive
- 01: Medium high drive
- 11: High drive.

The LSERDY flag in the RCC backup domain control register (RCC_BDCR) indicates whether the LSE crystal is stable or not. At start-up, the LSE crystal output clock signal is not released until this bit is set by hardware. An interrupt can be generated if enabled in the RCC clock interrupt register (RCC_CIER).

The LSE oscillator is switched on and off by programming the `LSEON` bit in RCC backup domain control register (RCC_BDCR).

3.3 Clock security system (CSS)

The device provides two clock security systems (CSS), one for HSE oscillator and one for LSE oscillator. They can be independently enabled by software.

When the clock security system on HSE is enabled, the clock detector is activated after the HSE oscillator start-up delay, and disabled when this oscillator is stopped:

- If the HSE oscillator is used directly or indirectly as the system clock. Indirectly meaning that it is used as PLL input clock, and the PLL clock is the system clock. When failure is detected, the system clock switches to the HSI oscillator and the HSE oscillator is disabled.
- If a failure is detected on the HSE clock, this oscillator is automatically disabled, a clock failure event is sent to the break inputs of the advanced-control timers TIM1, TIM8, TIM15, TIM16, and TIM17 and a non-mask-able interrupt is generated to inform the software of the failure (clock security system interrupt rcc_hsecss_it), allowing the MCU to perform the rescue operations needed. The rcc_hsecss_it is linked to the Arm® Cortex®-M7 NMI (non-maskable interrupt) exception vector.
- If the HSE oscillator clock was used as PLL clock source, the PLL is also disabled when the HSE fails.

The clock security system on LSE must be enabled only when the LSE is enabled and ready, and after the RTC clock has been selected through the RTCSRC[1:0] bits of RCC_BDCR register.

When an LSE failure is detected, the CSS on the LSE wakes the device up from all low-power modes except V_{BAT}. If the failure occurred in V_{BAT} mode, the software can check the failure detection bit when the device is powered on again. In all cases the software can select the best behavior to adopt (including disabling the CSS on LSE which is not automatic).

3.4 Clock recovery system (CRS)

The clock recovery system (CRS) is dedicated to the internal HSI48 RC oscillator.

The CRS is an advanced digital controller acting on the internal fine-granularity trim resulting in a very precise 48 MHz clock.

The CRS is ideally suited to provide a precise clock for the USB peripheral.

The CRS requires a synchronization signal.

Three possible sources are selectable with programmable pre-scaler and polarity:

- SYNC external signal provided through pin;
- LSE oscillator output;
- USB SOF packet reception.

For more details refer to the reference manual *STM32H723/733, STM32H725/735 and STM32H730 advanced Arm®-based 32-bit MCUs* (RM0468).

4 Alternate function mapping to pins

To effectively explore the alternate peripheral function pin mapping refer to the STM32CubeMX tool available on *www.st.com* website.

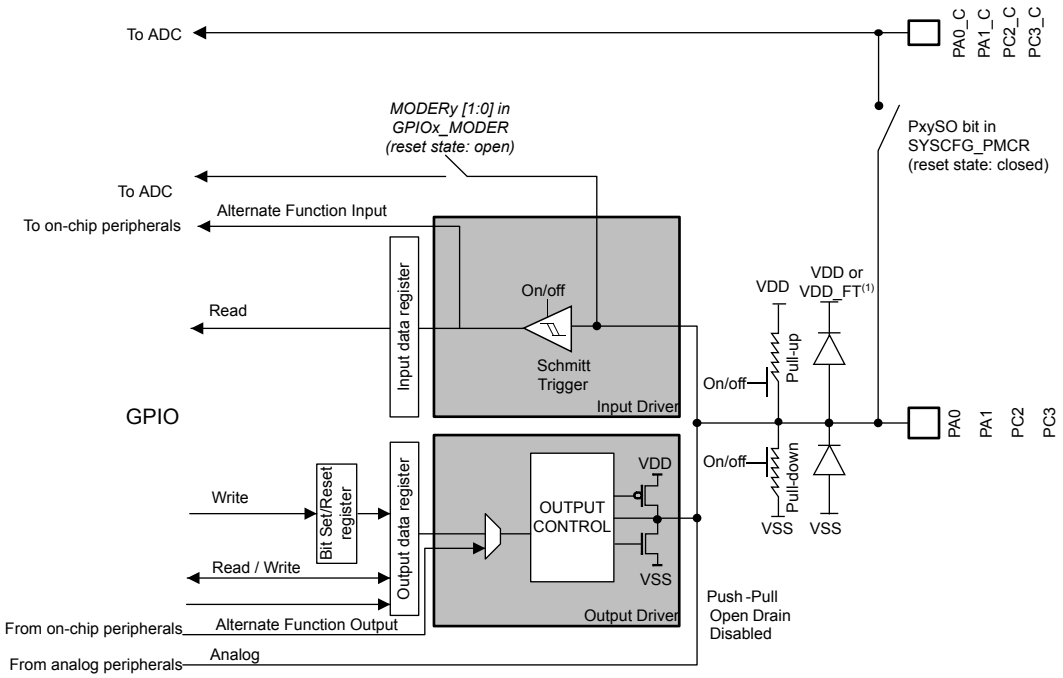
4.1 Analog inputs for ADC1, ADC2 and ADC3

The STM32H723/33, STM32H725/35 and STM32H730 microcontrollers embed four pads with a direct connection to the ADC (PA0_C; PA1_C; PC2_C; PC3_C).

It avoids the parasitic impedances of a conventional pad and thereby enhancing the performance of the ADC.

Figure 12. Analog inputs for ADC1 and ADC2 shows the pad schematic (also available in the reference manual *STM32H723/733, STM32H725/735 and STM32H730 advanced Arm®-based 32-bit MCUs* (RM0468)).

Figure 12. Analog inputs for ADC1 and ADC2



Each ADC has 6 inputs optimized for high performance INP0 to INP5 and INN0 to INN5 (fast channels).Refer to the ADC connectivity figure in the reference manual *STM32H723/733, STM32H725/735 and STM32H730 advanced Arm®-based 32-bit MCUs* (RM0468).

The other 14 channels have lower performance (slow channels)

STM32CubeMX and the table “pin/ball definition” in the *STM32H72x and STM32H73x datasheet* show the availability of the Pxy_C and Pxy depending on the package.

4.1.1 Packages having Pxy_C and Pxy pads available

The Pxy_C pads are routed with a direct connection to the ADC fast input channels.

For these packages, use the Pxy_C inputs for the ADC to get the best performance (see the *STM32H72x and STM32H73x datasheets* ADC characteristic table “Sampling rate for Direct channels”)

The performance of the Pxy standard pads connected to the ADC fast channels are described in the *STM32H72x and STM32H73x datasheets* ADC characteristic table “Sampling rate for Fast channels

The performance of the Pxy standard pads connected to the ADC slow channels are described in the *STM32H72x and STM32H73x datasheets* ADC characteristic table “Sampling rate for Fast channels

4.1.2 Packages having Pxy_C but not the peer Pxy

On some packages, the peer Pxy_C and Pxy is not available, only the Pxy_C are.

As described above these pads give the best performance for the ADC.

To access to all the alternate functions of the conventional pad, the internal switch between the two peer pads needs to be closed (PxySO bit).

In this way all the functionalities of the Pxy pad are available on the Pxy_C pad.

But there is an additional serial impedance due to this switch (300 Ω to 550 Ω) and additional parasitic capacitance (2.5 pF) which may impact timing sensitive signals.

STM32CubeMX and the table “Port A and Port C alternate function” of the *STM32H72x and STM32H73x datasheets* indicate the functions available on the Pxy_C pads by closing the switch between the two pads.

4.1.3 Package having Pxy available but nor the peer Pxy_C

Closing the switch in the pad (GPIOx_MODER bit) connects an ADC slow input to the Pxy pad (See Figure ADC connectivity in the reference manual *STM32H723/733, STM32H725/735 and STM32H730 advanced Arm®-based 32-bit MCUs* (RM0468)). Also refer to the ADC *STM32H72x and STM32H73x datasheets* characteristic table “Sampling rate for Slow channels”.

Another solution is to close the switch between the two peer pads (PxySO bit) instead of closing the switch in the pad. In this way, an ADC fast input is connected to the Pxy pad. The performance is improved but will not however be as high as for a package having a direct input from a Pxy_C pad. (see the *STM32H72x and STM32H73x datasheets* ADC characteristic table “Sampling rate for Medium speed channels”)

5 Boot configuration

5.1 Boot mode selection

In STM32H723/33, STM32H725/35 and STM32H730 microcontrollers, two different boot spaces can be selected through the BOOT pin and the boot base address programmed in the BOOT_ADD0 or BOOT_ADD1 option bytes as shown in the Table 5. Boot modes.

Table 5. Boot modes

Boot mode selection		Boot space
BOOT pin	Boot address option bytes	
0	BOOT_ADD0 [15:0]	Boot address defined by BOOT_ADD0[15:0] user option byte. Default factory programmed value: User Flash memory starting at 0x0800 0000.
1	BOOT_ADD1 [15:0]	Boot address defined by BOOT_ADD1[15:0] user option byte. Default factory programmed value: System Flash memory starting at 0x1FF0 0000.

The BOOT_ADD0 and BOOT_ADD1 address option bytes allow the boot to be programmed to any boot memory address from 0x0000 0000 to 0x3FFF 0000 which includes:

- All the Flash memory address space mapped on the AXIM interface.
- All the RAM address space: ITCM, DTCM RAMs and SRAMs mapped on the AXIM interface.
- The system memory bootloader.

The BOOT_ADD0/BOOT_ADD1 option bytes can be modified after the reset in order to boot from any other boot address after the next reset.

If the programmed boot memory address is out of the memory mapped area or a reserved area, the default boot fetch address is programmed as follows:

- Boot address 0: Flash memory at 0x0800 0000
- Boot address 1: ITCM-RAM at 0x0000 0000

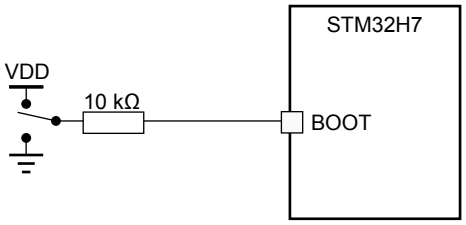
When the Flash level 2 protection is enabled, only boot from Flash memory is available. If the boot address programmed in the BOOT_ADD0 / BOOT_ADD1 option bytes is out of the memory range or belongs to the RAM address range, the default fetch will be forced to the Flash memory at address 0x0800 0000.

Note: When the secure access mode is enabled through option bytes, the boot behavior differs from the above description (refer to section Root secure services of the product reference manual).

5.2 Boot pin connection

Figure 13. Boot mode selection implementation example shows the external connection required to select the boot memory of STM32H723/33, STM32H725/35 and STM32H730 microcontrollers.

Figure 13. Boot mode selection implementation example



Resistor values are given only as a typical example.

5.3 System bootloader mode

The embedded bootloader code is located in the system memory. It is programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces.

Table 6. STM32H723/733, STM32H725/735 and STM32H730 microcontroller bootloader communication peripherals shows the supported communication peripherals by the system bootloader.

Table 6. STM32H723/733, STM32H725/735 and STM32H730 microcontroller bootloader communication peripherals

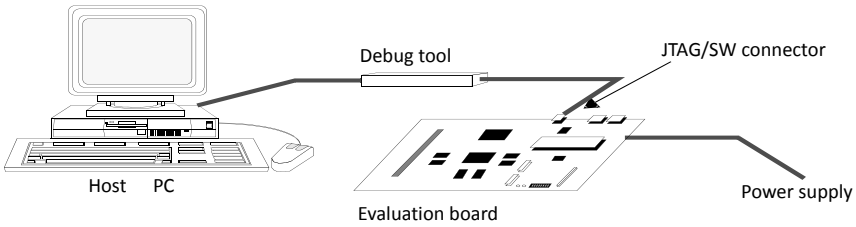
Bootloader peripherals	Bootloader pins
DFU	USB OTG FS (PA11/PA12) in device mode
USART1	PA9/PA10
USART2	PA2/PA3
USART3	PB10/PB11 or PD8/PD9
FDCAN1	PH13/PH14 or PD0/PD1
I2C1	PB6/PB9
I2C2	PF0/PF1
I2C3	PA8/PC9
SPI1	PA4/PA5/PA6/PA7
SPI3	PA15/PC10/PC11/PC12
SPI4	PE11 / PE12 / PE13 / PE14

6 Debug management

6.1 Introduction

The host / target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a JTAG or SW connector and a cable connecting the host to the debug tool. Figure 14. Host to board connection illustrates the connection of the host to the evaluation board.

Figure 14. Host to board connection



6.2 SWJ debug port (serial wire and JTAG)

The core of the STM32H723/33, STM32H725/35 and STM32H730 microcontrollers integrates the serial wire / JTAG debug port (SWJ-DP). It is an Arm® standard CoreSight™ debug port that combines a 5-pin JTAG-DP interface and a 2-pin SW-DP interface.

- The JTAG debug port (JTAG-DP) provides a 5-pin standard JTAG interface to the AHP-AP port.
- The serial wire debug port (SW-DP) provides a 2-pin (clock + data) interface to the AHP-AP port.

In the SWJ-DP, the two SW-DP JTAG pins the are multiplexed with some of the JTAG-DP five JTAG pins.

For more details on the SWJ debug port refer to the reference manual *STM32H723/733, STM32H725/735 and STM32H730 advanced Arm®-based 32-bit MCUs* (RM0468) SWJ debug port section (serial wire and JTAG).

6.2.1 TPIU trace port

The TPIU trace port comprises four data outputs plus one clock output. The number of data outputs can be configured by software and unused signals can be reused as GPIOs. If the trace port is not required, all the signals can be used as GPIOs. By default, the trace port is disabled.

The trace data and clock can operate at up to 133 MHz. As a result, care must be taken with the layout of these signals: the trace connector should be located as close as possible to the microcontroller, while still allowing enough space to attach the trace port analyzer probe.

Refer to Table 7. TPIU trace pins for a summary of trace pins and GPIO assignment.

Table 7. TPIU trace pins

Trace pin name	Type	Description	Pin assignment
TRACED0	Output	Trace synchronous data out 0	PC1 or PE3 or PG13
TRACED1	Output	Trace synchronous data out 1	PC8 or PE4 or PG14
TRACED2	Output	Trace synchronous data out 2	PD2 or PE5
TRACED3	Output	Trace synchronous data out 3	PC12 or PE6
TRACECLK	Output	Trace clock	PE2

6.2.2 External debug trigger

The bidirectional TRGIO signal can be configured as TRGIN or TRGOUT by software. Refer to Table 8. External debug trigger pins for a summary of trigger pins and GPIO assignment.

Table 8. External debug trigger pins

Trigger pin name	Type	Description	Pin assignment
TRGIO	Input/output	Bidirectional external trigger	PC7

6.3 Pinout and debug port pins

STM32H723/33, STM32H725/35 and STM32H730 microcontrollers are available in various packages with differing number of pins. As a result, some functionality is related to the pin availability (TPIU parallel output interface) and will differ between the packages.

6.3.1 SWJ debug port pins

Five pins are used as outputs from the STM32H723/33, STM32H725/35 and STM32H730 microcontrollers for the SWJ-DP as alternate general-purpose I/O functions. These pins are available on all packages and detailed in Table 9. SWJ debug port pins.

Table 9. SWJ debug port pins

SWJ-DP pin name	JTAG debug port		SW debug port		Pin assignment
	Type	Description	Type	Debug assignment	
JTMS/SWDIO	I	JTAG test mode selection	IO	Serial wire data input/output	PA13
JTCK/SWCLK	I	JTAG test clock	I	Serial wire clock	PA14
JTDI	I	JTAG test data input	-	-	PA15
JTDO/TRACESWO	O	JTAG test data output	-	TRACESWO if asynchronous trace is enabled	PB3
NJTRST	I	JTAG test nReset	-	-	PB4

6.3.2 Flexible SWJ-DP pin assignment

After RESET (SYSRESETn or PORESETn), all five pins used for the SWJ-DP are assigned as dedicated pins immediately available to the debugger host (note that the trace outputs are not assigned except if explicitly programmed by the debugger host).

However, the STM32H723/33, STM32H725/35 and STM32H730 microcontrollers offer the possibility of disabling some or all of the SWJ-DP ports and so freeing the associated pins for general-purpose IO (GPIO) usage.

Table 10. Flexible SWJ-DP assignment shows the different possibilities to release some pins.

Table 10. Flexible SWJ-DP assignment

Available debug ports	SWJ IO pin assigned				
	PA13/ JTMS/ SWDIO	PA14/JTCK/SWCLK	PA15/JTDI	PB3/JTDO	PB4/NJTRST
Full SWJ (JTAG-DP + SW-DP) - reset state	X	X	X	X	X
Full SWJ (JTAG-DP + SW-DP) but without NJTRST	X	X	X	X	-
JTAG-DP disabled and SW-DP enabled	X	X	-		
JTAG-DP disabled and SW-DP disabled	Released				

For more details on how to disable SWJ-DP port pins, refer to the *STM32H723/733, STM32H725/735 and STM32H730 advanced Arm®-based 32-bit MCUs* (RM0468) I/O pin alternate function multiplexer and mapping section.

6.3.3 Internal pull-up and pull-down on JTAG pins

The devices embed internal pull-ups and pull-downs to guarantee a correct JTAG behavior. Consequently, the pins are not left floating during reset and they are configured as follows until the user software takes control of them:

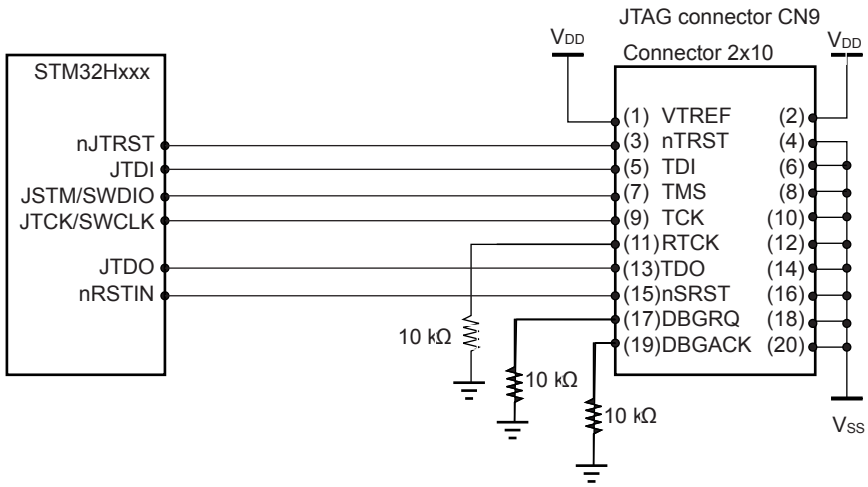
- NJTRST: internal pull-up.
- JTDI: internal pull-up.
- JTMS/SWDIO: internal pull-up.
- JTCK/SWCLK: internal pull-down.
- JTDO: floating state (tristate)

If these I/Os are externally connected to a different voltage, a leakage current will flow during and after reset, until they are reconfigured by software. Special care must be taken with the TCK/SWCLK pin, which is directly connected to some of the clock flip-flops, since it should not toggle before JTAG I/O is released by the user software.

6.3.4 SWJ debug port connection with standard JTAG connector

Figure 15. JTAG connector implementation shows the connection between STM32H723/33, STM32H725/35 and STM32H730 microcontrollers and a standard JTAG connector.

Figure 15. JTAG connector implementation



7 Recommendations

7.1 Printed circuit board

For technical reasons, it is best to use a multilayer printed circuit board (PCB) with a separate layer dedicated to the ground (V_{SS}) and another dedicated to the V_{DD} supply. This provides both good decoupling and good shielding effect. For many applications, cost reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for the ground and the power supply.

7.2 Component position

A preliminary layout of the PCB must separate the different circuits according to their EMI contribution in order to reduce the cross-coupling on the PCB, that is noisy, high-current circuits, low-voltage circuits, and digital components.

7.3 Ground and power supply (V_{SS},V_{DD})

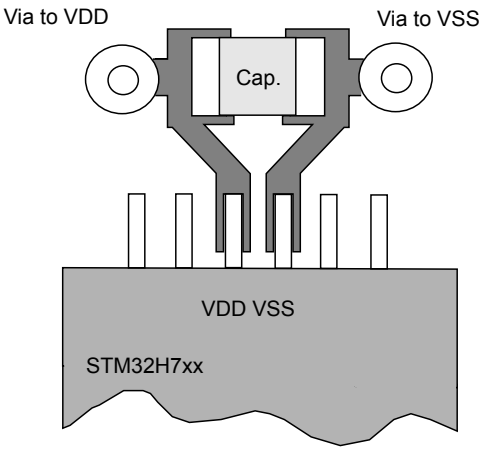
Every block (noisy, low-level sensitive, digital, etc.) should be grounded individually and all ground returns should be to a single point. Loops must be avoided or have a minimum area. The power supply should be implemented close to the ground line to minimize the supply loop area. This is due to the fact that the supply loop acts as an antenna, and therefore will become the EMI main transmitter and receiver. All component-free PCB areas must be filled with additional grounding to create adequate shielding (especially when using single-layer PCBs).

7.4 Decoupling

All the power supply and ground pins must be properly connected to the power supplies. These connections, including pads, tracks and vias should have lowest possible impedance. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair should be decoupled with filtering ceramic capacitors (100 nF) and one single ceramic capacitor (min. 4.7 µF) connected in parallel. These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Typical values are 10 nF to 100 nF, but the exact values depends on the application needs. Figure 16. Typical layout for V_{DD}/V_{SS} pair shows the typical layout of such a V_{DD}/V_{SS} pair.

Figure 16. Typical layout for V_{DD}/V_{SS} pair



7.5 Other signals

When designing an application, the EMC performance can be improved by closely studying:

- Signals for which a temporary disturbance affects the running process permanently (the case of interrupts and handshaking strobe signals, and not the case for LED commands). For these signals, a surrounding ground trace, shorter lengths and the absence of noisy and sensitive traces nearby (crosstalk effect) improve the EMC performance. For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (such as clock).
- Sensitive signals (such as high impedance).

7.6 Unused I/Os and features

All the microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources. To increase the EMC performance, unused clocks, counters or I/Os, should not be left free, e.g. I/Os should be set to 0 or 1 (pull-up or pull-down to the unused I/O pins.) and unused features should be frozen or disabled.

8 Reference design

8.1 Description

The STM32H725G-DK Discovery board and the NUCLEO-H723ZG and NUCLEO-H725ZG Nucleo boards are good references that can be used as a basis for a specific application development.

Details of these boards are available on *www.st.com* website.

9 Recommended PCB routing guidelines for STM32H723/733, STM32H725/735 and STM32H730 microcontrollers

9.1 PCB stack-up

In order to reduce the reflections on high speed signals, the impedance between the source, sink and transmission lines have to be matched. The impedance of a signal trace depends on its geometry and its position with respect to any reference plane.

The trace width and spacing between differential pairs for a specific impedance requirement is dependent on the chosen PCB stack-up. As there are limitations in the minimum trace width and spacing which depend on the type of PCB technology and cost requirements, a PCB stack-up needs to be chosen which addresses all the impedance requirements .

The minimum configuration that can be used is 4 or 6 layers stack-up. An 8 layers boards may be required for a very dense PCBs that have multiple SDRAM/SRAM/NOR/LCD components.

The following stack-ups (Figure 17. Four layer PCB stack-up example and Figure 18. Six layer PCB stack-up example) are intended as examples which can be used as guide lines for a stack-up evaluation and selection. These stack-up configurations place the GND plane adjacent to the power plane to increase the capacitance and reduce the physical gap between GND and the power plane. So high speed signals on the top layer will have a solid GND reference plane which helps reduce the EMC emissions, therefore, moving up in the layers and having a GND reference for each PCB signal layer will further improve the radiated EMC performance.

Figure 17. Four layer PCB stack-up example

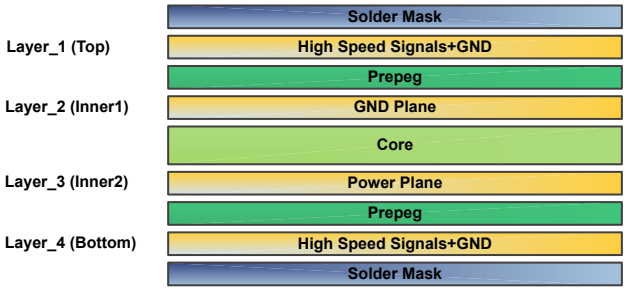
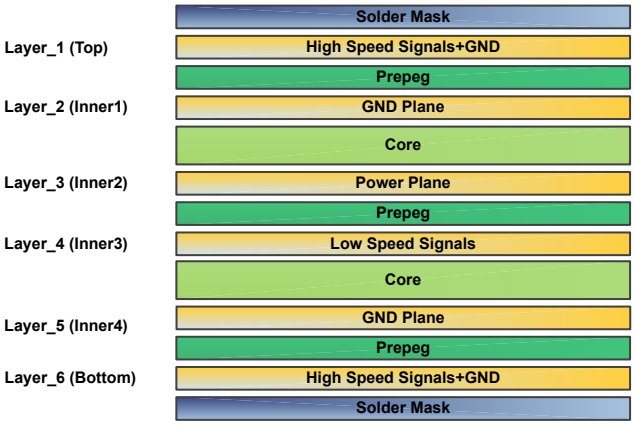


Figure 18. Six layer PCB stack-up example



9.2 Crystal oscillator

Use the application note: *Oscillator design guide for STM8S, STM8A and STM32 microcontrollers* (AN2867), for further guidance on how to layout and route crystal oscillator circuits.

9.3 Power supply decoupling

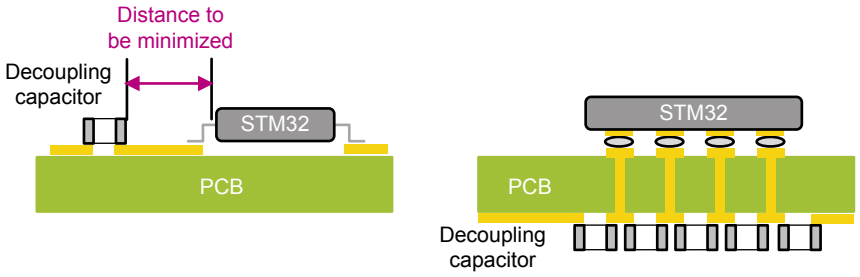
An adequate power decoupling for STM32H723/33, STM32H725/35 and STM32H730 microcontrollers is necessary to prevent excessive power and ground bounce noise. Refer to Section 2 Power supplies.

The following recommendations shall be followed:

- Place the decoupling capacitors as close as possible to the power and ground pins of the MCU. For BGA packages, it is recommended to place the decoupling capacitors on the opposing side of the PCB (see Figure 19. Decoupling capacitor placement depending on package type).
- Add the recommended decoupling capacitors to as many V_{DD}/V_{SS} pairs as possible.
- Connect the decoupling capacitor pad to the power and ground plane with a wide and short trace/via. This reduces the series inductance, maximizes the current flow and minimizes the transient voltage drops from the power plane and in turn reduces the ground bounce occurrence.

Figure 20. Example of decoupling capacitor placed underneath shows an example of decoupling capacitor placement underneath STM32H723/33, STM32H725/35 and STM32H730 microcontroller, closer to the pins and with less vias.

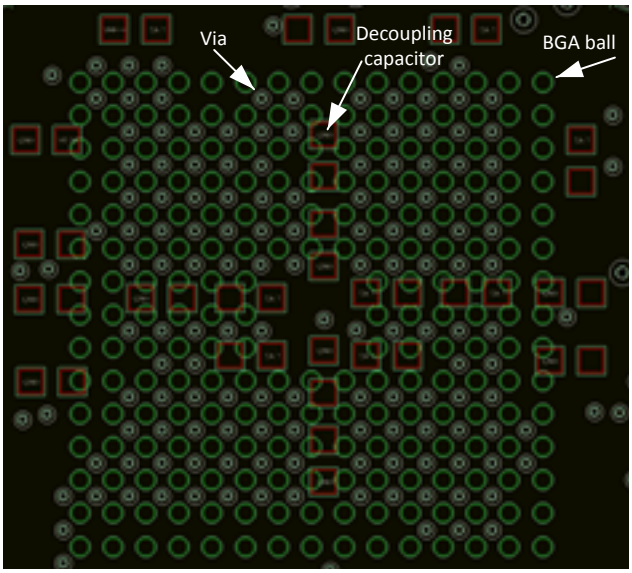
Figure 19. Decoupling capacitor placement depending on package type



Decoupling capacitor and STM32 MCU on the same side of the package (all packages except BGA)

Decoupling capacitor and STM32 MCU on the opposite sides of the package (BGA package)

Figure 20. **Example of decoupling capacitor placed underneath**



9.4 High speed signal layout

9.4.1 SDMMC bus interface

Interface connectivity

The SD/SDIO MMC card host interface (SDMMC) provides an interface between the AHB peripheral bus and Multi Media Cards (MMCs), SD memory cards and SDIO cards. The SDMMC interface is a serial data bus interface, that consists of a clock (CK), command signal (CMD) and 8 data lines (D[0:7]).

Interface signal layout guidelines

- Reference the plane using GND or PWR (if PWR, add 10nf switching cap between PWR and GND).
- Trace impedance: 50 Ω ± 10%.
- All clock and data lines should have equal lengths to minimize any skew.
- The maximum skew between data and clock should be less than 250 ps @ 10mm.
- The maximum trace length should be less than 120 mm. If the signal trace exceeds this trace-length/speed criteria, then a termination should be used.
- The trace capacitance should not exceed 20 pF at 3.3 V and 15 pF at 1.8 V.
- The maximum signal trace inductance should be less than 16 nH.
- Use the recommended pull-up resistance for CMD and data signals to prevent the bus from floating.
- The mismatch within data bus, data and CK or CK and CMD should be below 10mm.
- All data signals must have the same number of vias.

Note: The total capacitance of the SD memory card bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{CARD} of each card connected to this line. The total bus capacitance is $C_L = C_{Host} + C_{Bus} + N*C_{Card}$ where the host is an STM32H723/33, STM32H725/35 and STM32H730 microcontroller, the bus is all the signals and Card is SD card.

Figure 21. microSD card interconnection example and Figure 22. SD card interconnection example show different typical use cases

Figure 21. **microSD card interconnection example**

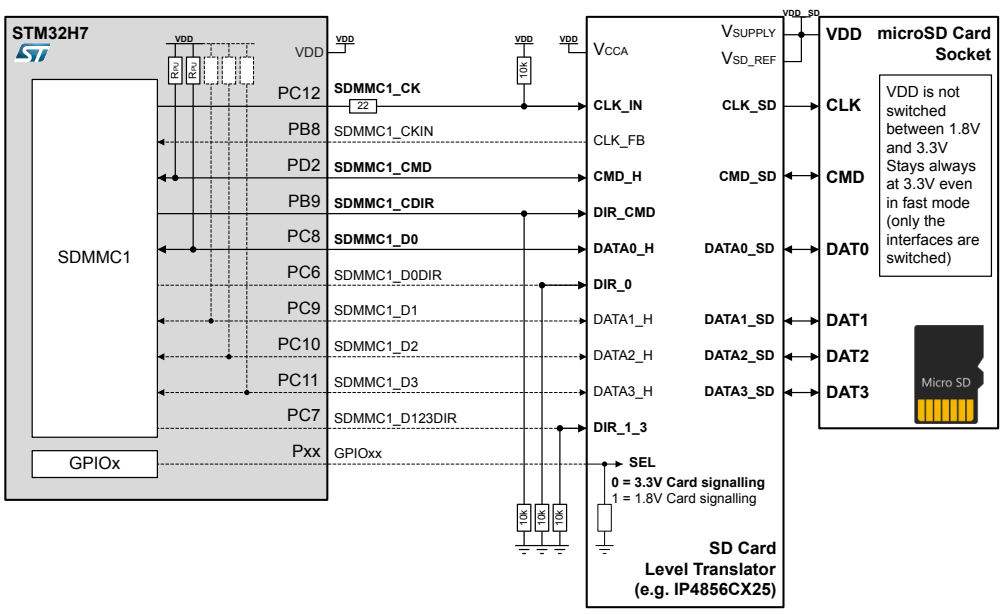
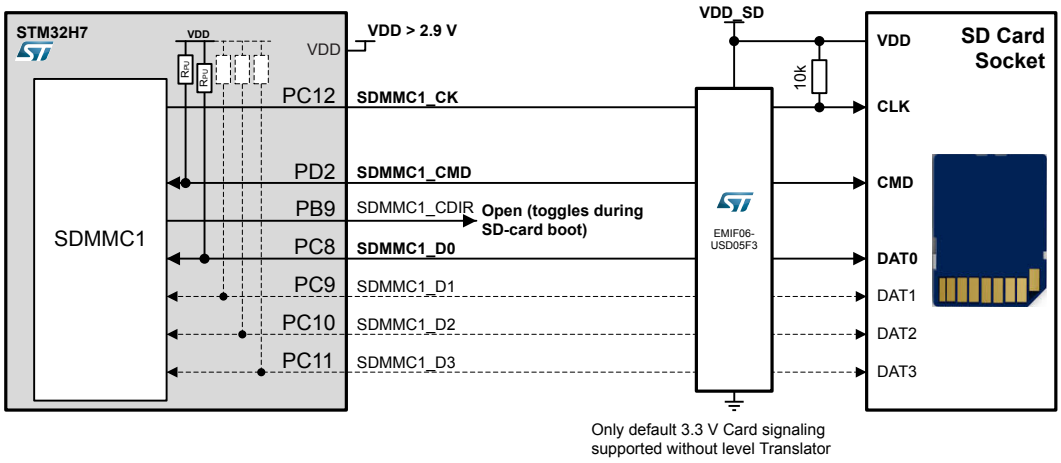


Figure 22. **SD card interconnection example**



9.4.2 Flexible memory controller (FMC) interface

Interface connectivity

The FMC controller and in particular SDRAM memory controller are composed of many signals, most of them have a similar functionality and work together. The controller I/O signals could be split in four groups as follow:

- An address group which consists of row/column address and bank address.
- A command group which includes the row address strobe (NRAS), the column address strobe (NCAS), and the write enable (SDWE).
- A control group which includes a chip select bank1 and bank2 (SDNE0/1), a clock enable bank1 and bank2 (SDCKE0/1), and an output byte mask for the write access (DQM).

- A data group/lane which contains 8 signals.

Note: It depends of the memory specification: SDRAM with x8 bus widths have only one data group, while x16 bus-width SDRAM have two lanes.

Interface signal layout guidelines

- For reference the plane using GND or PWR (if PWR), add 10 nf stitching cap between PWR and GND.
- Trace impedance: 50 Ω ± 10%.
- The maximum trace length should not exceed 120mm. If the signal trace exceeds this trace-length / speed criteria, then a termination should be used.
- To reduce the crosstalk, it is strongly recommended to place data tracks on the different layers to the address and control lanes. However, when the data and address / control tracks coexist on the same layer they must be separated from each other by at least 5 mm.
- Match the trace lengths for the data group within ± 10 mm of each other to reduce any excessive skew. Serpentine traces (this is an “S” pattern to increase trace length) can be used to match the lengths.
- Placing the clock (SDCLK) signal on an internal layer, minimizes the noise (EMI). Route the clock signal at least three times the width of the trace away from others signals. To avoid unnecessary impedance changes and reflection, avoid the use of vias as much as possible. Serpentine routing is to be avoided also.
- Match the clock traces to the data/address group traces length to within ±10 mm.
- Match the clock traces length to each signal trace in the address and command groups to within ±10 mm (with maximum of ≤ 20 mm).
- Trace capacitances:
  - At 3.3 V keep the trace capacitance within 20 pF with overall capacitive loading (including Data, Address, SDCLK and Control) no more than 30 pF.
  - At 1.8 V keep the trace capacitance within 15 pF with overall capacitive loading (including Data, Address, SDCLK and Control) no more than 20 pF.

9.4.3 Octo-SPI interface

Interface connectivity

The Octo-SPI is a specialized communication interface targeting single, dual, quad and octal communication. (Refer to the reference manual *STM32H723/733, STM32H725/735 and STM32H730 advanced Arm®-based 32-bit MCUs* (RM0468)) for details)

Refer to the *STM32H72x and STM32H73x datasheets* for the full electrical characteristic.

Interface signal layout guidelines

- Reference the plane using GND or PWR (if PWR, add 10nf stitching cap between PWR and GND
- Trace impedance: 50 Ω for single-ended and 100 Ω for differential pairs (CLK/NCLK)
- The maximum trace length should be less than120 mm. If the signal trace exceeds this trace-length/speed criterion, then a termination should be used
- Avoid using multiple signal layers for the data signal routing.
- Route the clock signal at least three times the width of the trace away from other signals. To avoid unnecessary impedance changes and reflection, avoid the use of vias as much as possible. Serpentine routing is to be avoided also.
- Match the trace lengths for the data group within ± 10 mm of each other to reduce any excessive skew. Serpentine traces (this is an “S” shape pattern to increase trace length) can be used to match the lengths.
- Avoid using a serpentine routing for the clock signal and use via(s) as little as possible for the whole path. A via alters the impedance and adds a reflection to the signal.
- Avoid discontinuities on high speed traces (vias, SMD components).

Figure 23. Octo-SPI interconnection example and Figure 24. Octo-SPI multiplexed interconnection example illustrate possible interconnection examples.

If SMD components are needed, place these components symmetrically to ensure good signal quality.

Figure 23. **Octo-SPI interconnection example**

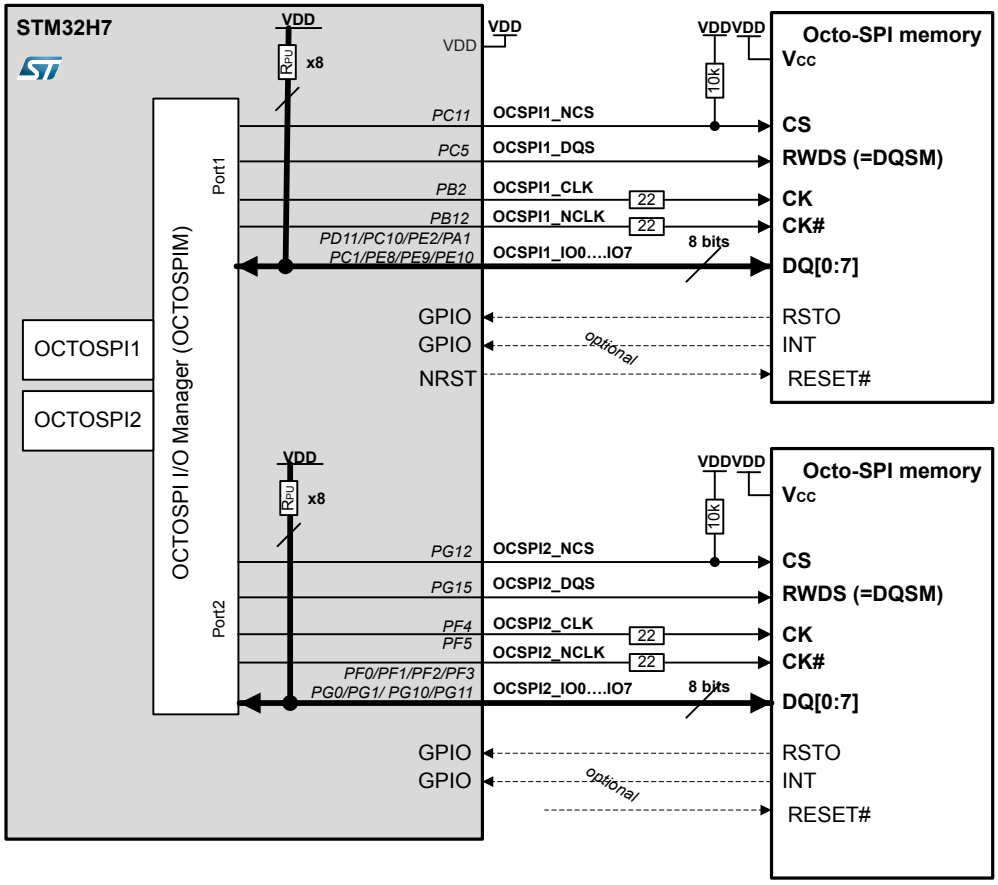
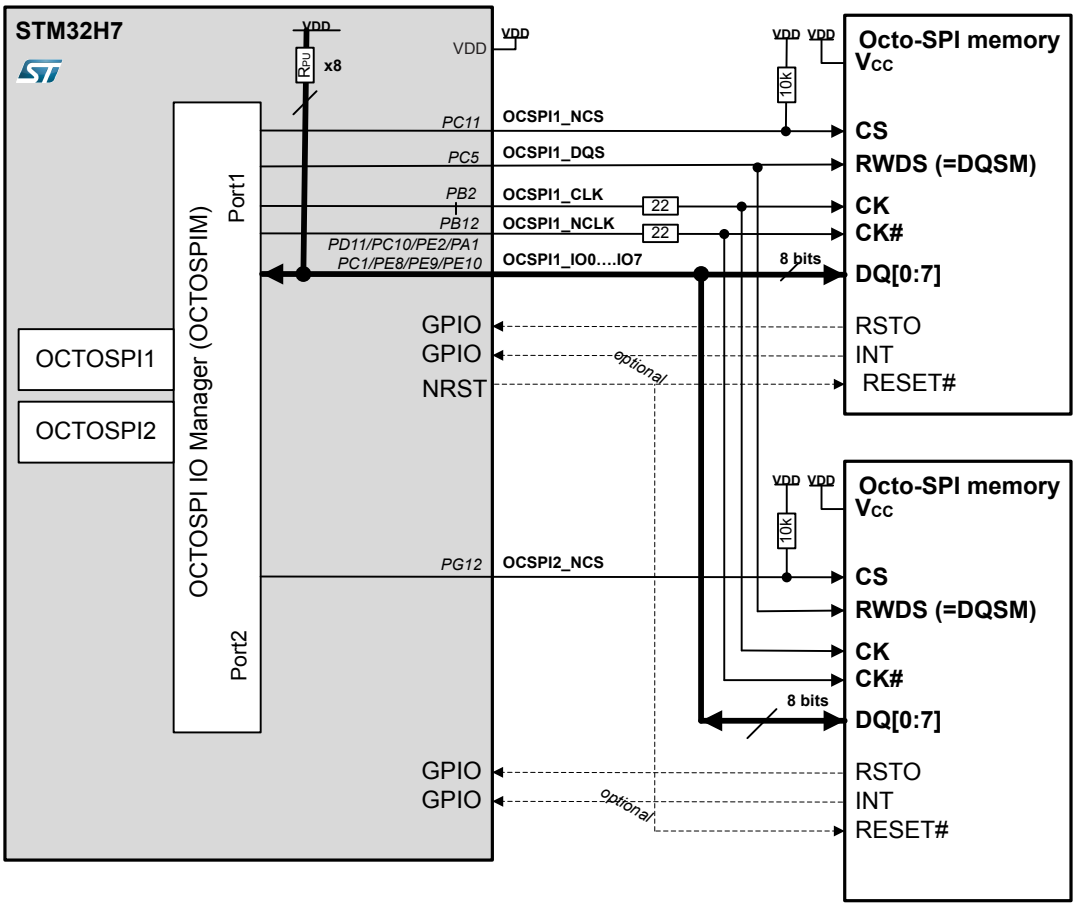


Figure 24. **Octo-SPI multiplexed interconnection example**



In multiplexed mode, the same bus can be shared between two external Octo-SPI memories.

The multiplexed mode must be configured to avoid unwanted transactions when the OCTOSPIs are disabled.

The multiplexed mode can be very useful for some packages where the port2 is not mapped.

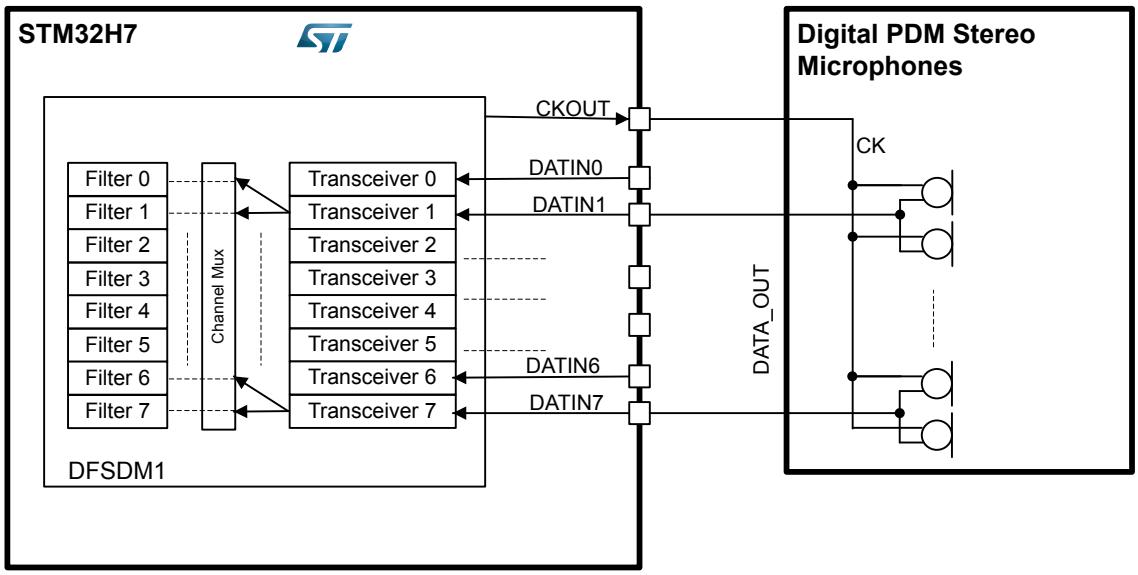
9.4.4 DFSDM interface

The digital filter for the sigma delta modulator (DFSDM) is dedicated to the external sigma-delta modulator's interface (refer to the reference manual *STM32H723/733, STM32H725/735 and STM32H730 advanced Arm®-based 32-bit MCUs* (RM0468) for details). It can, for instance, handle data stream issued from sensors or pulse density modulation (PDM) microphones.

The DFSDM embedded in STM32H723/33, STM32H725/35 and STM32H730 devices is composed of eight filters (see reference manual *STM32H723/733, STM32H725/735 advanced and STM32H730 Arm®-based 32-bit MCUs* (RM0468))

Figure 25. Stereo microphone interconnection shows an example of a stereo microphone interconnection.

Figure 25. **Stereo microphone interconnection**



This example can be transposed to other kinds of external sensors.

9.4.5 Embedded trace macrocell (ETM)

Interface connectivity

The ETM enables the reconstruction of the program execution. The data is traced using the data watchpoint and trace (DWT) component or the instruction trace macrocell (ITM) whereas instructions are traced using the embedded trace macrocell (ETM). The ETM interface is synchronous with the four data bus lines D[0:3] and the clock signal CLK.

Interface signals layout guidelines

- Reference the plane using GND or PWR (if PWR, add 10 nf stitching capacitor between PWR and GND
- Trace impedance: 50 Ω ± 10%
- All the data trace should be as short as possible (≤25 mm),
- Trace the lines which should run on the same layer with a solid ground plane underneath it without vias.
- Trace the clock which should have only point-to-point connection. Any stubs should be avoided.
- It is strongly recommended also for other (data) lines to be point-to-point only. If any stubs are needed, they should be as short as possible. If long stubs are required, there should be a possibility to optionally disconnect them (e.g. by jumpers).

10 Use case examples

STM32CubeMX must be used to determine the most appropriate package for a given use case.

Table 11. Use case examples gives some typical use case examples. It defines the package which supports a specific use case and identifies the peripherals that are available. All the examples below are also supported on larger packages.

Table 11. Use case examples

Package	Use Case	Peripheral	Comment
LQFP100 (no SMPS)	Display and µSD	LCD	RGB TFT Display 8/8/8
		I2C	Communication interface
		SDMMC2	µSD
		GPIO	SD card detection
		USB-FS	-
		USART3	Communication interface
		SPI3	Communication interface
		GPIO	remaining GPIO available
LQFP100 (no SMPS)	Display and OCTOSPI	LCD	RGB TFT display 8/8/8
		I2C1	Touch screen or communication interface
		OCTOSPIM_P1	External memory
		USART2	Communication interface
		SPI1	Communication interface
		USB-FS	-
		GPIO	Remaining GPIO available
LQFP100 (no SMPS)	Audio beam forming and VAD Display External memory or wifi module	FMC	Memory interface used to drive a display (up to 16 bit parallel)
		I2C4	Touch screen or communication interface
		DFSDM2	Digital microphone interface for voice activity detection (VAD), shared with DFSDM1 (see section ...)
		DFSDM1	Digital microphone interface (up to 8) Beam forming
		SDMMC	To interface WIFI module or memory
		SPI1	Communication interface
		USB-FS	-
LQFP100	Camera, Display and µSD	FMC	Memory interface used to drive a display (up to 14 bit parallel)
		I2C2	Touch screen or communication interface
		DCMI	14 bit parallel camera interface
		USB-FS	-
		SDMMC2	µSD (four bit mode)
		GPIO	µSD detection

11 Conclusion

This application note must be used as reference when starting a new design with an STM32H723/33, STM32H725/35 and STM32H730 microcontroller.

Revision history

Table 12. **Document revision history**

Date	Version	Changes
13-Nov-2019	1	Initial release.
20-May-2020	2	Changed document classification to public. Added STM32H730 Value Line. Updated external components for VLXSMPS and VDDLDO in Table 2. Power supply connection and updated values of external capacitors connected to VLXSMPS in Figure 3. Power supply component layout. Only one additional external inductor required to improve the overall system power consumption with SMPS in Section 2.1.7 SMPS step-down converter. Updated Section 2.2.1 Power-on reset (POR)/power-down reset (PDR). Updated external voltage range in Section 2.2.6 Bypass mode. Updated HIS frequency in Table 4. Clock source generation.

Contents

List of tables

List of figures