Application note

The STPMIC1 PCB layout guidelines

Introduction

This application note aims at providing some information about how to place the STPMIC1 on a 4-layer PCB, by paying attention to routing tracks and the switching part with high current path.

Therefore, the correct PCB routing as well as the component placement are key factors in highly integrated power management, and the following topics have to be taken into account:

- High frequency switching currents due to intrinsic behaviour of inductor-based DC/DC conversion
- Signal integrity of the digital interface
- Thermal management of dissipated power

An example of the complete PCB design is also provided and it can be used as reference for custom uses of the STPMIC1 in final applications.

1 Power section layout considerations

The correct PCB layout is extremely important for designs of switching power supply due to high switching currents and sensitive control signals in the surronding area. Increased power losses, output ripple, EMI emissions and the inaccurate regulation are direct consequences of an improper layout of the power section of any DC/DC converter. Less common effects are: induced noise on digital lines, loop instability and audible acoustic noise from passive components. In rare cases, stray inductance of long traces may cause abnormal voltage spikes which, in turn, may stress the STPMIC1 above its maximum voltage ratings (AMR). In the following sections, the rootcause of the critical current paths and some recommendations about how to limit their effects on the STPMIC1 performance are provided.

1.1 General recommendations

- Always consider and determine where and how the return currents flow
- As in all switching DC/DC converter configurations, the minimum length of critical traces is a key-factor as well as the use of ground and power planes
- Reduce the use of vias along the critical current paths
- Route analog signals in the analog section of the board only
- Do not route analog signals (voltage feedback signal) over ground plane gaps
- In case ground or power plane must be split (mechanical and or electrical reasons), do not place any trace across the gap on an adjacent layer
- Never underestimate the importance of decoupling capacitors. Decoupling is the process of placing a capacitor as close as possible to the STPMIC1 to provide the transient switching current. In a DC/DC converter, it is the process of placing an L-C network near the STPMIC1 to minimize the trace inductances causing overvoltage spikes. If they exceed the value of AMR, the device may be damaged
- A high capacity value of the decoupling capacitors is important for low-frequency decoupling effectiveness, but it is less important at high frequencies, where the most important rule is to reduce the stray inductance in series with the decoupling capacitors
- All passive components should be placed as close as possible to the STPMIC1 pins, but when this device packs many regulators in a small area, this can be difficult. A criterion for the passive components placement is to manage their distance from the STPMIC1 by following these priorities, the highest being the shortest distance:
  1. Input capacitors of each Buck converter and output capacitor of the Boost converter
  2. Input capacitors for each LDO and device power supply (VIN, INTLDO…)
  3. Inductors for each DC/DC converter
  4. Output capacitors of each Buck converter and input capacitor of the Boost converter
  5. Output capacitors for each LDO regulators
- Grouping and orientation of capacitors should be occur so that the input capacitor and output capacitor of each DC/DC have their ground side very close to each other, immediately returned to the ground plane and relatively far from the other DC/DC and LDO capacitor ground returns
- The positive side of the output capacitor must be placed as close as possible to the inductor, and from its connection point the voltage feedback trace should start toward VOUT pin

1.2 Buck converter critical current paths

Figure 1. Buck converter schematic (charging phase) and Figure 2. Buck converter schematic (discharging phase) show the simplified schematic of a buck converter, where in green/orange the critical paths of switching current during inductor charging/discharging phase are shown.

Figure 1. Buck converter schematic (charging phase)

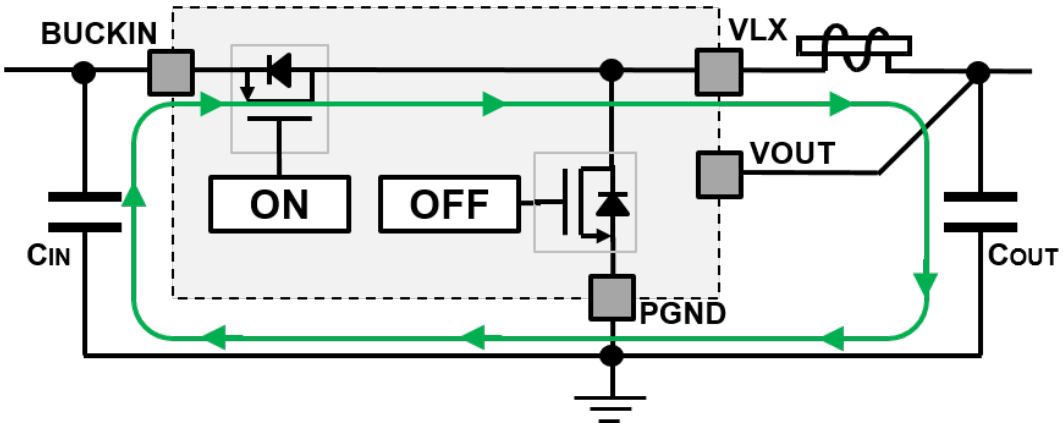
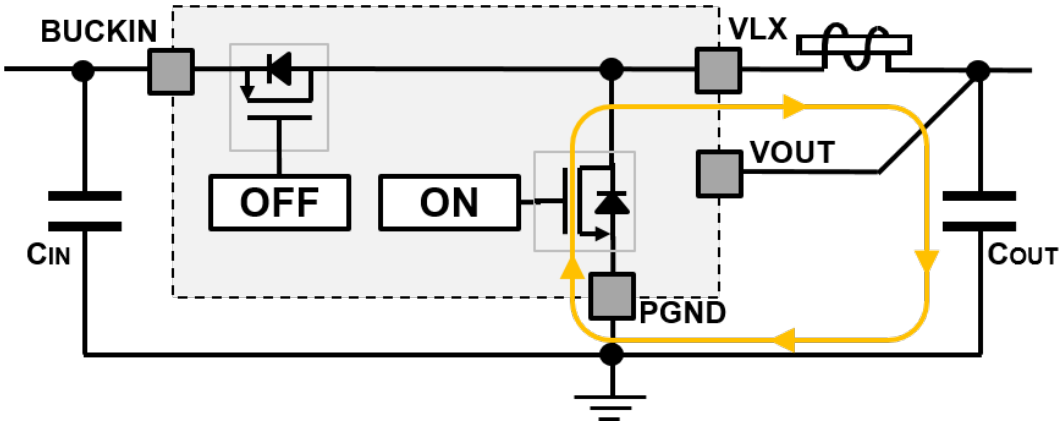


Figure 2. Buck converter schematic (discharging phase)



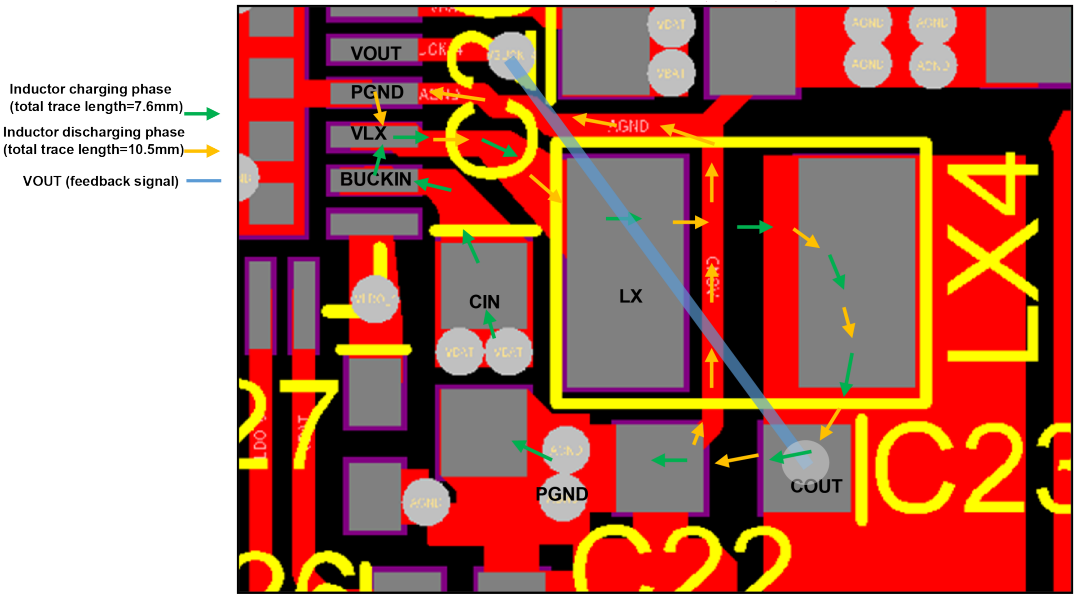
The capacitors and inductors should be placed as close as possible to the STPMIC1 and routed with both wide and short traces. The input capacitor is the most critical component to be placed in the PCB layout. It must be placed as close as possible to the BUCKIN pin and the related PGND pin, to minimize GND loop. If properly routed, the input capacitor cuts the high voltage spikes produced by the switching activity of the device.

Place the output capacitor close to the inductor. It is recommended to connect at a single common point or immediately connect to the ground plane using the appropriate number of vias:

- the ground side of the output capacitor
- the ground side of the input capacitor
- PGND pin of the device

The output voltage feedback signal should be picked exactly on the output capacitor and routed to VOUT pin (feedback signal) avoiding noisy nets. To minimise noise pick-up, its trace should be tiny, placed away from any switching trace, better if routed in a separate layer, shielded from switching lines by the ground plane as shown in Figure 3. Buck reference routing with critical paths where the track for the feedback signal is in the bottom layer (light blue trace).

Figure 3. **Buck reference routing with critical paths**



1.3 Boost converter critical current paths

Figure 4. Boost converter schematic (charging phase) and Figure 5. Boost converter schematic (discharging phase) show the simplified schematic of a boost converter, where in green/orange, the critical paths of switching current during inductor charging/discharging phase, are shown.

Figure 4. Boost converter schematic (charging phase)

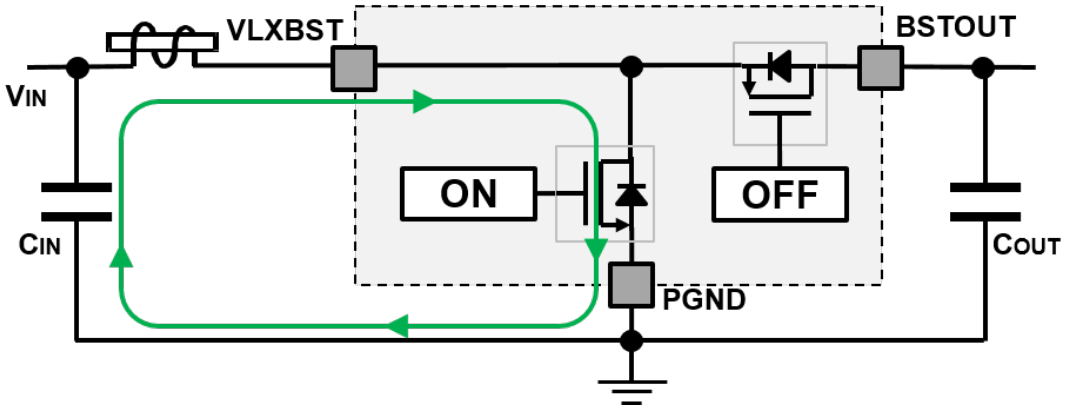
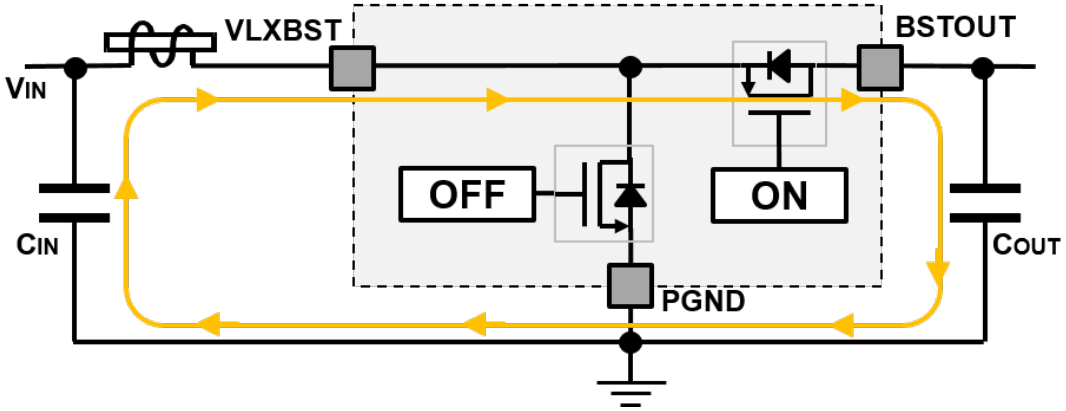


Figure 5. Boost converter schematic (discharging phase)



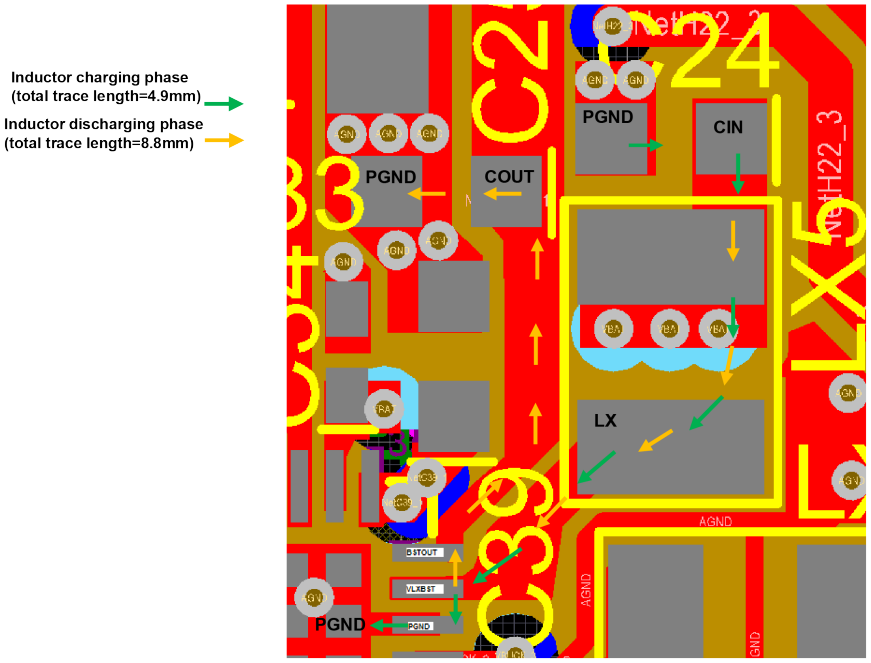
The track at the VLXBST node should be optimized to handle the large current by keeping a minimum area, because this is the noisiest node of the boost converter. Take care of any trace of a nearby sensitive node, such as the feedback signal of a buck converter, which should be kept off from the VLXBST node.

The output capacitor location is very important, because BSTOUT pin is also the feedback point of the boost regulation loop, so it should be placed close to the device and routed with a short and wide trace to minimize the parasitic inductance.

The ground side of the input capacitor should be shortly routed to the STPMIC1 power ground pin (PGND) and to the ground plane. Keep a short distance between VIN side of the input capacitor and the inductor, to guarantee a stable and clean voltage along VIN, despite the high current ripple caused by the switching activity.

Figure 6. Boost reference routing with critical paths shows the PCB layout of the boost converter section of the STEVAL-PMIC1x

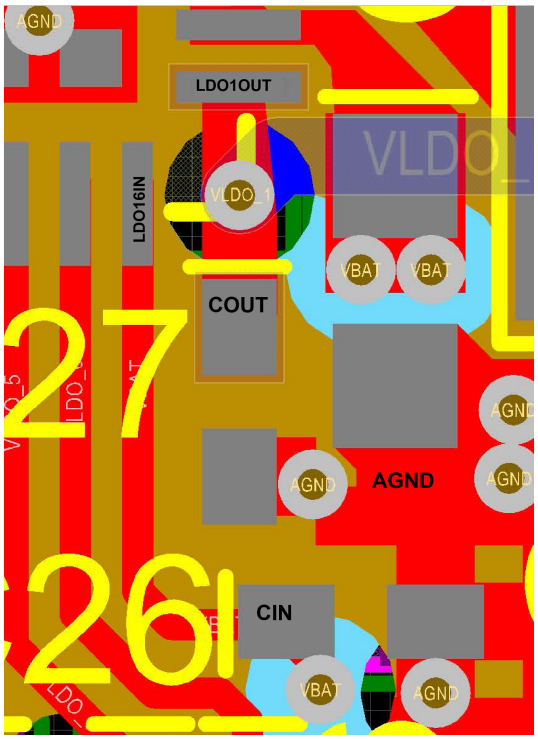
Figure 6. Boost reference routing with critical paths



1.4 LDOs

LDOs are not affected by the switching noise activity by itself, but since they are physically very close to the active buck and boost converters, the injected noise can be a problem. For this reason, each LDO supply should be filtered by a decoupling capacitor placed as close as possible to the input pin of the related LDO. Besides, to assure the best performance, the output capacitor should be placed close to the LDO output, possibly with its ground side far from any switching ground return, to avoid any noise injection.

Figure 7. LDO reference routing



2 Thermal considerations

The package of the STPMIC1 is the WFQFN 5x6x0.8 mm with an exposed pad (ePad), which helps the thermal power dissipation of the device. In the PCB, thermal vias carry the heat away from the IC and are typically arranged in array of about a dozen. It is strongly suggested to put a minimum of 9 via holes (ground-fill) underneath the ePad of the device, since the PCB acts as a heat-sink by mainly using the ground plane for the improved thermal power dissipation.

The exposed pad solder area can be segmented into a symmetric pad array, as shown in Figure 8. Exposed pad solder stencil and Figure 9. Vias placement suggestion, applying the solder paste to approximately 50% to 75% of the area of the exposed pad.

Figure 8. Exposed pad solder stencil

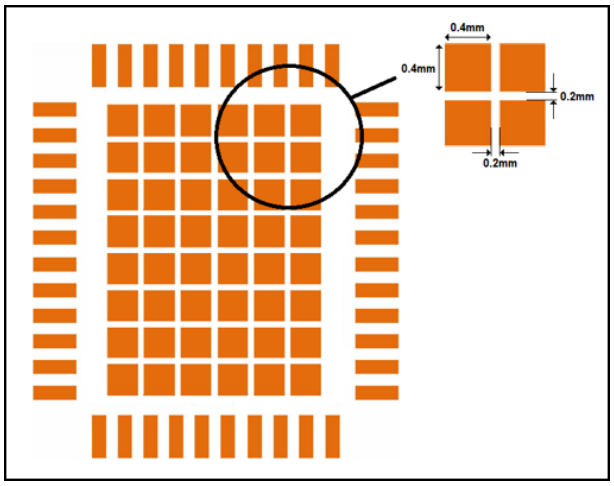


Figure 9. Vias placement suggestion

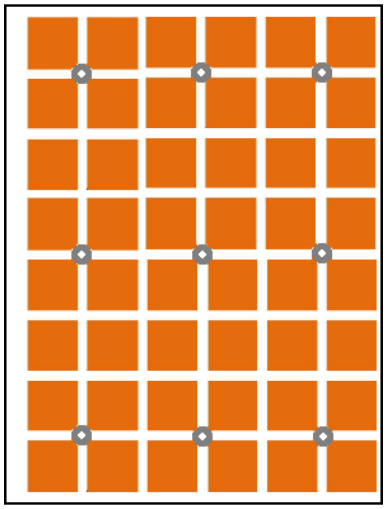
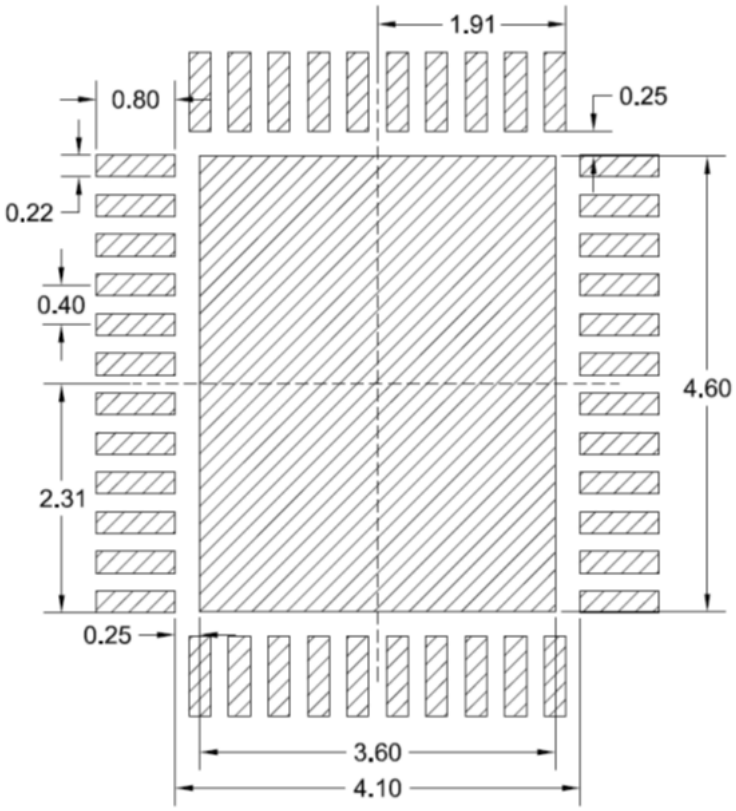


Figure 10. **Recommended footprint outline**



3 Digital interface layout considerations

To avoid the noise injection on the digital signals by the switching activity of the DC/DC converters, it is a good practice to shield the digital traces by ground planes placed on adjacent layers. Other suggestions are:

- Partition mixed-signal PCB with separate analog and digital sections
- Route digital signals only in the digital section of the board (I^2C BUS)
- In case ground or power plane must be split for a specific reason (i.e. mechanical and or electrical), do not place any traces across the gap on an adjacent layer
- The digital decoupling capacitor for VIO pin should be connected directly to the digital ground if VIO is supplied far from the STPMIC1

4 PCB example: the STPMIC1 evaluation board

Table 1. 4-layer stack-up PCB

Layer	Stack-up
Top	Component/power/signal
Mid signal 1	GND
Mid signal 2	Power/GND
Bottom	Small signal/GND

The following pictures show the board layout for the evaluation board STEVAL-PMIC1x. All guidelines are applied to the drawing of the board for the best performance of the STPMIC1.

Figure 11. Evaluation board with the STPMIC1 device

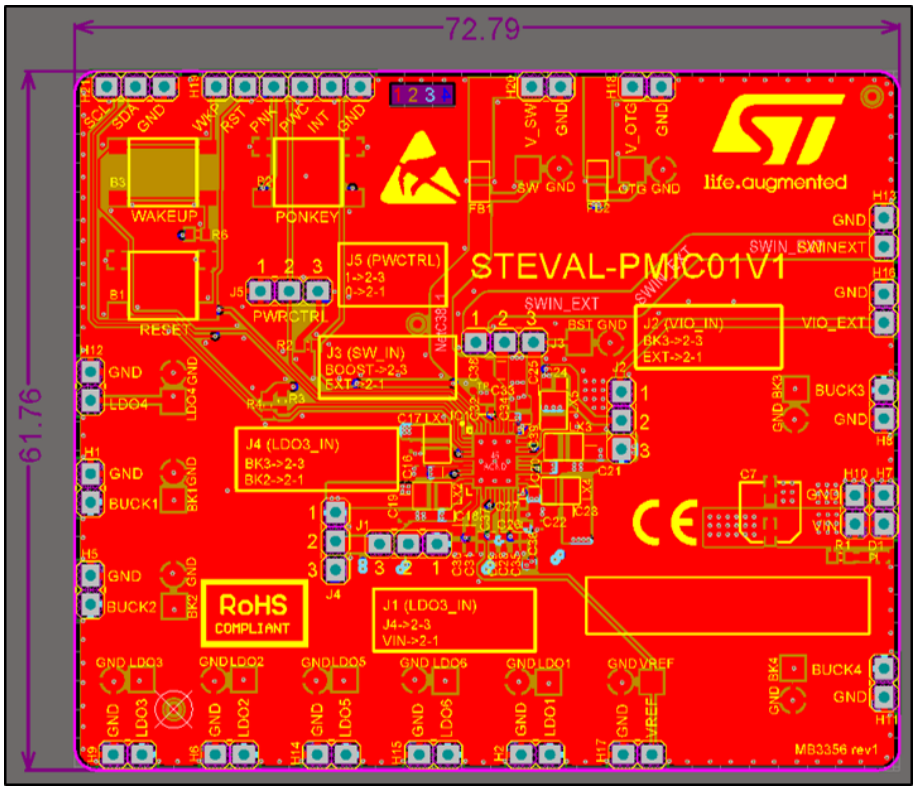


Figure 12. **Top layer (component/power/signal)**

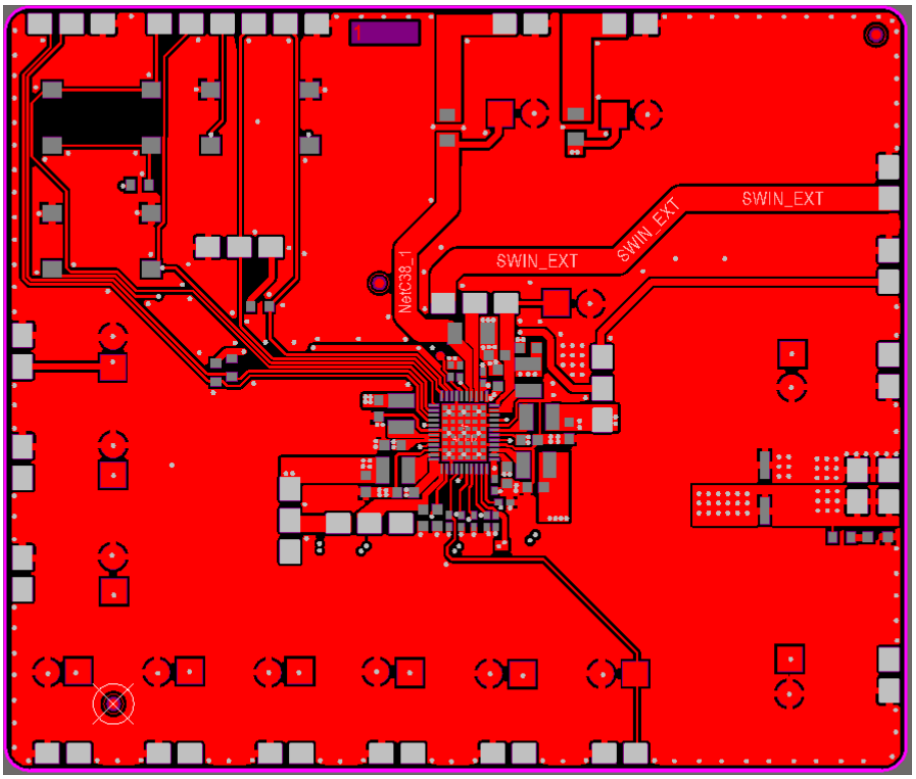


Figure 13. **Mid layer 1 (GND)**

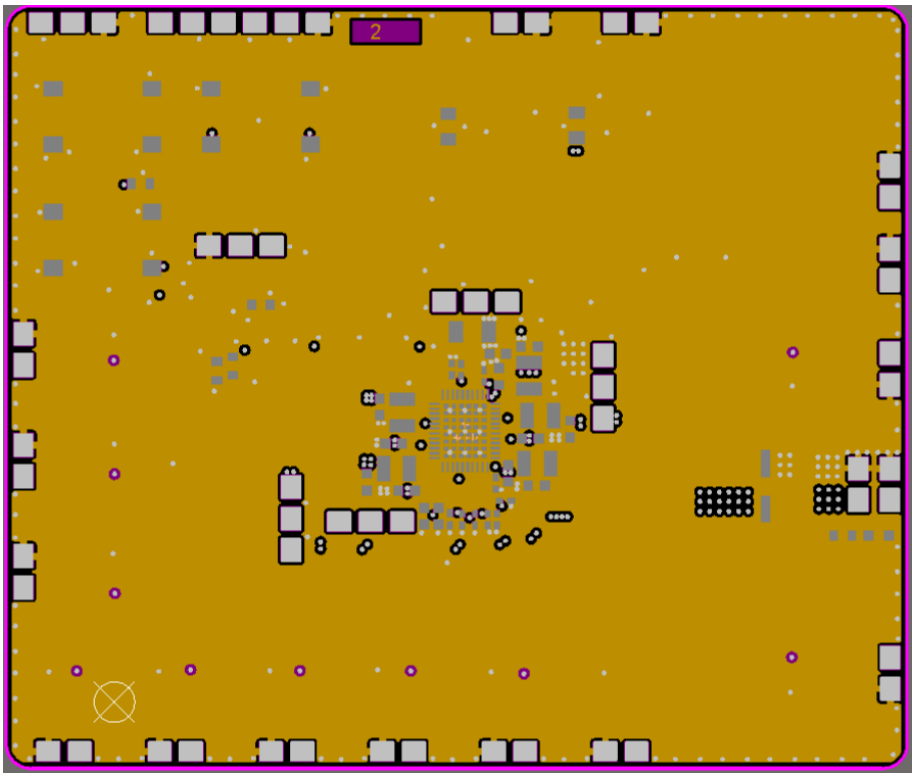


Figure 14. Mid layer 2 (Power/GND)

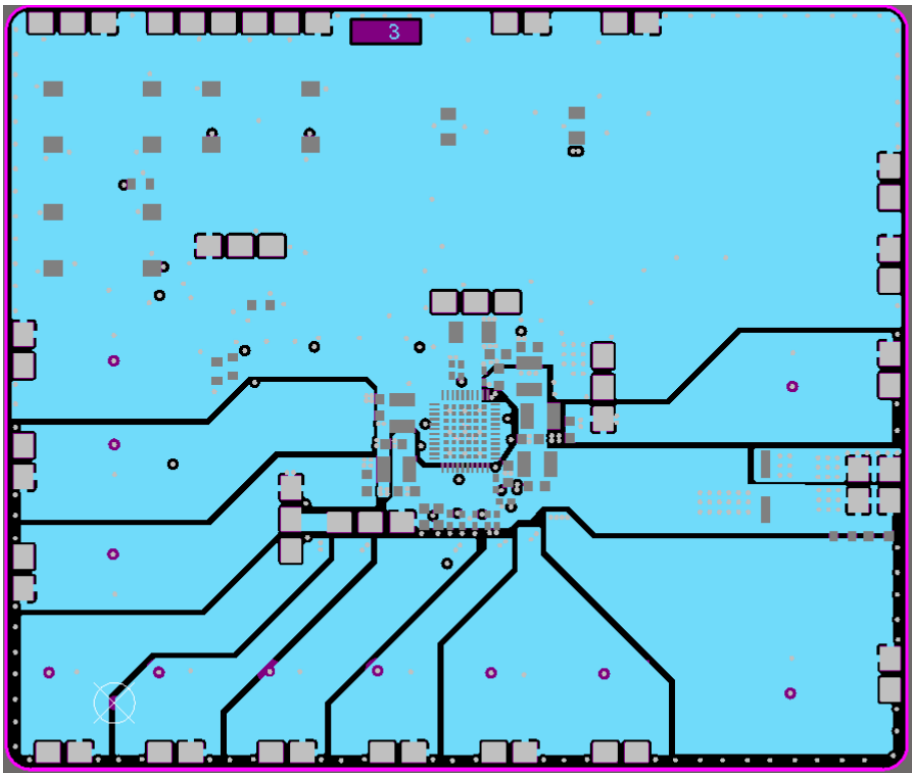
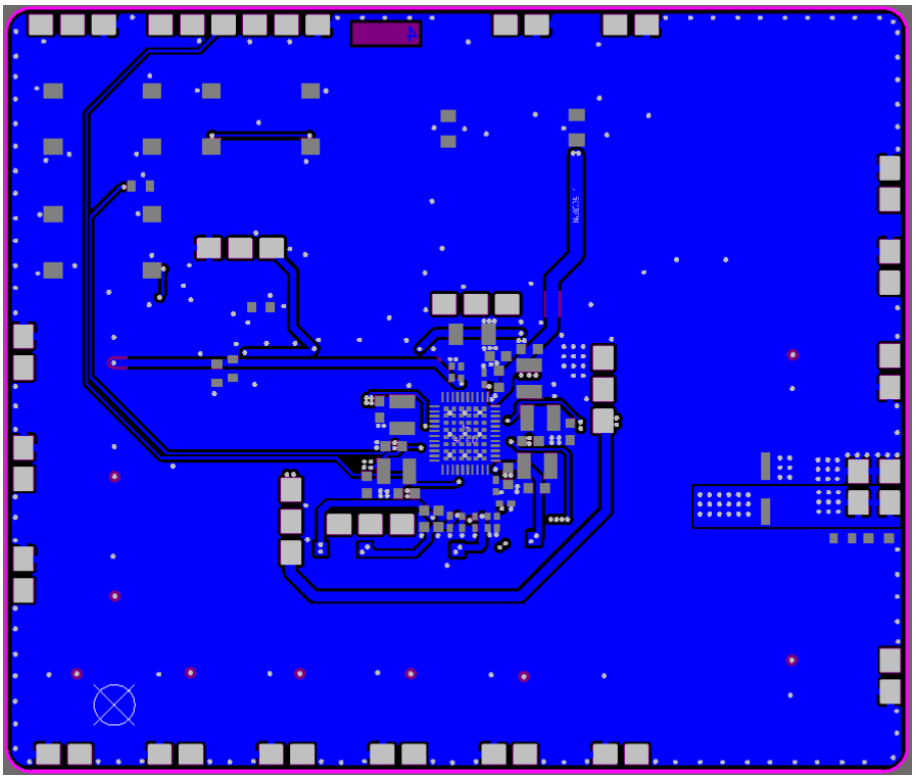


Figure 15. Bottom layer (Small signal/GND)

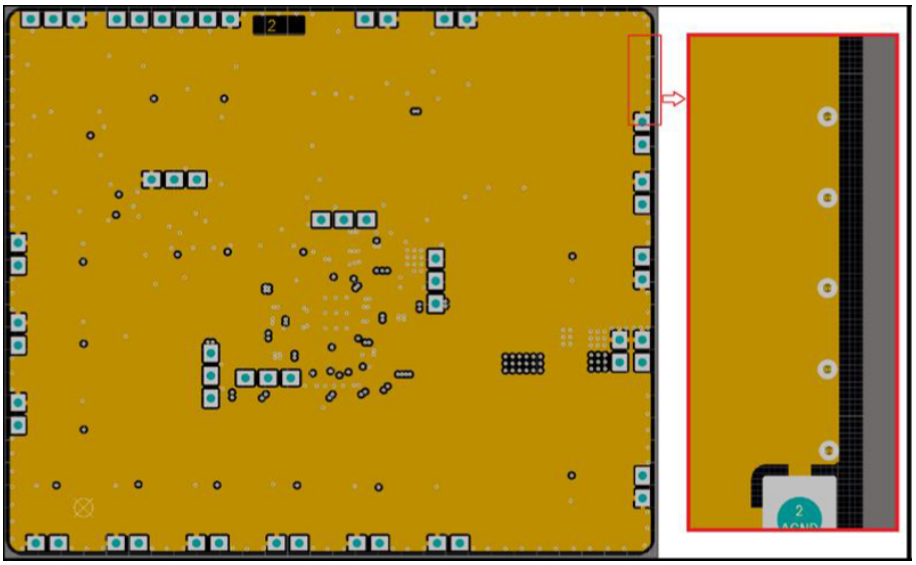


4.1 Power and ground plane

As both POWER and GROUND are planes, inductive effects are minimised, providing a very low impedance path to the STPMIC1. The use of a continuous ground layer with multiple via holes is a good method to achieve low impedance ground returns, but to keep low impedance over all areas of the PCB, it should never be neither narrowed nor partitioned.

Below a view of ground plane of mid layer 1, with GND vias placed all around the PCB edge with 2 mm spacing (see detail in Figure 16. Mid layer 1 (GND plane))

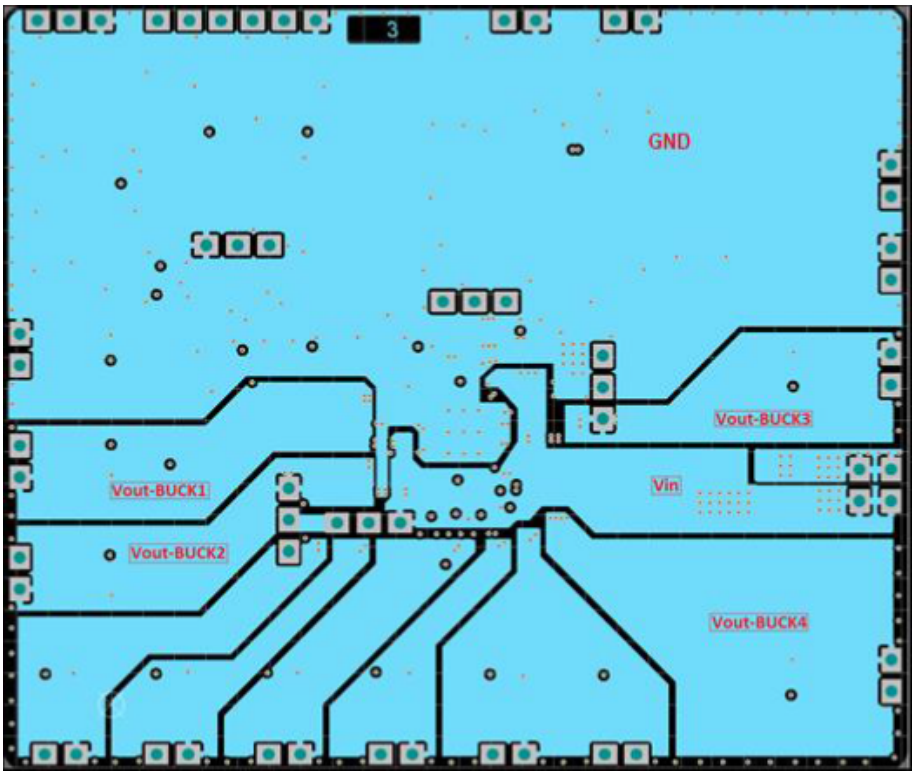
Figure 16. Mid layer 1 (GND plane)



The use of flat and large shapes, where possible, is recommended for all high current power supplies such as V_{IN}, V_{OUT} and VBUS. This has the added value to reduce power losses. When examining the ground and power planes, make sure that the plane continuity is not affected by too many vias.

Examples of power planes, vias placement and plane shapes are shown below for mid-layer 2, used to route V_{IN} and all V_{OUT} of the regulators out to connector headers.

Figure 17. **Mid layer 2 power/GND**



4.2 Via holes

Though the ground plane is a good ground reference, the presence of the vias along ground returns introduces some stray inductances at high frequency. Placing a multiple via holes in a plane reduces this effect considering that the stray inductances are in parallel. Those via holes must be spaced in such a way that the power plane is not excessively cut-up.

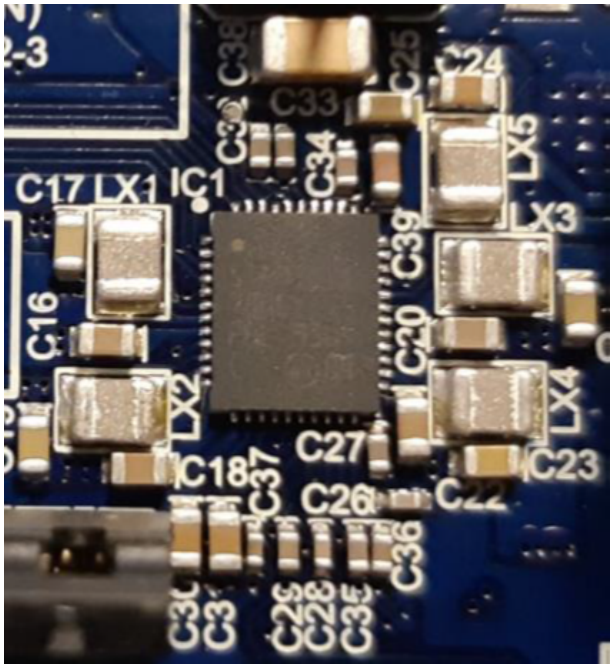
Table 2. Via size

Via type	Hole size	Pad size
Via holes	0.2 mm	0.45 mm

4.3 Component placement example

The Figure 18. Component placement example shows a placement with high component density. In this board all suggestions described in this application note have been met. It is a good practice to put all components on top of the layout and use the bottom side only if it is really needed by the application/board size.

Figure 18. Component placement example



Revision history

Table 3. **Document revision history**

Date	Version	Changes
06-Dec-2019	1	Initial release.

Contents

List of figures