

## STEVAL-VP22201B: 5 V/1.8 W 30 kHz buck demo with the VIPER222XSTR

### Introduction

The STEVAL-VP22201B is a 5 V - 0.36 A power supply set in buck topology using the [VIPER222XSTR](#) off-line high voltage converter by STMicroelectronics, specifically developed for non-isolated SMPS. The device features:

- A 730 V avalanche rugged power section
- Integrated HV-start-up current generator
- Onboard soft-start
- PWM operation at 30 kHz with frequency jittering for lower EMI
- Transconductance error amplifier with 1.2 V  $\pm 2\%$  reference voltage

Thanks to the advanced light load management and ultra-low consumption of the [VIPER222XSTR](#) internal blocks, the evaluation board input power consumption in no-load conditions can be reduced to less than 20 mW at 230 V<sub>AC</sub>, and the most stringent energy saving regulations in terms of active mode and light load efficiency can be achieved.

IC protection features include:

- Pulse skip mode to avoid flux-runaway during start-up
- Delayed overload shutdown for safe fault condition management
- Thermal shutdown

All protections (except pulse skip mode) involve auto-restart mode.

Figure 1. STEVAL-VP22201B top and bottom view



# 1 Board electrical specifications and design

The electrical specifications of the demo board are listed in the table below.

**Table 1. STEVAL-VP22201B electrical specifications**

Parameter	Symbol	Value
Input voltage range	$V_{IN}$	[85 V <sub>AC</sub> ; 265 V <sub>AC</sub> ]
Output voltage	$V_{OUT}$	5 V
Max. output current	$I_{OUT}$	0.36 A
Total Output Power ( $P_{OUT1}+P_{OUT2}$ )	$P_{OUT}$	1.8 W
Precision of Output 1 regulation	$\Delta V_{OUT\_LF}$	±5%
High frequency Output 1 ripple voltage	$\Delta V_{OUT\_HF}$	50 mV
Max. ambient operating temperature	$T_{AMB}$	60 °C
Switching frequency	$F_{OSC}$	30 kHz

## 1.1 Circuit description

The EA-IN pin is the inverting input of the [VIPER222XSTR](#) internal error amplifier and is an accurate 1.2 V voltage reference with respect to the GND pin. This allows the voltage across the capacitor C8 to be set (which actually is a replica of the output voltage) through the R3 and R4 voltage divider in the circuit schematic, according to the following formula:

$$V_{OUT} = V_{EA\_IN} \cdot \left(1 + \frac{R4}{R3}\right) \quad (1)$$

Where resistor R4 is split into R4a and R4b to improve tuning of the output voltage value.

The compensation network is connected between the EA-OUT pin (the output of the error amplifier) and the GND pin.

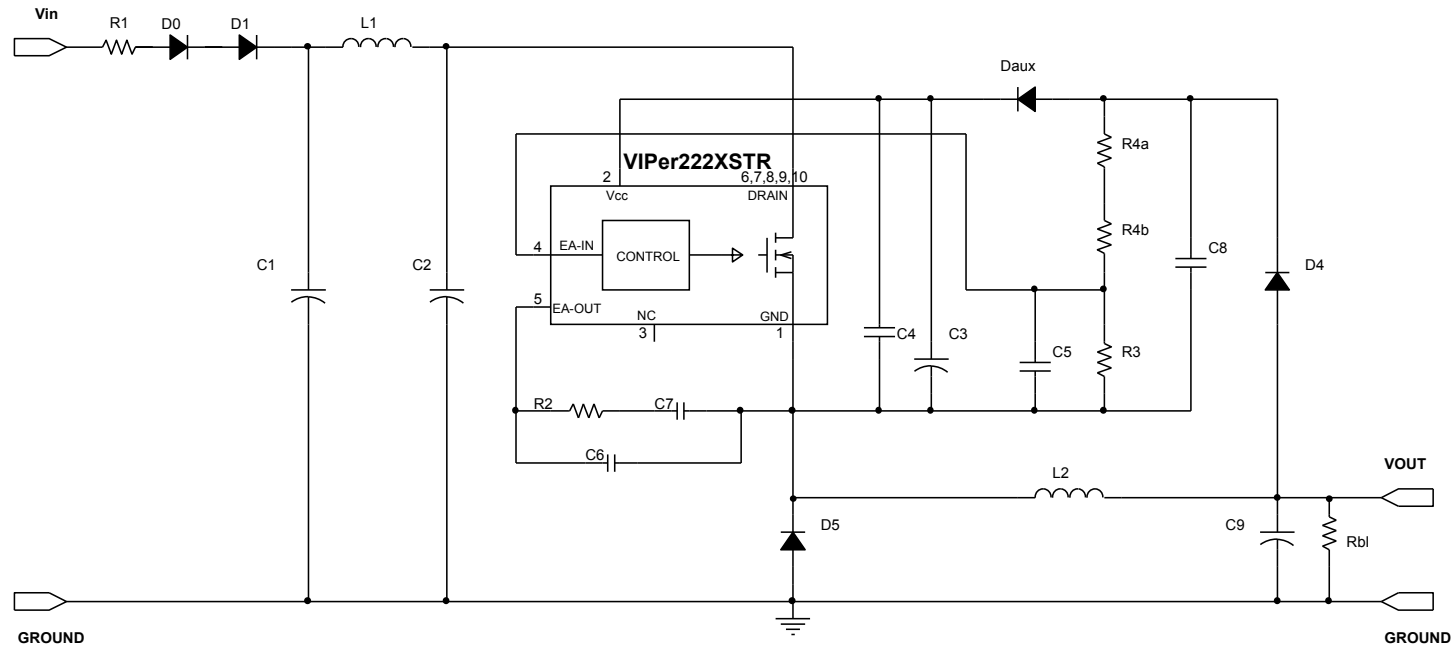
The bleeder resistor Rbl provides a 1 mA approximate minimum load to avoid overvoltage when the output load is disconnected. It is a trade-off between overvoltage containment and increased power consumption under no load. At power-up, as  $V_{DRAIN}$  exceeds  $V_{HVSTART}$ , the internal HV current generator charges VCC capacitor C3 to  $V_{CCOn}$ , the power MOSFET starts switching, the current generator is turned off and the IC is powered through C3.

When  $V_{OUT}$  reaches its steady-state value, the IC is biased from the output through the diode  $D_{AUX}$ . This external biasing and can be applied because the 5 V output voltage is high enough to keep the C3 voltage above the  $V_{CSOn}$  threshold, whose maximum value  $V_{CSOn\_max}$  is 4.5 V. With this setting, the VCC voltage shape during steady-state operation is constant and follows the output voltage, the HV current generator is never activated, and very low input power consumption under light or no-load conditions is possible (less than 20 mW at 230 V<sub>AC</sub> under no-load with an appropriate design) thanks to the low consumption of the internal blocks of the IC.

## 2

## Schematic diagrams

Figure 2. STEVAL-VP22201B schematic diagram



### 3 Bill of materials

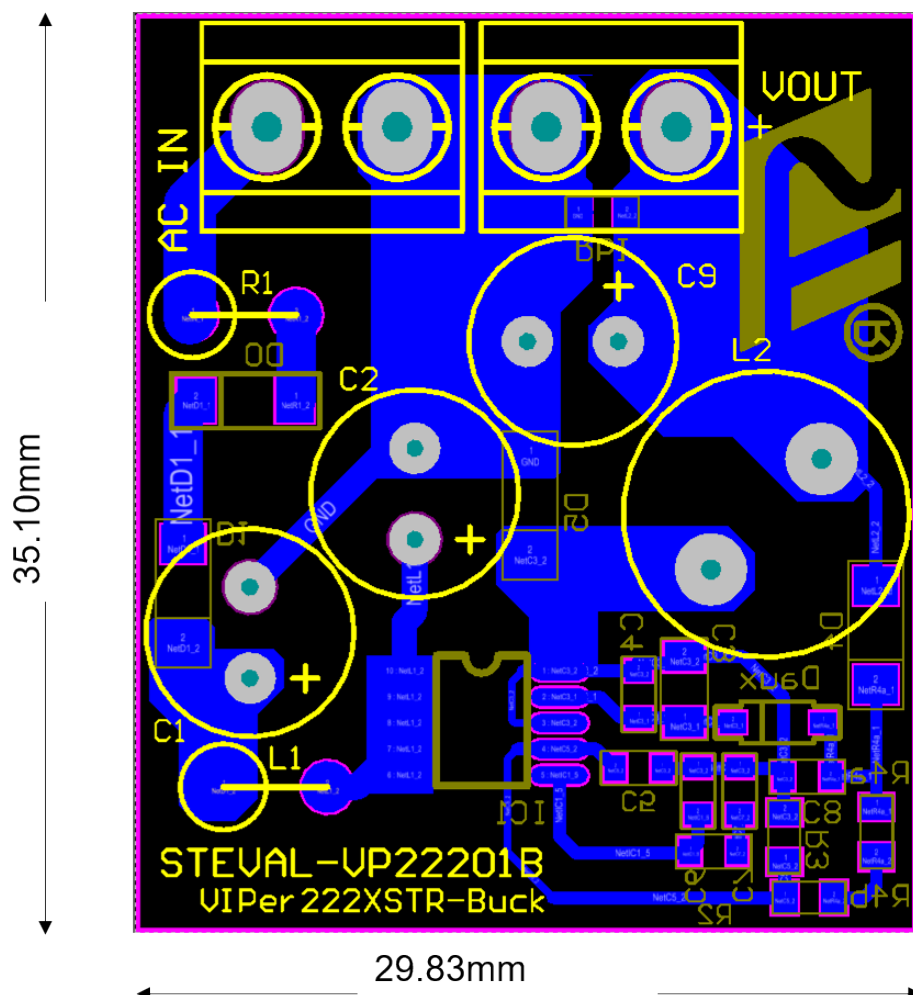
**Table 2. STEVAL-VP22201B bill of materials**

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
1	1	D0	1000V, 1A	General purpose diode , DO-214AC	ON Semiconductor	MRA4007T3G
2	1	D1	1000V, 1A	General purpose diode, DO-214AC	ON Semiconductor	MRA4007T3G
3	1	Daux	150V, 0.15A	Signal schottky diode, SOD-123	ST	<a href="#">BAT46ZFILM</a>
4	1	D4	600V, 1A	General purpose diode , SMA	ST	<a href="#">STTH1L06A</a>
5	1	D5	600V, 1A	General purpose diode , SMA	ST	<a href="#">STTH1L06A</a>
6	1	C1	4.7µF, 400V, ±20%	Electrolitic Capacitor, Ø8mm - p3.5mm - h 13.5mm	Rubycon	400PX4R7MEFC8X11.5
7	1	C2	4.7µF, 400V, ±20%	Electrolitic Capacitor, Ø8mm - p3.5mm - h 13.5mm	Rubycon	400PX4R7MEFC8X11.5
8	1	C3	2.2µF, 50V, ±10%	Multilayer Ceramic Capacitor, 0805	Taiyo Yuden	UMK212BB7225KG-T
9	1	C4	100nF, 50V, ±10%	Multilayer Ceramic Capacitor , 0603	Yageo	CC0603KRX7R9BB104
10	2	C5, C6	not mounted	Multilayer Ceramic Capacitor, 0603		
11	1	C7	1nF, 50V, ±5%	Multilayer Ceramic Capacitor, 0603	TDK	C1608C0G1H102J080AA
12	1	C8	220nF, 50V, ±10%	Multilayer Ceramic Capacitor, 0603	TDK	C1608X7R1H224K080AB
13	1	C9	330µF, 16V, ±20%	electrolitic cap. ultra-low ESR, ZL series, Ø8mm – p.3.5mm – h11.5mm	Rubycon	16ZL330MEFC8X11.5
14	1	R1	15Ω, 1W, ±5%	flameproof resistor , Ø3m - p9mm	TE Connectivity	ROX1SJ15R
15	1	R2	2.7kΩ, 0.1W, ±1%	resistor , 0603	Vishay	CRCW06032K70FKEA
16	1	R3	22kΩ, 0.1W, ±1%	resistor , 0603	Vishay	CRCW060322K0FKEA
17	1	R4a	56kΩ, 0.1W, ±1%	resistor , 0603	Vishay	CRCW060356K0FKEA
18	1	R4b	22kΩ, 0.1W, ±1%	resistor , 0603	Vishay	CRCW060322K0FKEA
19	1	Rbl	5.6kΩ, 0.1W, ±1%	resistor , 0603	Vishay	CRCW06035K60FKEA
20	1	L1	1mH , 0.2A, ±5%	filter inductor, axial	EPCOS	B82144A2105J000

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
21	1	L2	0.47mH, 0.99A, ±10%	power inductor, radial Ø10.5mm – p5mm - h12mm	Coilcraft	DR0810-474L
22	1	IC1	-	Offline HV converter, SSO-10	ST	VIPER222XSTR
23	1	IN	250Vac, 13.5A	through hole input connector, L.11.5mm - W.10.76mm - D.8.2mm - P.5.08mm	TE Connectivity	282837-2
24	1	OUT	250Vac, 13.5A	through hole output connector, L.11.5mm - W.10.76mm - D.8.2mm - P.5.08mm	TE Connectivity	282837-2

## 4 Board layout

Figure 3. Layout complete

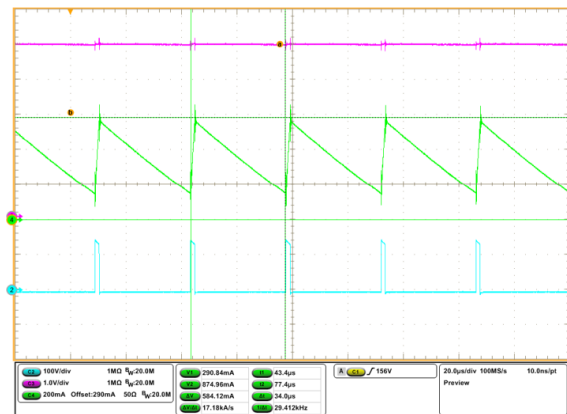


## 5 Testing the board

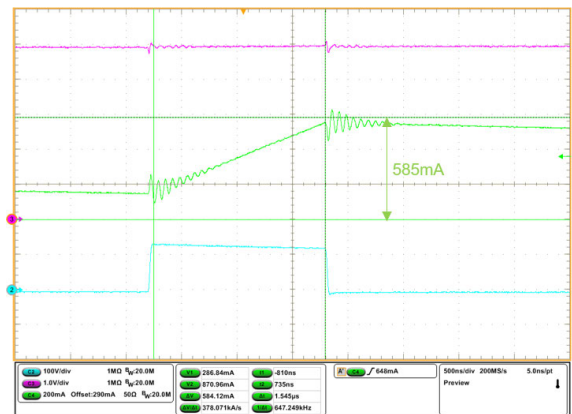
### 5.1 Typical waveforms

Voltage and current waveforms at nominal  $V_{IN}$  in full load conditions are shown below.

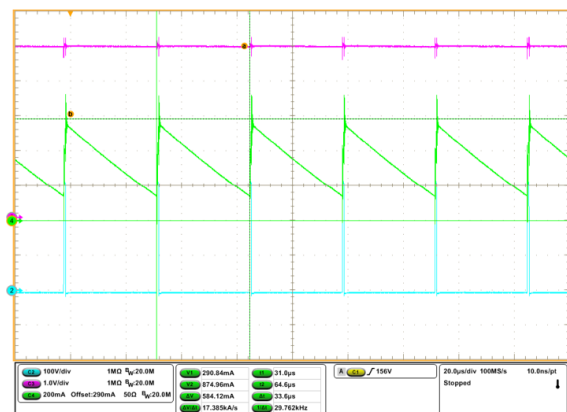
**Figure 4. Waveforms @ 115 V<sub>AC</sub>, full load**



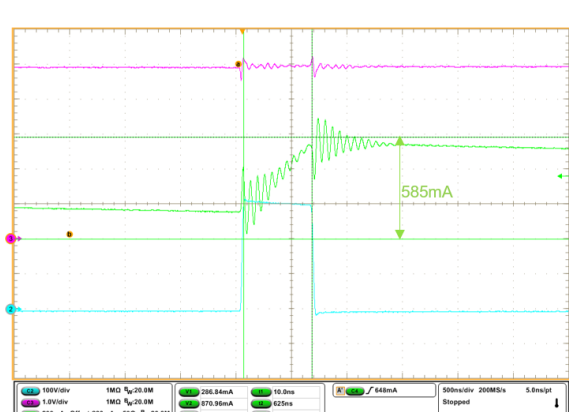
**Figure 5. Waveforms @ 115 V<sub>AC</sub>, full load, zoom**



**Figure 6. Waveforms @ 230 V<sub>AC</sub>, full load**

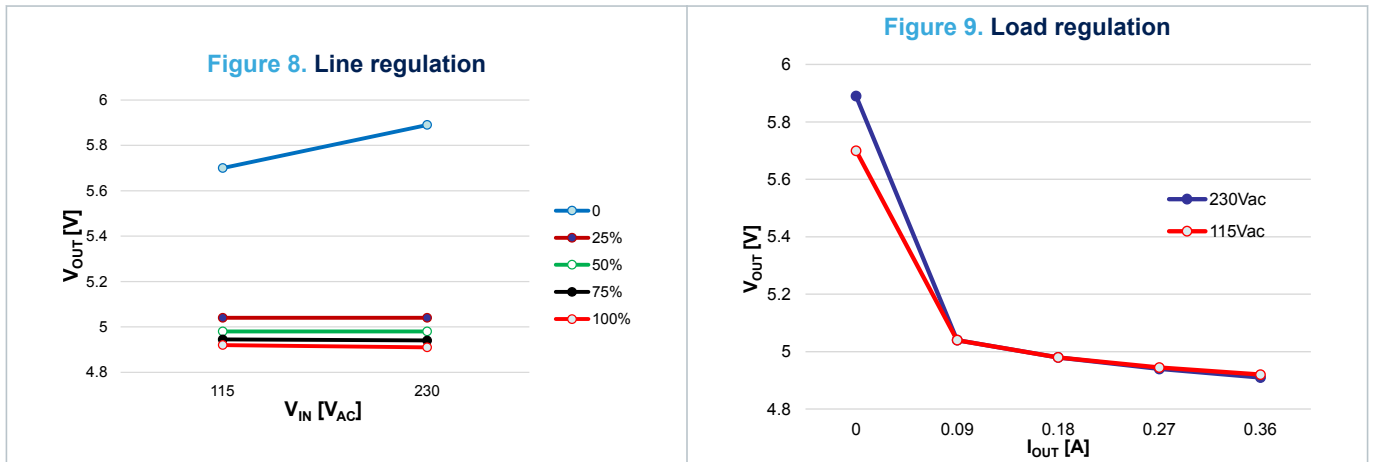


**Figure 7. Waveforms @ 230 V<sub>AC</sub>, full load, zoom**



### 5.2 Line and load regulation

The output voltage has been measured in different line and load conditions. The results are shown in the following figures.



### 5.3 Efficiency measurements

The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% of maximum load, at nominal input voltages ( $V_{IN} = 115\text{ V}_{AC}$  and  $V_{IN} = 230\text{ V}_{AC}$ ).

**Table 3. STEVAL-VP22201B active mode efficiency**

Input voltage	Active mode efficiency [%]
115 V <sub>AC</sub>	71.3
230 V <sub>AC</sub>	68.7

### 5.4 Light load performance

For a 1.8 W SMPS, version 5 of Code of Conduct (CoC5) requires efficiency higher than 61% when the output load is 10% of the nominal output power, and input power consumption lower than 150 mW in no load condition. The following tables demonstrate the STEVAL-VP22201B compliance with these requirements.

**Table 4. STEVAL-VP22201B efficiency at 10% output load**

Input voltage	efficiency at 10% output load [%]
115 V <sub>AC</sub>	70.0
230 V <sub>AC</sub>	65.3

**Table 5. STEVAL-VP22201B input power consumption under no load**

$V_{IN}$ [V <sub>AC</sub> ]	No load	
	$V_{OUT}$ [V]	$P_{IN}$ [mW]
115	5.70	11.97
230	5.89	16.47

Another standard, EuP lot 6, requires that the input power should be less than 500 mW when the converter is loaded with 250 mW.

The following table shows how the STEVAL-VP22201B board satisfies this requirement, along with efficiency figures for  $P_{OUT} = 25\text{ mW}$  and  $P_{OUT} = 50\text{ mW}$  light load conditions.



**Table 6. STEVAL-VP22201B light load performance**

$V_{IN}$ [V <sub>AC</sub> ]	efficiency [%]		
	$P_{OUT}=25mW$	$P_{OUT}=50mW$	$P_{OUT}=250mW$
115	54.3	61.4	70.4
230	48.7	56.7	65.7

The following table provides data for another output power (or efficiency) criterion, when the input power is one watt.

**Table 7. Efficiency at  $P_{IN}=1W$** 

$V_{IN}$ [V <sub>AC</sub> ]	efficiency at $P_{IN}=1W$ [%]
115	71.5
230	69.6

## 6 Functional check

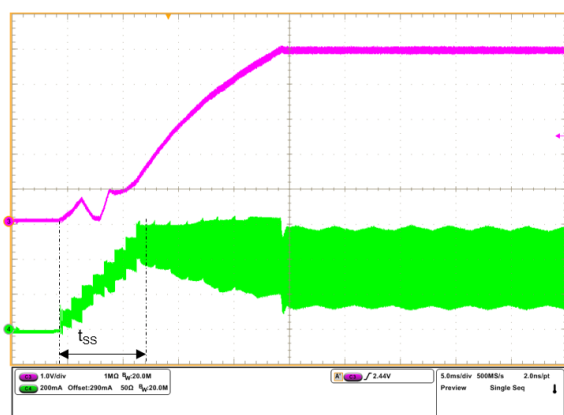
### 6.1 Start-up

The start-up phase at maximum load and 115 V<sub>AC</sub> and 230 V<sub>AC</sub> nominal input voltages are shown in Figure 10 and Figure 12.

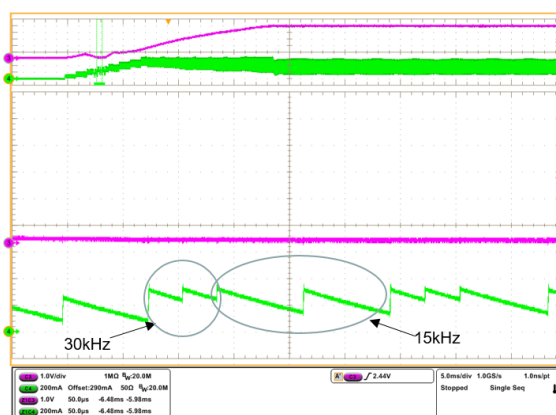
An internal soft-start function progressively increases the cycle-by-cycle current limitation set point from zero up to I<sub>DLIM</sub> in 8 steps. This limits drain current during the output voltage rise, thus reducing the stress on the secondary diode. The t<sub>SS</sub> soft-start time needed for the current limitation to reach its final value is internally set at 8 ms. This function is activated for any converter start-up attempt or after a fault event. The IC has a “pulse skipping” feature, which skips a switching cycle whenever the OCP comparator is triggered within the minimum on-time. The switching frequency is thus halved down to the minimum allowed value of F<sub>OSC\_MIN</sub> (15 kHz, typ.).

By allowing a longer inductor discharge time, this feature helps prevent current runaway: the possible uncontrolled increase in drain current during the very first cycles of converter start-up, due to the initial inability of the system to maintain the volt-second balance when there is a large input-to-output voltage differential. Whenever the OCP comparator is not triggered within the minimum on-time, a switching cycle is restored, thus doubling the switching frequency up to the nominal frequency F<sub>OSC</sub>.

**Figure 10. Start-up at V<sub>IN</sub> = 115 V<sub>AC</sub>, full load**

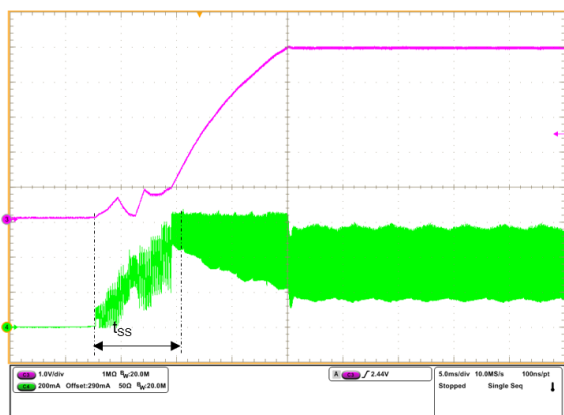


**Figure 11. Start-up at V<sub>IN</sub> = 115 V<sub>AC</sub>, full load, zoom**

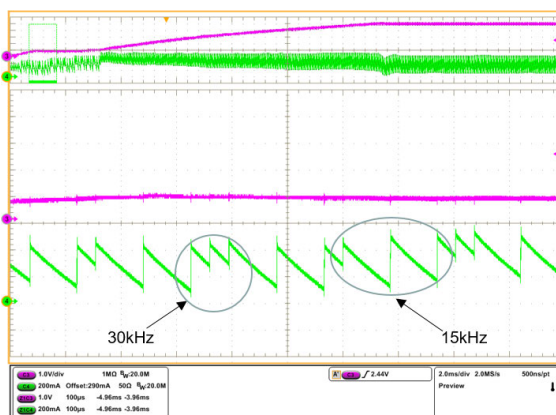


Pulse skipping and F<sub>OSC</sub> restoration are evident in and Figure 11 and Figure 13

**Figure 12. Start-up at V<sub>IN</sub> = 230 V<sub>AC</sub>, full load**

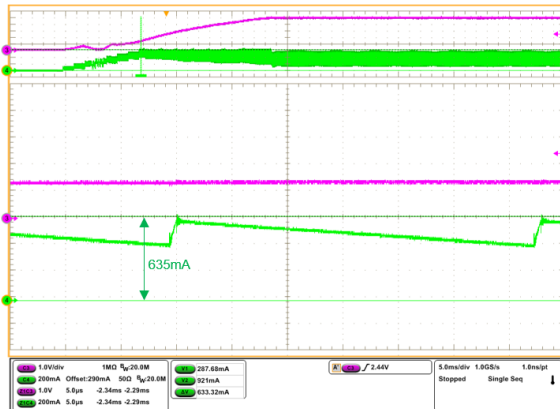


**Figure 13. Start-up at V<sub>IN</sub> = 230 V<sub>AC</sub>, full load, zoom**

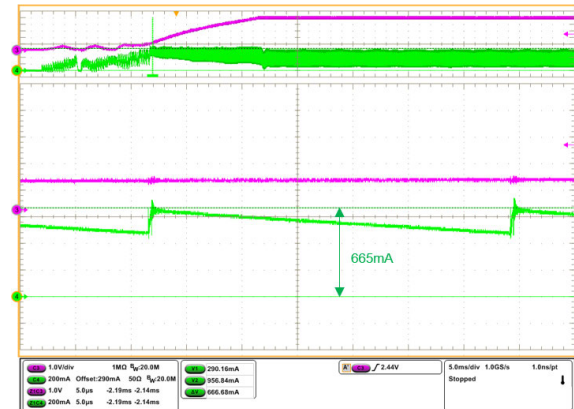


The effect of pulse skipping feature is shown in Figure 14 and Figure 15 : the maximum value reached by the peak current at start-up is quite low, both at 115 V<sub>AC</sub> and at 230 V<sub>AC</sub>.

**Figure 14. Max. peak current at V<sub>IN</sub> = 115 V<sub>AC</sub>, start-up in full load conditions**



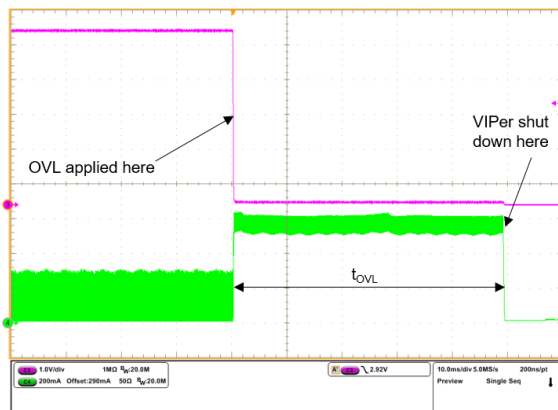
**Figure 15. Max. peak current at V<sub>IN</sub> = 230 V<sub>AC</sub>, start-up in full load conditions**



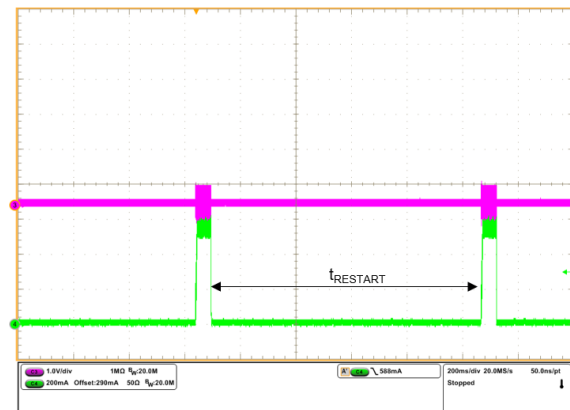
## 6.2 Overload protection

During an overload or short-circuit, the drain current reaches I<sub>DLIM</sub> (see Figure 16) . For every cycle that this condition is met, an internal OCP counter is incremented and the protection is tripped if the fault is maintained for time t<sub>OVL</sub> (50 ms typical, set internally): the power section is turned off and the converter is disabled for time t<sub>RESTART</sub> (1 s typical). After this time, the IC resumes switching and, if the fault is still present, the protection occurs indefinitely in the same way (see Figure 17). This ensures a low rate of converter restart attempts for safe operation and extremely low power throughput while avoiding IC overheating in case of repeated fault events.

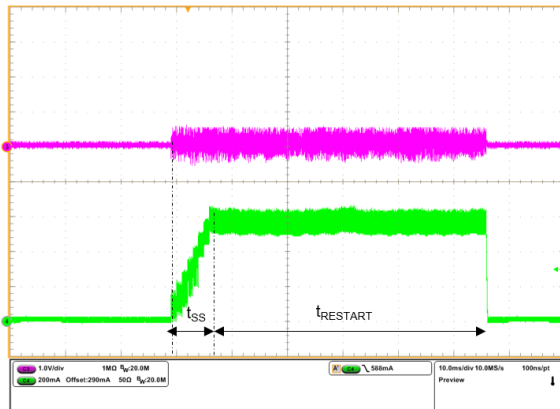
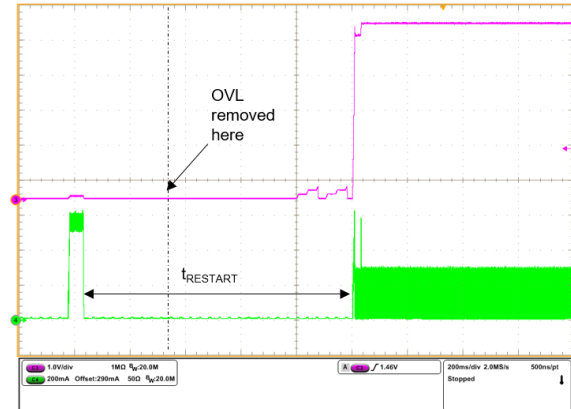
**Figure 16. Output overload applied: OLP tripping**



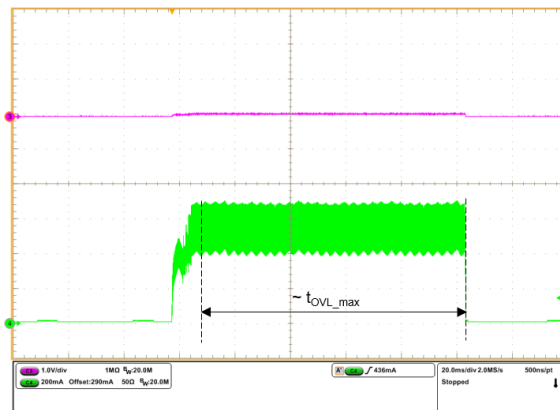
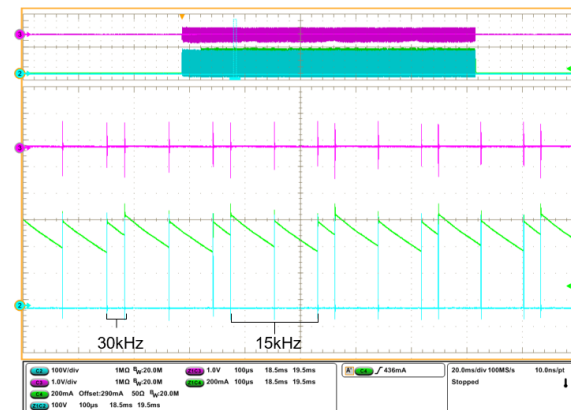
**Figure 17. Output overload maintained: OLP steady-state**



Moreover, every time the protection is tripped, the internal soft start-up function is invoked at restart (Figure 18). The IC resumes normal operation when the short is removed. If the short is removed during t<sub>SS</sub> or t<sub>OVL</sub>, before the protection is tripped, the counter decrements each cycle down to zero and the protection is not tripped. If the short-circuit is removed during t<sub>RESTART</sub>, the IC waits for the t<sub>RESTART</sub> period to elapse before resuming switching (Figure 19).

**Figure 18. Output overload maintained:  $t_{SS}$  and  $t_{OVL}$** 

**Figure 19. OLP: short-circuit removed and auto-restart**


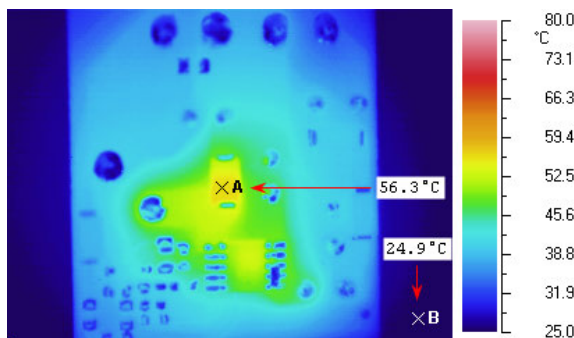
During overload at high  $V_{IN}$ , when the  $t_{ON}$  falls, the  $I_{DLIM}$  may be exceeded within the minimum on time, causing the switching frequency to be reduced by the pulse skipping function and the time needed for the OCP counter to reach its end of count to increase accordingly. In case of  $F_{OSC} = 30\text{ kHz}$ ,  $t_{OVL}$  could range between 50 ms (when pulse skipping is never invoked) and 100 ms (when pulse skipping is always invoked, and the actual switching frequency is always half  $F_{OSC}$ ). In Figure 20  $t_{OVL}$  is increased to 100 ms. The magnified Figure 21 shows the frequency reduction due to pulse skipping during overload. When the fault is removed, the device waits for  $t_{RESTART}$  to elapse before resuming switching via soft-start.

**Figure 20. Output overload at 230 V<sub>AC</sub>:  $t_{OVL}$  increase**

**Figure 21. Output overload at 230 V<sub>AC</sub>: pulse skipping**


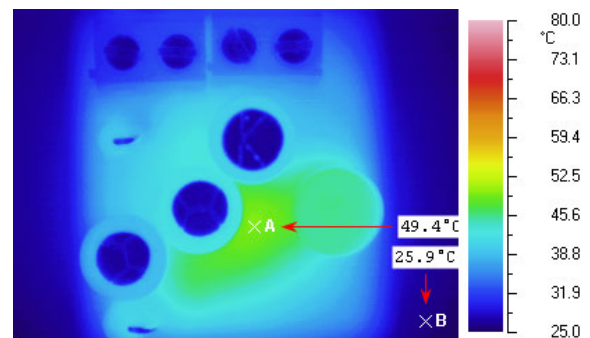
## 7 Thermal measurements

Thermal analysis of the board was performed using an IR camera at 115 V<sub>AC</sub> and 230 V<sub>AC</sub> mains input, full load condition. The results are shown in the following figures, where “A” indicates the highest temperature point and “B” the ambient temperature.

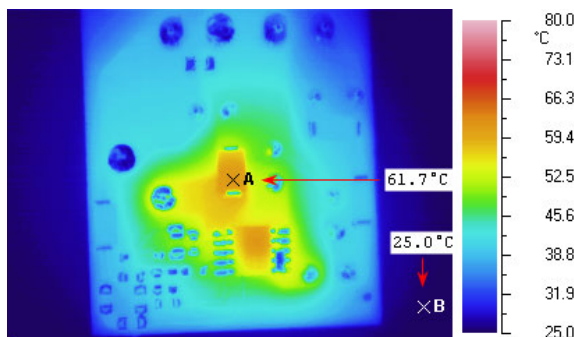
**Figure 22. Thermal measurements at V<sub>IN</sub> = 115 V<sub>AC</sub> full load (bottom view)**



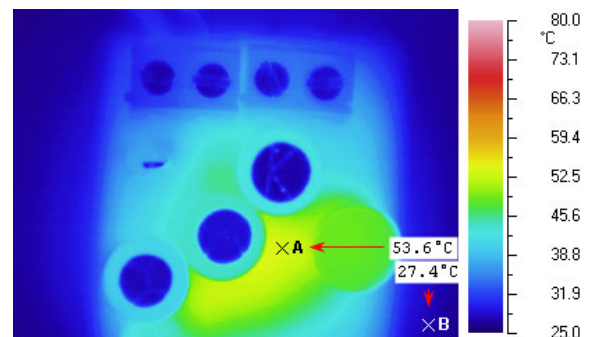
**Figure 23. Thermal measurements at V<sub>IN</sub> = 115 V<sub>AC</sub> full load (top view)**



**Figure 24. Thermal measurements at V<sub>IN</sub> = 230 V<sub>AC</sub> full load (bottom view)**

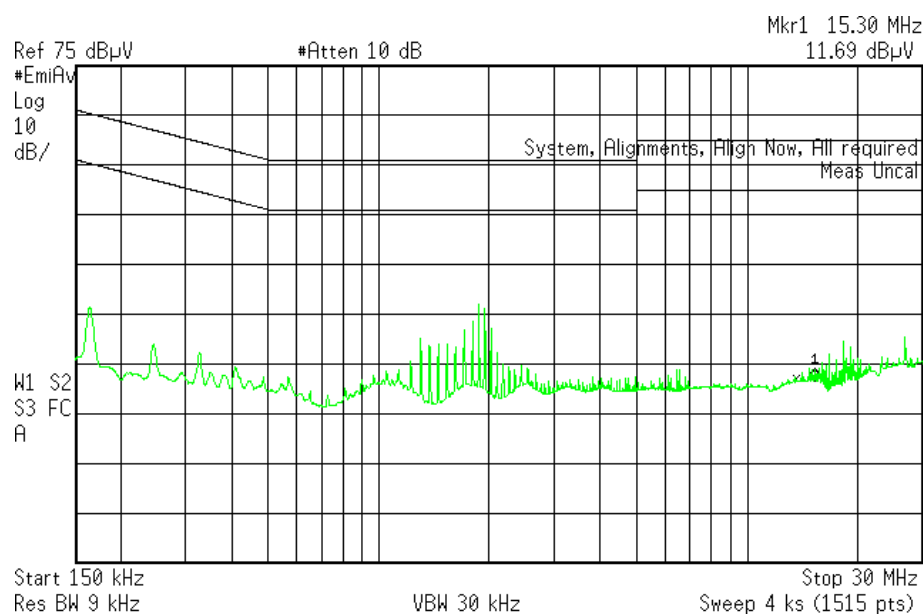


**Figure 25. Thermal measurements at V<sub>IN</sub> = 230 V<sub>AC</sub> full load (top view)**

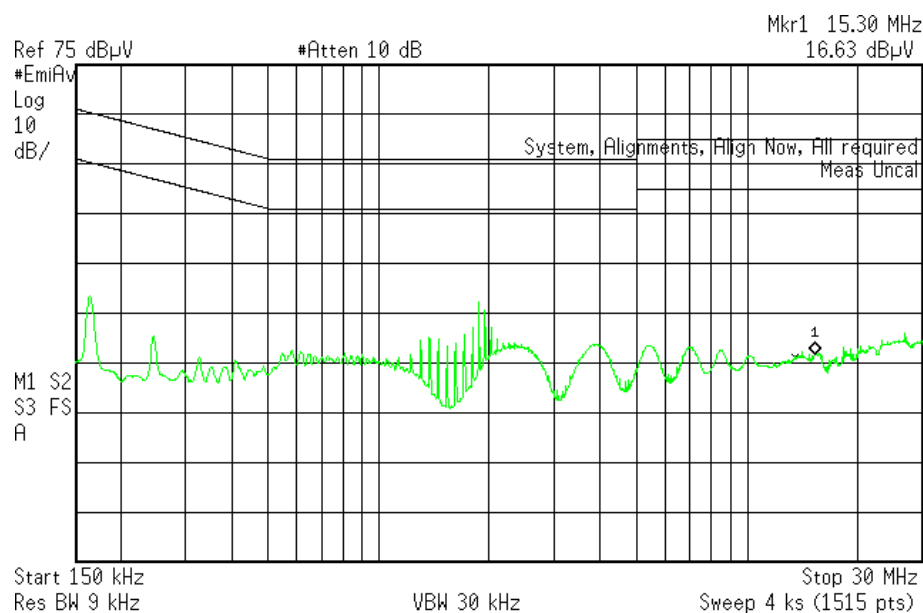


## 8 Noise measurements

**Figure 26. STEVAL-VP22201B CE average measurement at 115 V<sub>AC</sub> full load**



**Figure 27. STEVAL-VP22201B CE average measurement at 230 V<sub>AC</sub> full load**

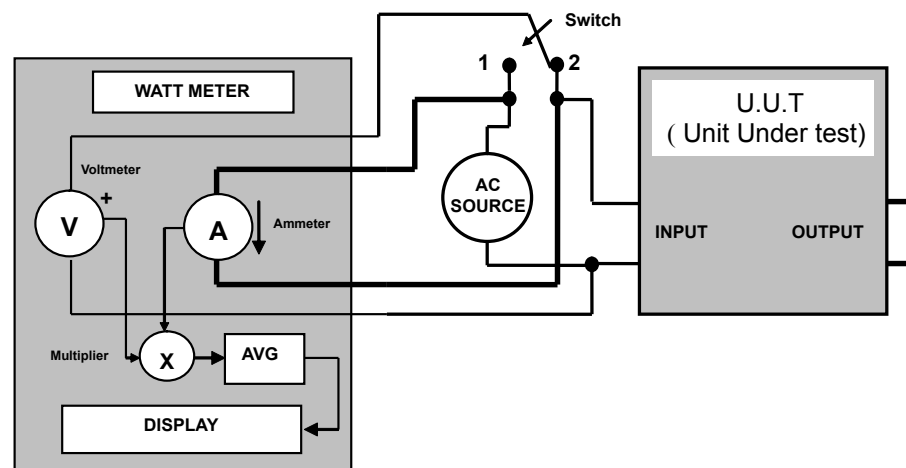


## Appendix A Appendix (test equipment and measurement of efficiency and low load performance)

The converter input power has been measured using a wattmeter. The wattmeter measures simultaneously the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The wattmeter is a digital instrument so it samples the current and voltage and converts them in digital forms. The digital samples are then multiplied giving the instantaneous measured power. The sampling frequency is in the range of 20 kHz (or higher depending on the instrument used). The display provides the average measured power, averaging the instantaneous measured power in a short period of time (1 s typ.).

The figure below shows how the wattmeter is connected to the UUT (unit under test) and to the AC source and the wattmeter internal block diagram.

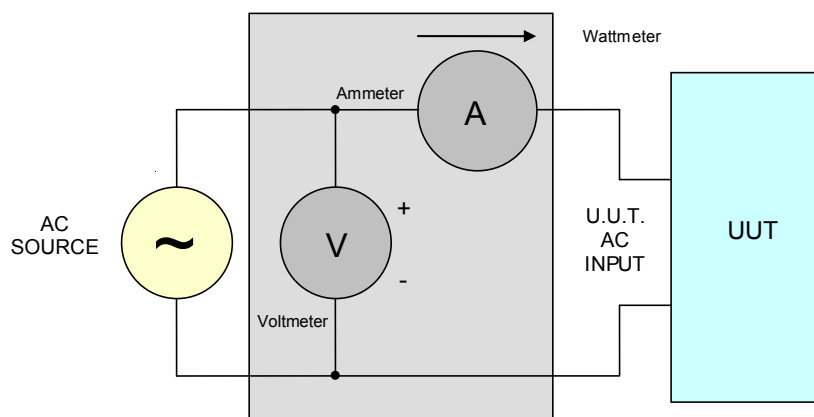
**Figure 28. Connections of the UUT to the wattmeter for power measurements**



An electronic load has been connected to the output of the power converter (UUT), allowing the converter load current to be set and measured, while the output voltage has been measured by a voltmeter. The output power is the product between load current and output voltage. The ratio between the output power, calculated as previously stated, and the input power, measured by the wattmeter, is the converter efficiency, which has been measured in different input/output conditions.

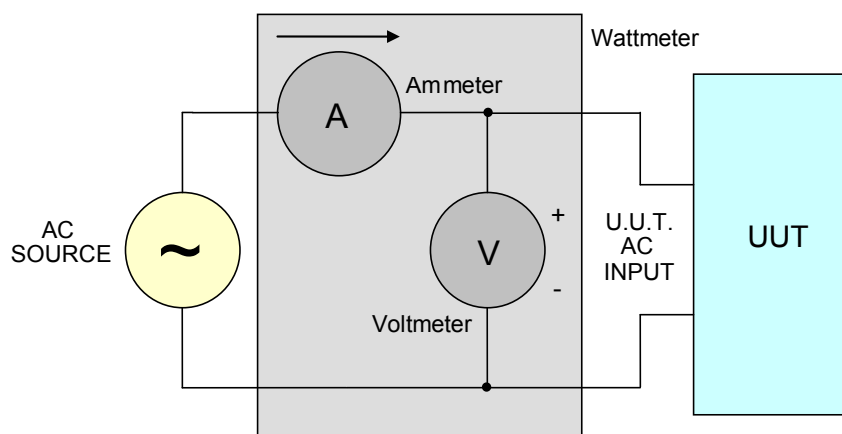
**Measuring input power notes** With reference to the figure above, the UUT input current causes a voltage drop across the ammeter internal shunt resistance (the ammeter is not ideal so it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT. If the switch of the figure above is in position 1 (see also the simplified scheme of the next figure) this voltage drop causes an input measured voltage higher than the input voltage at the UUT input that, of course, affects the measured power. The voltage drop is generally negligible if the UUT input current is low (for example when we measure the input power of UUT in light load conditions).

**Figure 29. Switch in position 1 - setting for standby measurements**



In case of high UUT input current (for measurements in heavy load conditions), the voltage drop can be relevant (compared to the UUT real input voltage). If this is the case, the switch in [Figure 28. Connections of the UUT to the wattmeter for power measurements](#) should be changed in position 2 (see simplified scheme of figure below) where the UUT input voltage is measured directly to the UUT input terminal and the input current does not affect the measured input voltage.

**Figure 30. Switch in position 2 - setting for efficiency measurements**



On the other hand, the position of the last figure may introduce a relevant error during light load measurements, when the UUT input current is low and the leakage current inside the voltmeter itself (which is not an ideal instrument and does not have infinite input resistance) is not negligible. This is the reason why it is better to use the setting of [Figure 29. Switch in position 1 - setting for standby measurements](#) for light load measurements and [Figure 30. Switch in position 2 - setting for efficiency measurements](#) for heavy load measurements.

If it is not clear which measurement scheme has the lesser effect on the result, try with both and register the lower input power value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT is operated at 100% of nameplate output current output for at least 30 minutes (warm-up period) immediately prior to conducting efficiency measurements.

After this warm-up period, the AC input power is monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value observed, the UUT can be considered stable and the measurements can be recorded at the end of the 5 minute period. If AC input power is not stable over a 5 minute period, the average power or accumulated energy is measured over time for both AC input and DC output.

Some wattmeter models allow integrating the measured input power in a time range and then measuring the energy absorbed by the UUT during the integration time. Dividing by the integration time itself the average input power is calculated.



## Revision history

**Table 8. Document revision history**

Date	Version	Changes
17-Mar-2020	1	Initial release

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