STEVAL-VP319X1B: 5 V/3 W 30 kHz buck demo with VIPER319X

Introduction

The STEVAL-VP319X1B is a 5 V/3 W power supply in buck topology based on the VIPER31 energy saving off-line high voltage converter.

The board features:

- Universal input mains range: 85–265 V_{AC}[1]
- Frequency: 50-60 Hz
- Output voltage: 5 V
- Output current: 0.6 A
- Input power consumption at no load: < 16 mW at 230 V_{AC}
- 4-point average active mode efficiency at full load: > 69.7% (compliant with European CoC ver. 5)
- 4-point average active mode efficiency at 10% full load: > 60.58% (compliant with European CoC ver. 5)
- Compliance with IEC55022 Class B conducted EMI IEC55022 Class B conducted EMI

1. *BOM modification for input range extension down to 40 V_{AC} and the related relevant results are detailed in Section 10: Extended input voltage range operation.*

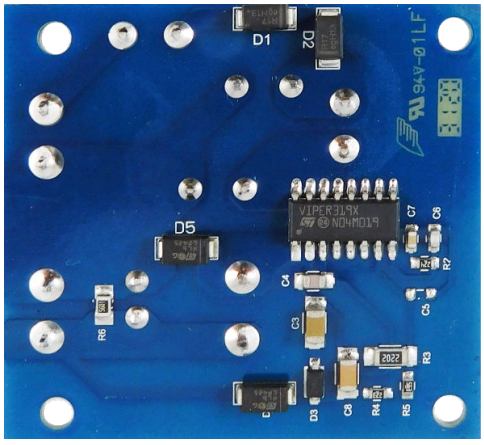
The VIPER31 features:

- 800 V avalanche rugged power section
- Integrated HV start-up current generator
- On-board soft start
- 990 mA typical drain current limitation (at T_J = 25°C)
- Ultra-low consumption (350 µA max. quiescent current) and advanced light load management
- PWM operation at 30 kHz with frequency jittering for lower EMI
- Trans-conductance error amplifier with 1.2 V ± 2% reference voltage
- Protections:
  - pulse skip mode to avoid flux-runaway during start-up
  - delayed overload shutdown for safe fault condition management
  - thermal shutdown

Except for pulse-skip mode, all protections involve auto restart mode.

Figure 1. STEVAL-VP319X1B top view

Figure 2. STEVAL-VP319X1B bottom view



1 Adapter features

Table 1. **STEVAL-VP319X1B electrical specifications**

Parameter	Symbol	Value
Input voltage range	V_{IN}	85 to 265 V_{AC}
Output voltage	V_{OUT}	5 V
Max. output current	I_{OUT}	0.6 A
Max. output power	P_{OUT}	3.0 W
Precision of output regulation	Δ_{VOUT_LF}	±5 %
High frequency output voltage ripple	Δ_{VOUT_HF}	50 mV
Max. ambient operating temperature	T_{AMB}	60ºC
Switching frequency	F_{OSC}	30 kHz

2 Circuit description

The FB pin is the inverting input of the VIPER31 internal error amplifier and is an accurate 1.2 V voltage reference with respect to the GND pin. It allows setting the voltage across C8 capacitor (a replica of the output voltage) through the voltage divider that includes R3, R4 and R5 resistors.

The compensation network is connected between COMP pin (the output of the error amplifier) and GND pin.

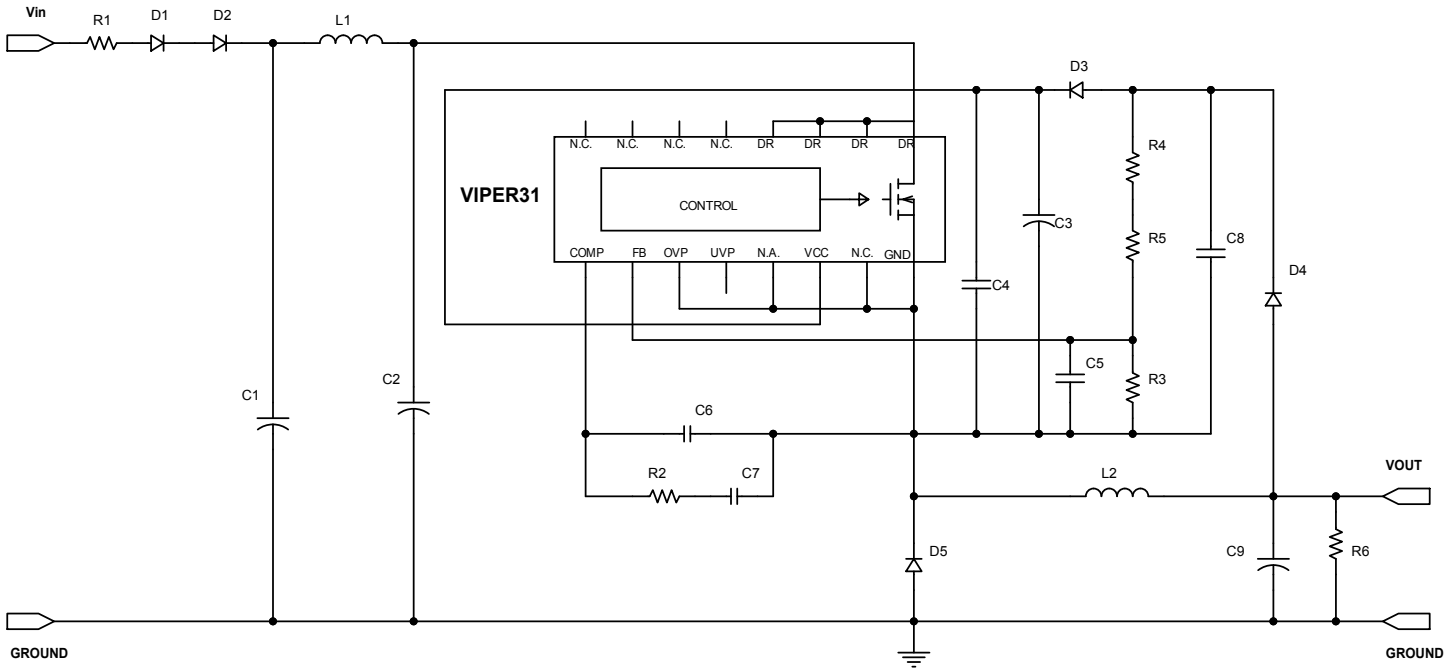
The Rbl bleeder resistor provides an approximate minimum load of 1 mA to avoid overvoltage when the output load is disconnected, creating a tradeoff between the overvoltage containment and the power consumption increase under no load.

At power-up, as V_{DRAIN} exceeds $V_{HVSTART}$, the internal HV current source charges the VCC capacitor, C3, to V_{CCon}, the power MOSFET starts switching, the current source is turned off and the IC is powered by C3.

When V_{OUT} reaches its steady-state value, the IC is biased from the output through D3 diode. This external biasing can be applied as the 5 V output voltage is high enough to keep C3 voltage above the V_{CSon} threshold (max. value is V_{CSon_max} = 4.5 V). With this setting, the VCC voltage, during steady-state operation, is constant, the HV current source is never activated and very low input power consumption under light or no load conditions is possible (less than 16 mW at 230 V_{AC} under no load with an appropriate design) thanks to the low consumption of the IC internal blocks.

3 Schematic diagrams

Figure 3. **STEVAL-VP319X1B circuit schematic**



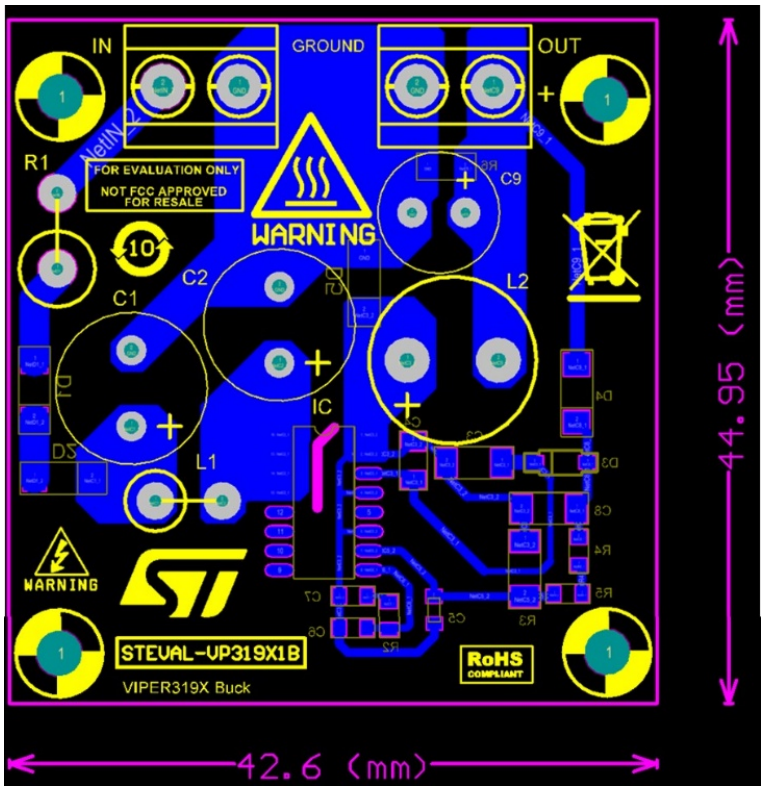
4 Bill of materials

Table 2. **STEVAL-VP319X1B bill of materials**

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
1	1	IN	l. 11.36mm - w. 10.0mm - d. 8.1mm - p. 5.08 mm 300 Vac 14 A	Through hole input connector	Wurth Elektronik	691213510002
2	1	OUT	l. 11.36mm - w. 10.0mm - d. 8.1mm - p. 5.08 mm 300 Vac 14 A	Through hole input connector	Wurth Elektronik	691213510002
3	1	D1	MRA4007T3G DO-214AC 1000 V 1 A	General purpose diode	ON Semiconductor	MRA4007T3G
4	1	D2	MRA4007T3G DO-214AC 1000 V 1 A	General purpose diode	ON Semiconductor	MRA4007T3G
5	1	D3	BAT46ZFILM SOD-123 100 V 0.15 A	General purpose signal Schottky diode	ST	BAT46ZFILM
6	1	D4	STTH1L06A SMA 600 V 1 A	Low drop ultra-fast diode	ST	STTH1L06A
7	1	D5	STTH1L06A SMA 600 V 1 A	Low drop ultra-fast diode	ST	STTH1L06A
8	1	R1	10 ohm through hole 1 W ±5%	Inrush resistor	TE Connectivity	ROX1SJ10R
9	1	R2	180 kohm 0603 0.1 W ±1%	SMD resistor	Vishay	CRCW0603180KFKEA
10	1	R3	22 kohm 1206 0.25 W ±1%	SMD resistor	Vishay	CRCW120622K0FKEA
11	1	R4	22 kohm 0603 0.1 W ±1%	SMD resistor	Vishay	CRCW060322K0FKEA
12	1	R5	56 kohm 0603 0.1 W ±1%	SMD resistor	Vishay	CRCW060356K0FKEA
13	1	R6	5.6 kohm 0805 0.125 W ±1%	SMD resistor	Vishay	CRCW08055K60FKEA
14	1	C1	10 µF through hole, d = 10 mm, p = 5 mm, h = 16 mm 400 Vcc ±20%	Electrolytic capacitor	Wurth Elektronik	860241375002
15	1	C2	10 µF through hole, d = 10mm, p = 5mm, h = 16mm 400Vcc ±20%	Electrolytic capacitor	Wurth Elektronik	860241375002
16	1	C3	4.7 µF 1206 50 Vcc ±10%	Multi-layer ceramic capacitor	Kemet	C1206C475K5PACTU
17	1	C4	100 pF 0805 50 Vcc ±10%	Multi-layer ceramic capacitor	Wurth Elektronik	885012207080
18	1	C5	Not connected	Capacitor	-	-
19	1	C6	330 pF 0603 50 Vcc ±10%	Multi-layer ceramic capacitor	Wurth Elektronik	885012206080
20	1	C7	22 nF 0603 50 Vcc ±10%	Multi-layer ceramic capacitor	Wurth Elektronik	885012206091
21	1	C8	220 nF 1206 50 Vcc ±10%	Multi-layer ceramic capacitor	Kemet	C1206C224K5RACTU
22	1	C9	680 µF through hole, d = 8 mm, p. = 3.5 mm; hole: 0.7 mm 10 Vcc ±20%	Electrolytic capacitor with ultra-low ESR	Rubycon	10ZLH680MEFC8X11.5
23	1	L1	1 mH through hole, 'Ø5.2 m - lungh. 14.8 mm 0.2 A ±5%	Small signal inductor	Epcos	B82144A2105J000
24	1	L2	270 µH t. h., d = 11mm, p = 6 mm, h = 11.5 mm, hole: 0.8 mm 1.3 A ±1%	Power inductor	Coilcraft	RFB1010-271L
25	1	IC1	VIPER319XDTR SO16N	Energy saving off-line high voltage converter	ST	VIPER319XDTR

5 Board layout

Figure 4. **STEVAL-VP319X1B evaluation board layout**



6 Testing the board

6.1 Typical waveforms

Figure 5. Voltage and current waveforms at 115 V_{AC} full load

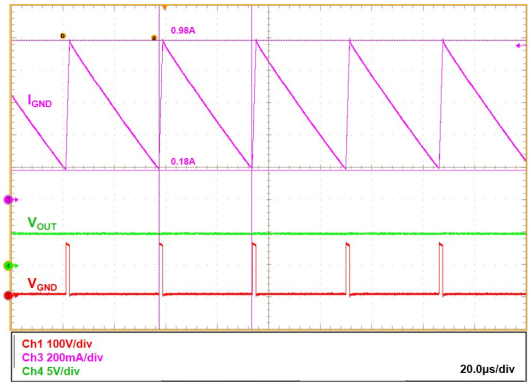


Figure 6. Voltage and current waveforms at 115 V_{AC} full load (zoom)

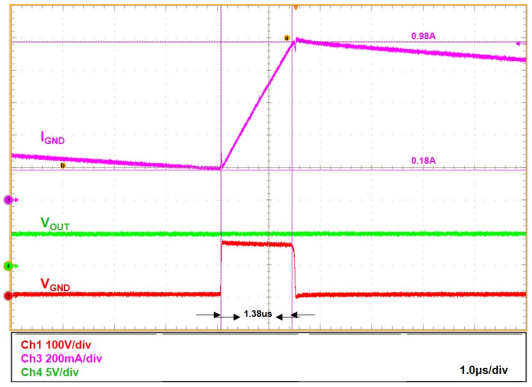


Figure 7. Voltage and current waveforms at 230 V_{AC} full load

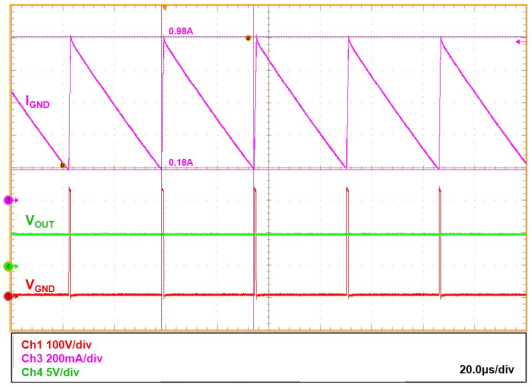
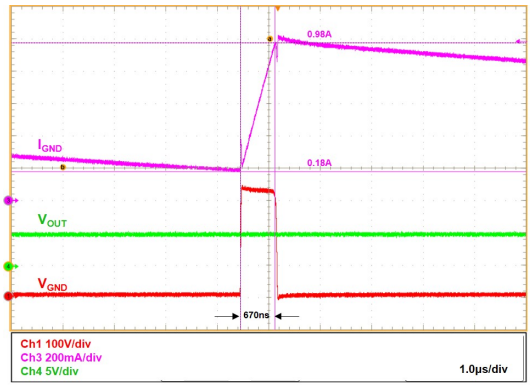


Figure 8. Voltage and current waveforms at 230 V_{AC} full load (zoom)



6.2 Line and load regulations

Figure 9. Line regulation

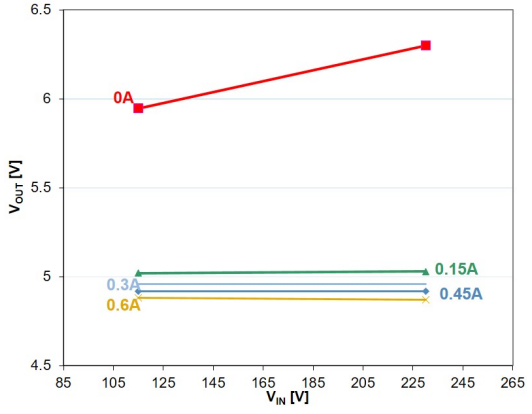
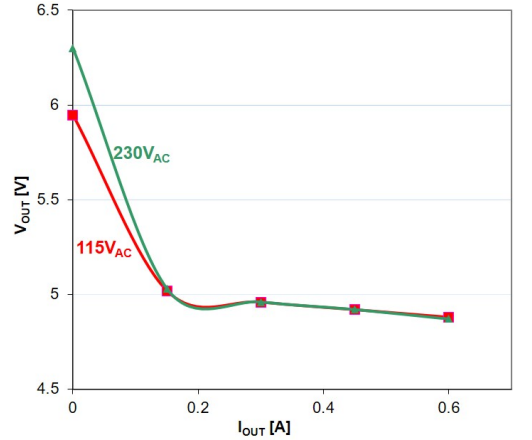


Figure 10. Load regulation



6.3 Efficiency

The active mode efficiency is defined as the average of the efficiency measured at 25%, 50%, 75% and 100% maximum load at V_{IN} = 115 V_{AC} and V_{IN} = 230 V_{AC} nominal input voltages.

External power supplies (contained in a separate housing from the end-use devices they are powering) need to comply with the Code of Conduct, version 5, "Active mode efficiency" criterion.

SMPSs with V_{OUT}< 6 V and I_{OUT} > 550 mA are classified as low voltage external power supplies: for a power throughput of 3.0 W, the CoC5 active mode efficiency requirement is 69.73%.

Another applicable standard is the Department of energy (DOE) requirement of 69.64% active mode efficiency for the same power throughput.

Table 3. Active mode efficiency demonstrates the STEVAL-VP319X1B complies with the above standards.

Table 3. Active mode efficiency

Regulation requirements (P_{OUTnom} = 3 W)		STEVAL-VP319X1B performance
CoC5 requirement	DOE requirement	
69.73%	69.64%	71.36% (at V_{IN} =115 V_{AC})
		69.81% (at V_{IN} = 230 V_{AC})

6.4 Light load performance

Another CoC5 efficiency requirement states that the output load is 10% of the nominal output power. The STEVAL-VP319X1B is compliant with this requirement, as shown in the table below.

Table 4. CoC5 requirement and STEVAL-VP319X1B performance at 10% output load

CoC5 efficiency requirements at P_{OUTnom}/10 (P_{OUTnom} = 3 W)	STEVAL-VP319X1B performance
60.58%	71.76% (at V_{IN} = 115 V_{AC})
	69.77% (at V_{IN} = 230 V_{AC})

Power consumption when the power supply is not loaded is also considered in CoC5. The compliance criteria for EPS converters with nominal output power below 49 W and the STEVAL-VP319X1B at no load input power consumption measurements (at nominal input voltages) are shown in the table below, demonstrating the evaluation board compliance with these requirements.

Table 5. CoC5 power consumption criteria for no load and STEVAL-VP319X1B performance

Max. consumption at no load (0.3W < Pno < 49W)	STEVAL-VP319X1B no load consumption
75 mW	12.7 mW (at V_{IN} = 115 V_{AC})
	15.6 mW (at V_{IN} = 230 V_{AC})

Depending on the equipment supplied, different criteria are taken into account when measuring a converter performance. In particular, under light load (EuP lot 6) the input power should be less than 500 mW when the converter is loaded with 250 mW.

The following table shows how the STEVAL-VP319X1B board satisfies this requirement, along with efficiency measurements for P_{OUT} = 25 mW and P_{OUT} = 50 mW under light load conditions.

Table 6. Light load performance

V_{IN}[V_{AC}]	Efficiency [%]		
	P_{OUT} = 25 mW	P_{OUT} = 50 mW	P_{OUT} = 250 mW
115	56.08	62.56	70.95

$V_{IN}[V_{AC}]$	Efficiency [%]		
	P_{OUT} = 25 mW	P_{OUT} = 50 mW	P_{OUT} = 250 mW
230	53.89	60.81	69.20

Another criterion is the output power (or efficiency) when the input power is equal to 1 W.

Table 7. Efficiency at P_{IN} = 1 W

V_{IN} [V_{AC}]	Efficiency at P_{IN} = 1 W [%]
115	73.36
230	71.00

7 Functional check

7.1 Start-up

An internal soft-start function progressively increases the cycle-by-cycle current limitation set point from zero to I_{DLIM} in 8 steps. This limits the drain current peak value during the output voltage rise, thus reducing the stress on the free-wheeling diode (D5).

The t_{SS} soft-start time needed for the current limitation to reach its final value is internally set at 8 ms. This function is activated for any converter start-up attempt or after a fault event. The IC pulse skipping feature skips a switching cycle whenever the OCP comparator is triggered within the minimum on-time. The switching frequency is thus halved down to the minimum allowed value of F_{OSC_MIN} (15 kHz, typ.). When the OCP comparator is not triggered inside the minimum on-time, a switching cycle is restored, doubling the switching frequency up to the nominal frequency F_{OSC}.

By allowing a longer inductor discharge time, this feature helps prevent current runaway, that is, the possible uncontrolled increase in drain current during the first cycle of the converter start-up, due to the initial inability of the system to maintain the volt-second balance when there is a large input-to-output voltage differential.

Figure 11. Start-up at V_{IN} = 115 V_{AC}, full load

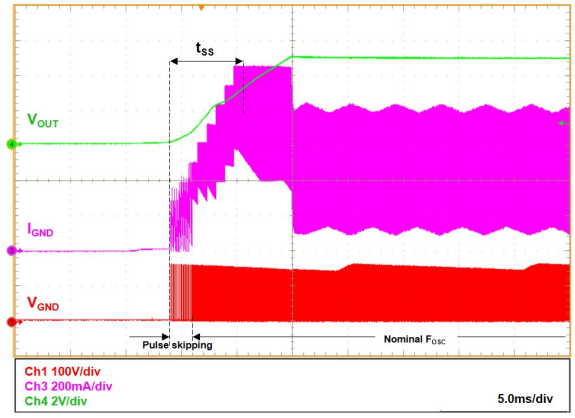
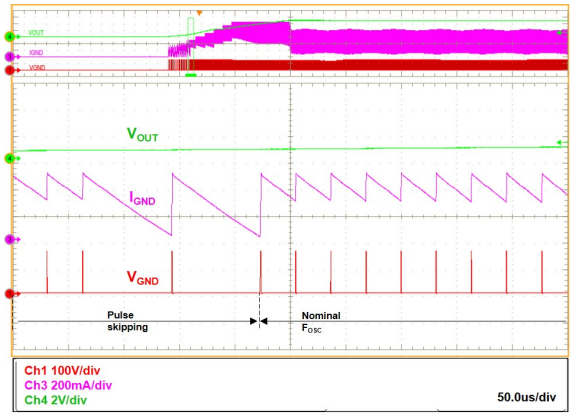


Figure 12. Start-up at V_{IN} = 115 V_{AC}, full load, zoom



Thanks to the pulse skipping feature, the maximum value reached by the peak current at start-up is quite low, even at 230 V_{AC}.

Figure 13. Start-up at V_{IN} = 230 V_{AC}, full load

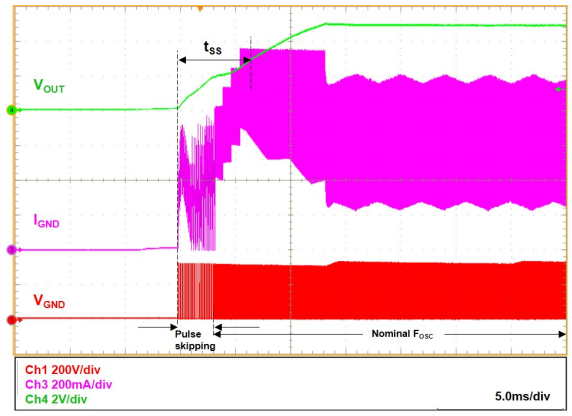
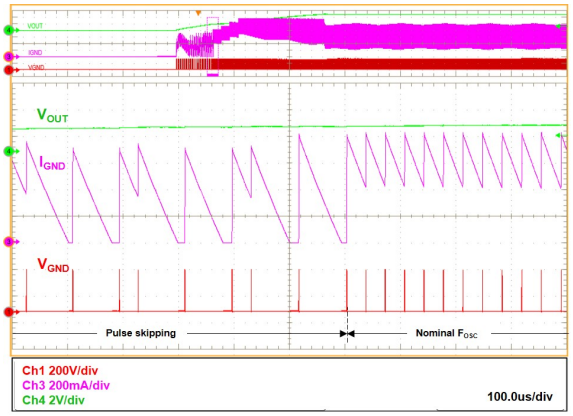


Figure 14. Start-up at V_{IN} = 230 V_{AC}, full load, zoom



7.2 Overload protection (OLP)

During an overload or short circuit, the drain current reaches I_{DLIM}. For every cycle during which this condition is met, an internal OCP counter is incremented. If the fault is maintained for t_{OVL} (50 ms typ., internally set), the VIPER31 is shut down for $t_{RESTART}$ (1 second, typ.) as shown in Figure 15. Output overload applied: OLP tripping. After this time, the IC resumes switching and, if the fault persists, the protection occurs indefinitely in the same way with the internal soft start-up function invoked at any restart (see Figure 16. Output overload maintained: OLP steady-state). This lowers the restart attempt rate to ensure safe operation with extremely low power throughput and to avoid IC overheating.

The IC resumes normal operation when the short is removed. If the fault is removed during t_{SS} or t_{OVL}, before protection tripping, the counter counts down each cycle to zero and the protection is not tripped. If the short circuit is removed during $t_{RESTART}$, the IC waits for the $t_{RESTART}$ period to elapse before resuming switching via soft start (Figure 17. Output overload removed: converter restarts).

Figure 15. Output overload applied: OLP tripping

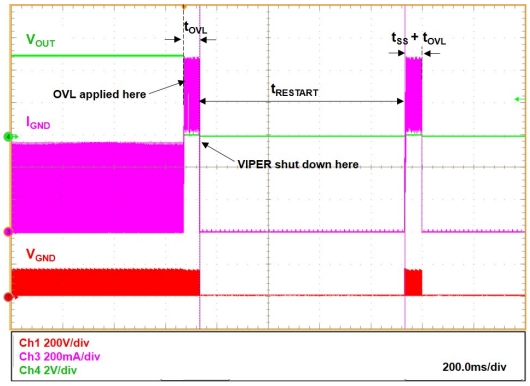


Figure 16. Output overload maintained: OLP steady-state

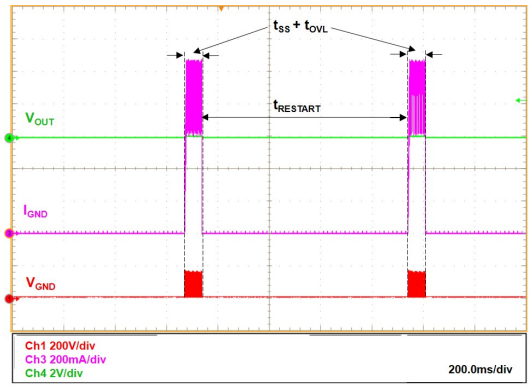
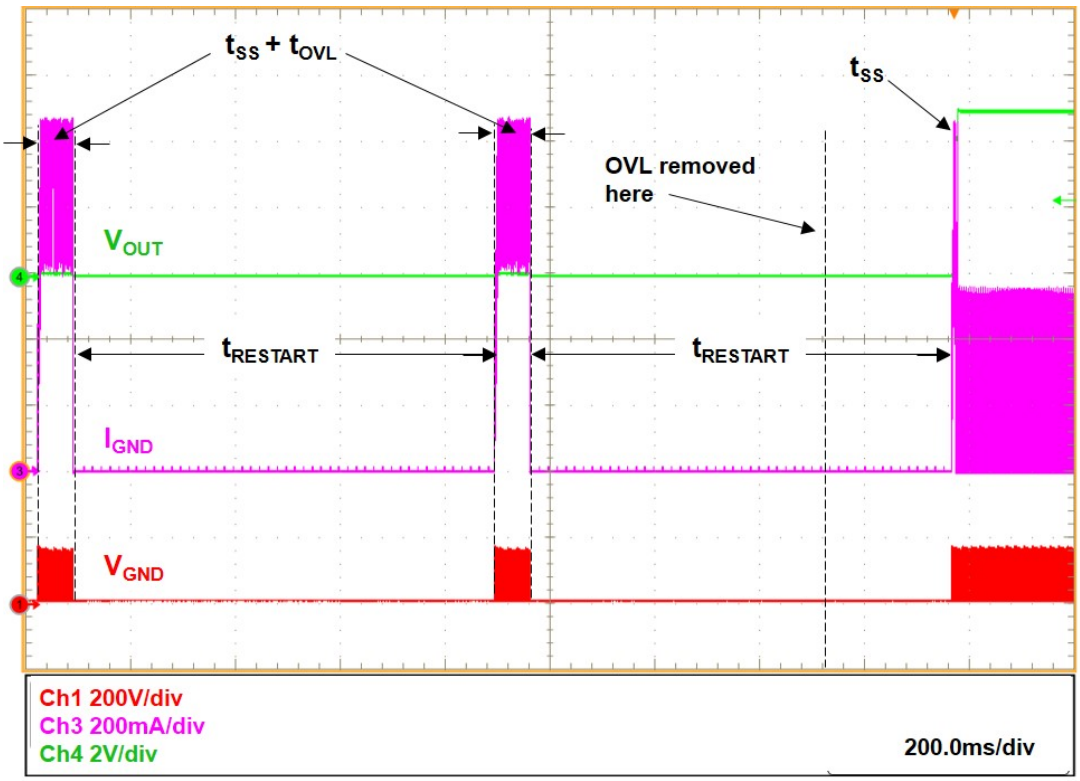


Figure 17. Output overload removed: converter restarts



During overload (especially at high V_{IN} when T_{on} is lower) the I_{DLIM} might be exceeded within the minimum ON time, causing the switching frequency to be reduced by the pulse skipping feature; consequently, the time needed for the OCP counter to reach its end of count might increase.

In particular, the actual value of t_{OVL} could vary between 50 msec (when pulse skipping is never invoked) and 100 msec (when pulse skipping is always invoked and the actual switching frequency is 15 kHz = $F_{OSC}/2$).

Figure 18. Output overload @ 230 V_{AC}: t_{OVL} increase

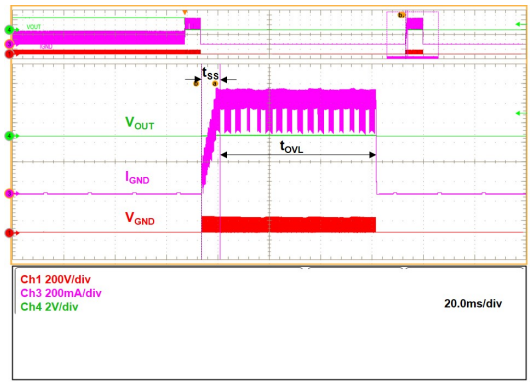
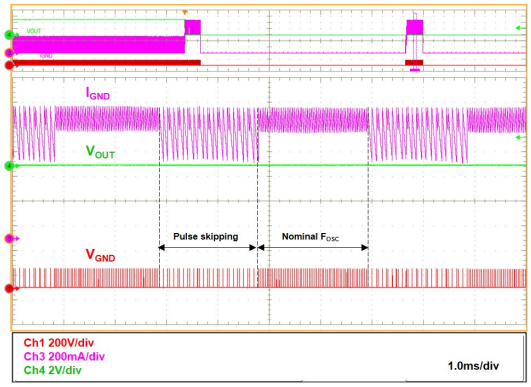


Figure 19. Output overload @ 230 V_{AC}: pulse skipping



8 Thermal measurements

The board thermal analysis has been performed using an IR camera at 85 V_{AC}, 115 V_{AC}, 230 V_{AC} and 265 V_{AC} mains input under full load condition. The results are shown in the following figures.

Note: In the bottom side views, A indicates the free-wheeling diode (D5), B indicates the VIPER31 and C indicates the input rectifiers (D1 and D2).

In top side views, A indicates the input resistor (R1) and B indicates the power inductor (L2).

Figure 20. Thermal measurements at V_{IN} = 85 V_{AC} full load (bottom view)

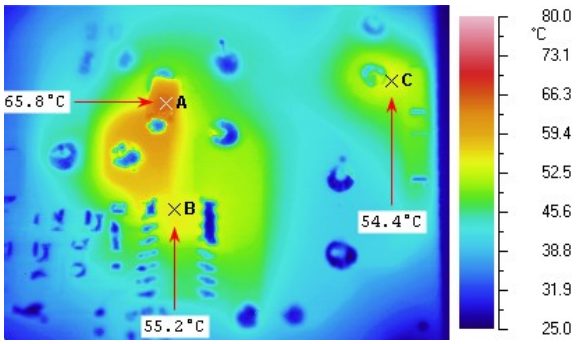


Figure 21. Thermal measurements at V_{IN} = 85 V_{AC} full load (top view)

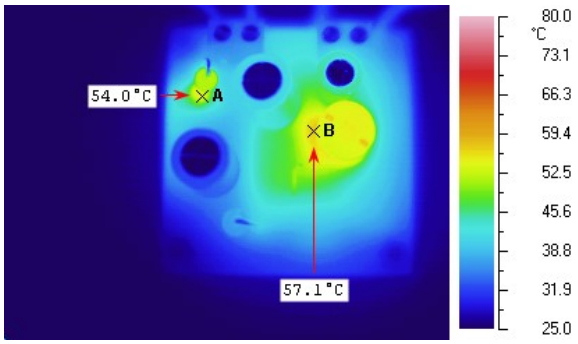


Figure 22. Thermal measurements at V_{IN} = 115 V_{AC} full load (bottom view)

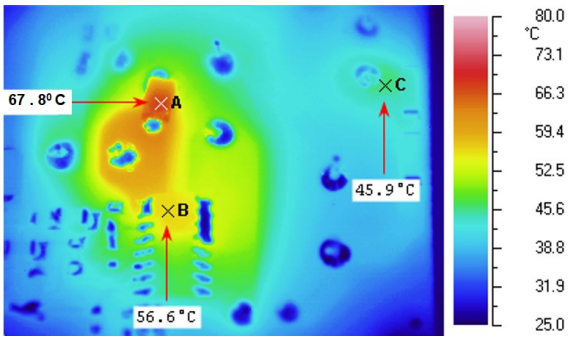


Figure 23. Thermal measurements at V_{IN} = 115 V_{AC} full load (top view)

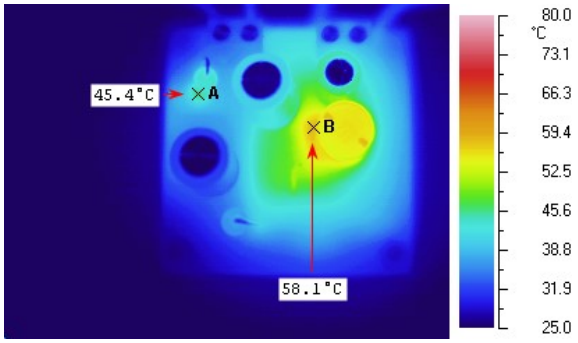


Figure 24. Thermal measurements at V_{IN} = 230 V_{AC} full load (bottom view)

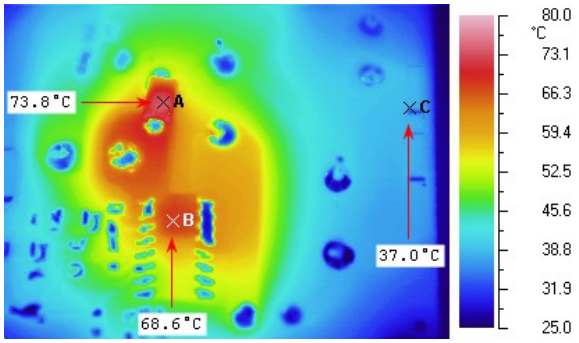


Figure 25. Thermal measurements at V_{IN} = 230 V_{AC} full load (top view)

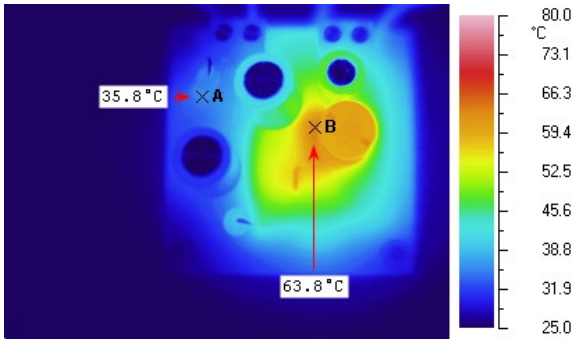


Figure 26. Thermal measurements at V_{IN} = 265 V_{AC} full load (bottom view)

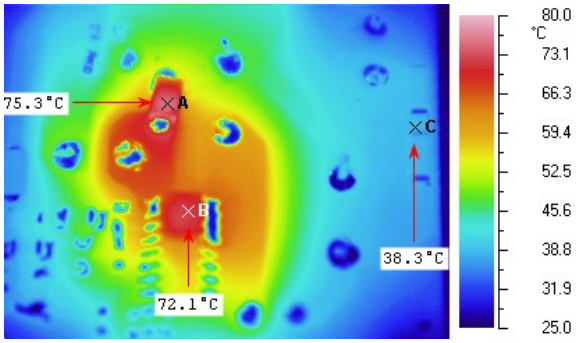
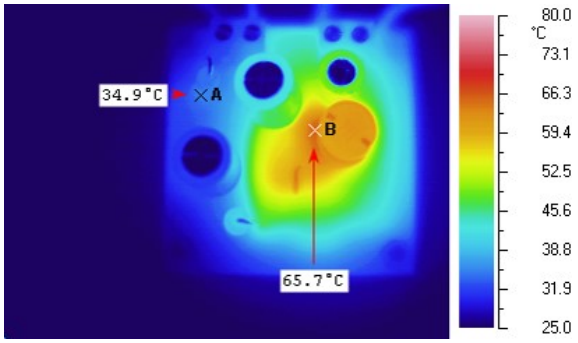


Figure 27. Thermal measurements at V_{IN} = 265 V_{AC} full load (top view)



9 EMI measurements

A pre-compliance test for European normative EN55022 (Class B) has been performed using an EMC analyzer with an average detector and a line impedance stabilization network (LISN).

Figure 28. EMI measurements with average detector at 115 V_{AC}, full load

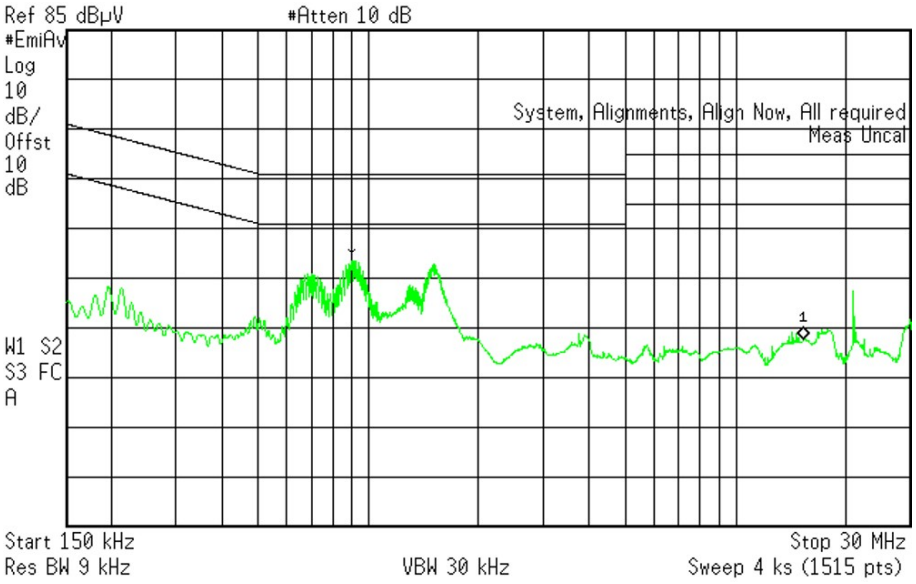
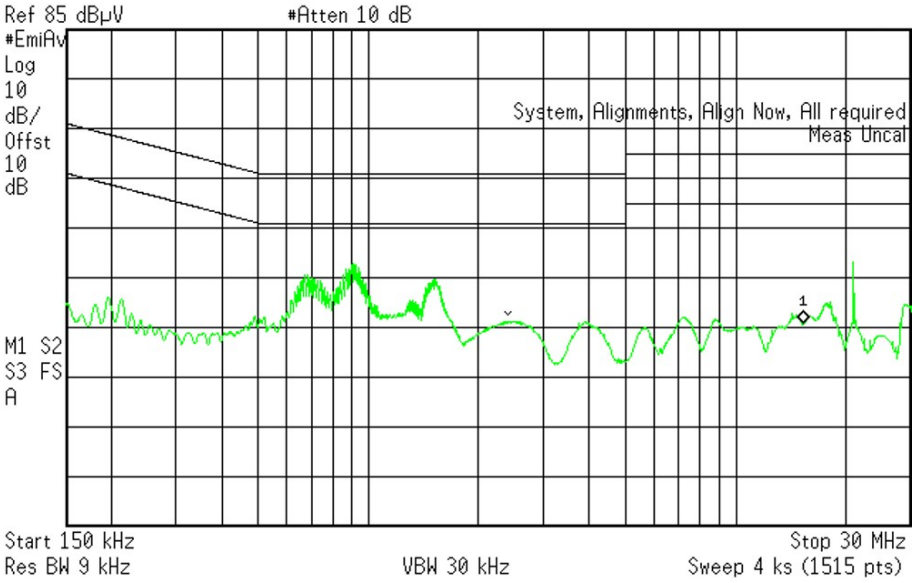


Figure 29. EMI measurements with average detector at 230 V_{AC}, full load



10 Extended input voltage range operation

By increasing the input capacitor size, the STEVAL-VP319X1B can supply nominal load starting from 40 V_{AC}.

To extend the input range, you have to modify the BoM and select part numbers with the same footprint of the original C1 and C2 components: 10 mm diameter and 5 mm lead spacing.

Table 8. STEVAL-VP319X1B BOM modification for extended range operation

Ref.	Description
C1	33 µF/400 V electrolytic capacitor
C2	33 µF/400 V electrolytic capacitor

The following figures show the typical waveforms and thermal measurements at full load with this modification applied.

Figure 30. Typical waveforms at 40 V_{AC}, full load

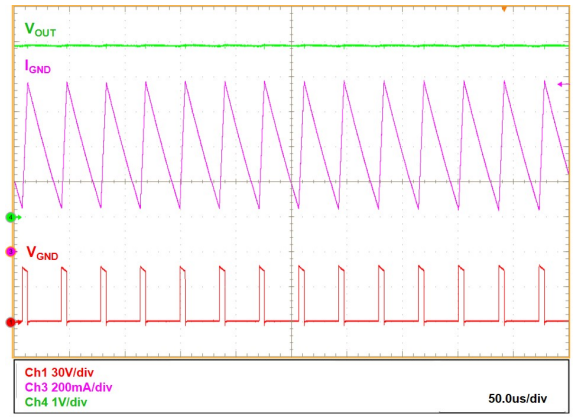


Figure 31. Typical waveforms at 40 V_{AC}, full load (zoom)

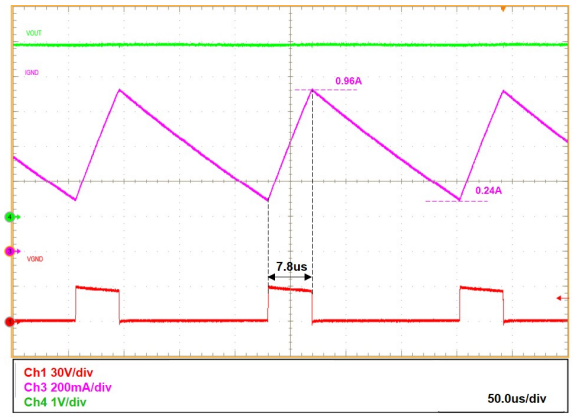


Figure 32. Thermal measurements at V_{IN} = 40 V_{AC} full load (bottom view)

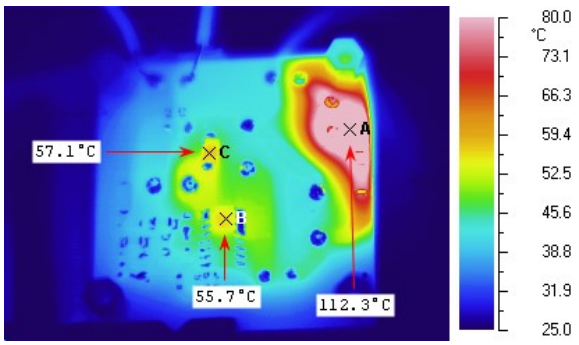
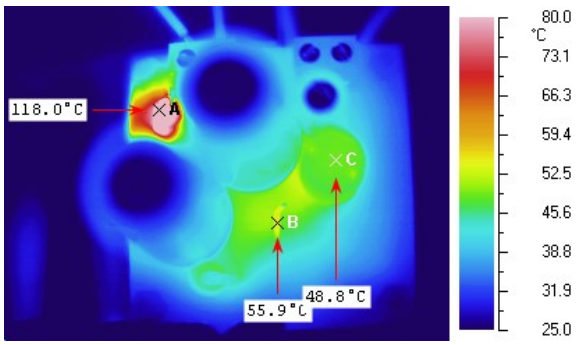


Figure 33. Thermal measurements at V_{IN} = 40 V_{AC} full load (top view)



11 Conclusions

The STEVAL-VP319X1B has been characterized demonstrating that VIPER31 allows designing, with few external components, an SMPS converter compliant with the most stringent energy regulations.

The STEVAL-VP319X1B consumes less than 16 mW at 230 V_{AC} mains under no load condition and can satisfy CoC5 and DOE requirements for active mode and light load efficiency for low power external power supplies.

By increasing the size of the input bulk capacitor, the board can supply the rated power starting from 40 V_{AC}.

The 800 V avalanche rugged power MOSFET and the embedded protections add reliability to the power converter, making VIPER31 the best choice for applications requiring robustness and energy efficiency.

Appendix A

A.1 CCM flyback converter transfer function

In control theory, the term "plant" stands for PWM modulator plus Power stage, and in the following equation, its transfer function (control-to-output) is indicated as *Gvc(s)*. In deep CCM, *Gvc(s)* can be described by the approximate expression:

$$G_{VC}(s) = H_0 \cdot \frac{1 + \frac{s}{\omega_{Z1}}}{1 + \frac{s}{\omega_{P1}}} \cdot G_{HF}(s) \quad (1)$$

$$G_{HF}(s) = \frac{1}{1 + \frac{s}{Q_O \cdot \omega_O} + \frac{s^2}{{\omega_O}^2}} \quad (2)$$

Gain pole and zero are defined below:

$$H_0 = \frac{R_0}{H_{COMP}} \cdot \frac{1}{1 + \frac{R_O \cdot T_S}{L} \cdot \left(0.5 - D\right)} \quad (3)$$

$$\omega_{Z1} = \frac{1}{R_C \cdot C_0} \quad (4)$$

$$\omega_{P1} \approx \frac{1}{R_0 \cdot C_0} + \frac{T_S}{L \cdot C_0} \cdot \left(0.5 - D\right) \quad (5)$$

$$\omega_O = \frac{\pi}{T_S} \quad (6)$$

$$Q_O = \frac{1}{\pi \cdot [0.5 - D]} \quad (7)$$

where:

$R_0 = V_{OUT}/I_{OUT}$ = nominal output resistance

$H_{COMP} = \Delta V_{COMP}/\Delta I_{DRAIN}$ (from the VIPER31 datasheet)

$T_S = 1/F_{OSC}$

C_0 = output capacitor capacitance

R_C = output capacitor ESR

D = converter duty cycle

L = primary inductance

A.2 Compensator design

A.2.1 Compensator transfer function

To compensate the CCM buck a type-2 compensator is used, whose transfer function has the following expression:

$$G_C(s) = G_{co} \cdot \frac{1 + \frac{S}{\omega_{ZC}}}{s \cdot \left(\frac{S}{\omega_{pc}}\right)} \quad (8)$$

It provides the integrator effect to ensure the high DC gain to minimize the static error, and a pole-zero pair, to boost the phase according to the phase margin target.

The synthesis of the compensator is done using a manual pole-zero placement technique, in which the zero is placed in the vicinity of the power stage dominant pole to cancel its effect and the pole position is adjusted to achieve the required phase margin.

The below step–by–step procedure can be followed to design the compensator:

Step 1. Select the crossover frequency f_C and the phase margin Φ_m.

Step 2. Evaluate the gain and phase of the plant at crossover frequency:

$$G_{vc(f_c)} = |G_{vc}(2 \cdot \pi \cdot f_c)| \tag{9}$$

$$\Phi_{vc(f_c)} = \arg[G_{vc}(2 \cdot \pi \cdot f_c)] \tag{10}$$

Step 3. The compensated open-loop gain must attain the unit gain at f_C, with the required phase margin, so the compensator must be designed to obtain the following gain and phase at f_C:

$$G_{c(f_c)} = \left|G_c(2 \cdot \pi \cdot f_c)\right| = \frac{1}{G_{vc(f_c)}} \tag{11}$$

$$\Phi_{c(f_c)} = \arg\left[G_c(2 \cdot \pi \cdot f_c)\right] = 90 - 180 + \Phi_m - \Phi_{vc(f_c)} \tag{12}$$

Step 4. Cancel the plant pole, $f_{P1} = \omega_{P1}/(2 \cdot \pi)$, by placing the zero of the compensator f_{zc} in the proximity ($\alpha = 1 \quad to \quad 5$).

$$f_{zc} = \frac{\omega_{zc}}{2 \cdot \pi} = \alpha \cdot f_{P1} \tag{13}$$

Step 5. Place the compensator pole to boost the phase and get the desired phase margin.

$$f_{pc} = \frac{f_c}{\tan\left[\tan^{-1}\left(\frac{f_c}{f_{zc}}\right) - \Phi_{c(f_c)}\right]} \tag{14}$$

Step 6. Calculate the gain G_{co}

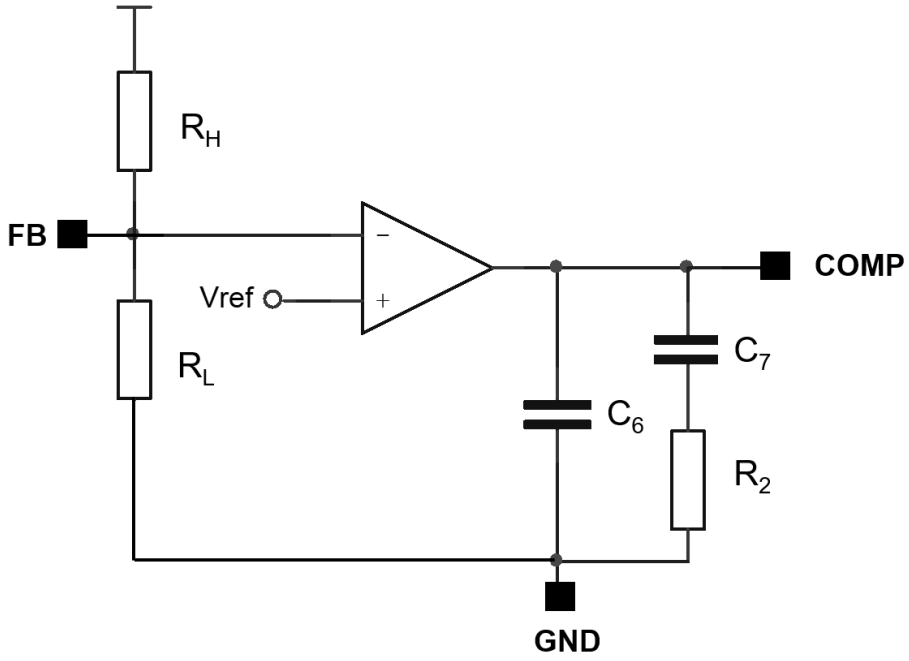
$$G_{co} = G_{c(fc)} \cdot \frac{\omega_c \cdot \sqrt{1 + \left(\frac{f_c}{f_{pc}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{zc}}\right)^2}} \tag{15}$$

The synthesis of $G_C(s)$ is completed.

A.2.2 Compensator network implementation

The figure below shows the compensation arrangement using a type-2 error amplifier with operational transconductance amplifier (OTA). The OTA output current is proportional to the differential input voltage, through the transconductance G_m (for its value, refer to the VIPER31 datasheet).

Figure 34. **Compensation network implementation with OTA**



The compensator transfer function has the following expression:

$$G_c(s) = \frac{R_L \cdot G_m}{(R_H + R_L) \cdot (C_6 + C_7)} \cdot \frac{1 + s \cdot R_2 \cdot C_7}{s \cdot \left[1 + s \cdot R_2 \cdot \left(\frac{C_6 \cdot C_7}{C_6 + C_7}\right)\right]} \quad (16)$$

Comparing Eq. (16) with Eq. (8), the compensator gain, pole and zero can be recognized as:

$$G_{co} = \frac{R_L \cdot G_m}{(R_H + R_L) \cdot (C_6 + C_7)} \quad (17)$$

$$f_{zc} = \frac{\omega_{zc}}{2 \cdot \pi} = \frac{1}{2 \cdot \pi \cdot R_2 \cdot C_7} \quad (18)$$

$$f_{pc} = \frac{\omega_{pc}}{2 \cdot \pi} = \frac{C_6 + C_7}{2 \cdot \pi \cdot C_6 \cdot C_7 \cdot R_2} \quad (19)$$

A.2.3 Compensator network calculation

To select each component:

Step 1. The high-side resistor of the voltage divider setting the output voltage, R_H is selected arbitrarily. Tens or hundreds kohms are suggested to reduce the voltage divider consumption.

Step 2. The low-side resistor R_L is calculated as follows:

$$R_L = \frac{V_{FB\_REF}}{V_{OUT} - V_{FB\_REF}} \cdot R_H \quad (20)$$

Where V_{FB_REF} (1.2 V, typ.) is the reference voltage of the VIPER31 internal error amplifier.

Step 3. Divide Eq. (18) by Eq. (19) to obtain:

$$\frac{f_{zc}}{f_{pc}} = \frac{C_6}{C_6 + C_7} \quad (21)$$

Step 4. Combine Eq. (21) with Eq. (17)

$$C_6 = \frac{f_{zc}}{f_{pc}} \cdot \frac{R_L \cdot G_m}{(R_H + R_L) \cdot G_{co}} \quad (22)$$

Step 5. Get C_7 from Eq. (17).

$$C_7 = \frac{R_L \cdot G_m}{(R_H + R_L) \cdot G_{co}} - C_6 \quad (23)$$

Real OTA should include output resistor R_{ea} and output capacitor C_{ea} to modify the transfer function from what expressed in Eq. (8) and Eq. (16). But, R_{ea} is actually in the range of several Mohms and can be neglected. With this approximation, C_{ea} can be considered in parallel with C_6 and modification of Eq. (16) simply consists in replacing C_6 with $C_6 + C_{ea}$.
Eq. (22) and Eq. (23) can be rewritten as follows:

$$C_6 = \frac{f_{zc}}{f_{pc}} \cdot \frac{R_L \cdot G_m}{(R_H + R_L) \cdot G_{co}} - C_{ea} \quad (24)$$

$$C_7 = \frac{R_L \cdot G_m}{(R_H + R_L) \cdot G_{co}} - (C_6 + C_{ea}) \quad (25)$$

Step 6. Calculate R_2 from Eq. (18).

$$R_2 = \frac{1}{2 \cdot \pi \cdot f_{zc} \cdot C_7} \quad (26)$$

For STEVAL-VP319X1B, the phase margin is set at 76^0 (high enough for stability) and the crossover frequency at 1.4 kHz, which limits to an acceptable value the output voltage undershoot following a step load change.
With reference to Section 3: Schematic diagrams, R_H = R4 + R5 (its selection is 78 kohm), and R_L = R3. C_{ea} value is 10 pF.

Table 9. Synthesis of the compensator

Part	Ref. equation	Theoretical value	Selected value
R_L	$R_L = \frac{V_{FB\_REF}}{V_{OUT} - V_{FB\_REF}} \cdot R_H$	24 kohm	22 kohm
C_6	$C_6 = \frac{f_{zc}}{f_{pc}} \cdot \frac{R_L \cdot G_m}{(R_H + R_L) \cdot G_{co}} - C_{ea}$	319 nF	330 nF
C_7	$C_7 = \frac{R_L \cdot G_m}{(R_H + R_L) \cdot G_{co}} - (C_6 + C_{ea})$	21.5 nF	22 nF
R_2	$R_2 = \frac{1}{2 \cdot \pi \cdot f_{zc} \cdot C_7}$	177 kohm	180 kohm

The resulting crossover frequency f_C and phase margin Φ_m are in line with the targets:

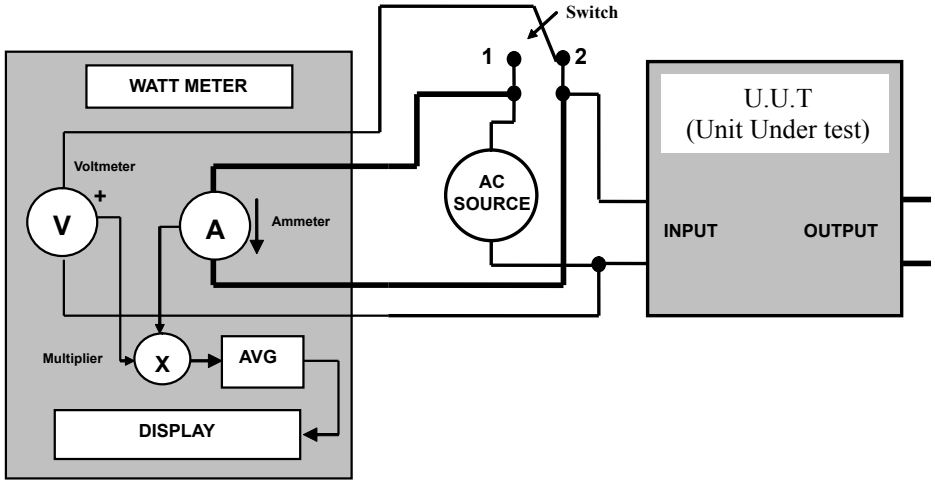
- f_C = 1.2 kHz
- $\Phi_m = 74.9^0$

Appendix B Test equipment and measurement of efficiency and light load performance

The converter input power is measured by a wattmeter, which simultaneously measures the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The digital wattmeter samples the current and voltage, converts them in digital formats, which are then multiplied to obtain the instantaneous measured power. The sampling frequency is in the range of 20 kHz or higher. The average measured power over a short interval (1 s typ.) is displayed.

The following figure shows the wattmeter connection to the UUT (unit under test) and AC source, as well as the wattmeter internal block diagram.

Figure 35. Connections of the UUT to the wattmeter for power measurements



An electronic load is connected to the output of the power converter (UUT), allowing the converter load current to be set and measured, while the output voltage is measured by a voltmeter. The output power is the product of load current and output voltage.

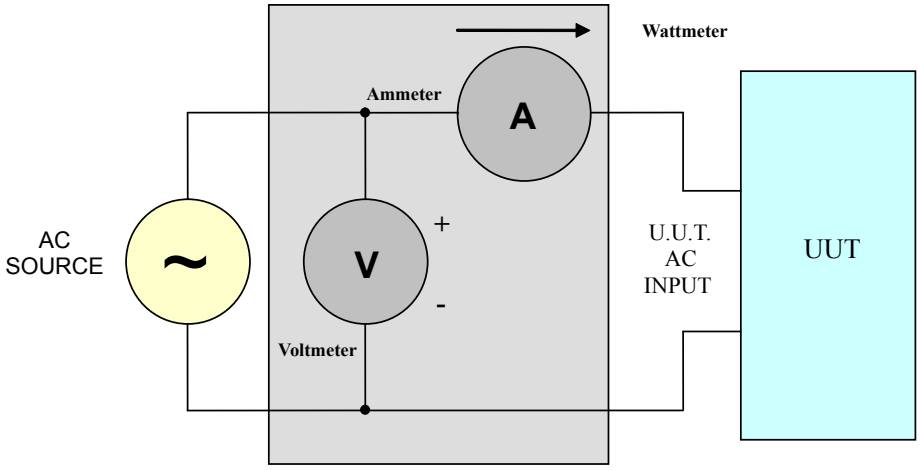
The ratio between the above output power calculation and the input power measured by the wattmeter indicates the converter efficiency, measured under different input/output conditions.

B.1 Considerations when measuring input power

With reference to Figure 35. Connections of the UUT to the wattmeter for power measurements, the UUT input current causes a voltage drop across the ammeter internal shunt resistance and across the cables connecting the wattmeter to the UUT.

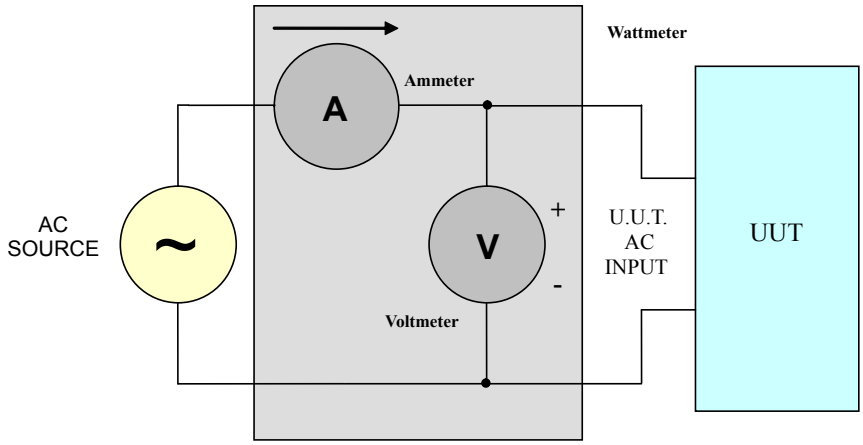
If the switch in Figure 35. Connections of the UUT to the wattmeter for power measurements is in position 1 (see the simplified schematic below) this voltage drop causes an input measured voltage higher than the input voltage at the UUT input, which distorts the measured power. The voltage drop is generally negligible if the UUT input current is low (e.g., the input power of UUT under low load condition).

Figure 36. **Switch in position 1 - setting for standby measurements**



For high UUT input currents (e.g., heavy load conditions), the voltage drop compared to the UUT real input voltage can become significant. In this case, the switch in Figure 35. Connections of the UUT to the wattmeter for power measurements should be set to position 2 (see the simplified schematic below), where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

Figure 37. **Switch in position 2 - setting for efficiency measurements**



However, the setting shown in Figure 37. Switch in position 2 - setting for efficiency measurements might cause a relevant error during light load measurements, when the UUT input current is low and the leakage current inside the voltmeter is not negligible. Then, the settings shown in Figure 36 are recommended for light load measurements and the settings shown in Figure 37 are recommended for heavy loads.

You can try both settings to choose the lower input power value.

As stated in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT should operate at 100% of the nameplate output current output for at least 30 minutes (warm-up period) before measuring efficiency.

After this warm-up period, the AC input power has to be monitored for 5 minutes to assess the stability of the UUT:

- if the power level does not drift by more than 5% from the maximum value observed, the UUT can be considered stable and the measurements can be recorded
- if the AC input power is not stable, the average power or accumulated energy has to be measured for AC input and DC output

Some wattmeters allow integrating the measured input power over a time range and measuring the energy absorbed by the UUT during the integration time. The average input power is obtained by dividing by the integration time itself.

Revision history

Table 10. **Document revision history**

Date	Version	Changes
15-Sep-2020	1	Initial release.
31-Mar-2025	2	Updated Introduction, Section 4: Bill of materials, Section 7.2: Overload protection (OLP), Appendix A.1: CCM flyback converter transfer function , Appendix A.2.1: Compensator transfer function, Appendix A.2.2: Compensator network implementation and Appendix A.2.3: Compensator network calculation.

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