Introduction

The aim of this document is to clarify the usage and features of the SAR ADC found inside the chips in the SPC58 family, and help the user to design the external components to achieve the desired level of precision of the sampled signals.

In particular, it is important to reject as much noise as possible from the reference voltage, as its variations will directly affect the accuracy of the conversion.

The accuracy of the conversion is usually measured in LSBs, which is the highest order bit that is different from the actual value. For example, if the “real” value were 10010100 but an error caused it to be measured as 10010000, we would have an error of 3 LSBs, since the error involves the third least significant bit.
1 SAR ADC Characteristics

The SAR ADC device includes two kind of converters:

• A fast ADC (SAR ADC)
• A slow ADC (SARB ADC)

All analog input pins routed to either type of ADC are multiplexed with a dual analog input switch pad cell. Simultaneous sampling by two converters on the same analog input is not allowed. Figure 1 shows the internal SAR ADC block diagram.

This is a summary of the most relevant features of the SAR ADC IP:

• 12 bit resolution
• Reference voltage: from 2.0 V to 6.0 V
• Supply voltage: from 3.5 V to 5.5 V
• Maximum clock frequency: 14.4 MHz
• Programmable sampling time
• Software controlled power-down

Please refer to the SoC datasheet for detailed features.
To preserve the accuracy of the ADC, it is necessary that the analog input pins have a low AC impedance. A large capacitor $C_F$ with good high frequency characteristics at the input pin of the device contributes to attenuating the noise on the signal to sample, and the charge it accumulates will charge the ADC internal capacitor during the sampling phase.

However, this high impedance can limit the ADC sampling rate. A current limiter resistance $R_L$ is usually necessary after the RC filter, to control the current spike when the sampling phase begins, and its value will affect the maximum sampling rate, too.

Figure 2 shows a typical input network and the input equivalent circuit of a SAR ADC channel.

**Figure 2. External network and input equivalent circuit (fast SARn channels)**

$C_S$ is the sampling capacitance, and $C_{P1}$ and $C_{P2}$ are the two contributions of the pin capacitance. The value for these equivalent capacitors is given in the SoC data sheet. $R_S$ is the series resistance of the input signal and is usually outside of the designer’s control. $R_F$ is the parasitic resistance of the input capacitor $C_F$, which acts as an RC filter.

### 2.1 Design of the current limiter

The sampling capacitor $C_S$ can be modeled as a switching current sink element. Its capacitive reactance at a given conversion frequency $f_C$ is:

$$R_{eq} = \frac{1}{2\pi f_C C_S}$$ (1)

The sampled voltage will be partitioned between $R_{eq}$ and the series of $R_S$ and $R_F$. The error in the acquisition will be negligible if the voltage drop is within half a LSB:

$$\frac{R_S + R_F}{R_{eq}} < \frac{1}{2} \text{ LSB}$$ (2)

Considering that, for a 12 bit converter, 1 LSB is $\frac{1}{2^{12}}$, that formula yields:

$$R_S + R_F < \frac{R_{eq}}{2 \cdot 2^{12}} = \frac{1}{8192 \cdot 2\pi f_C C_S}$$ (3)

This equation provides a design constraint on the filter resistance. For example, using the values given on the data sheet ($f_C = 400$ KHz, $C_S = 5$ pF), and assuming that the intrinsic series resistance of the signal to convert is known:

$$R_S + R_F < \frac{1}{8192 \cdot 2\pi \cdot 4 \cdot 10^{-5} \cdot 5 \cdot 10^{-12}} = 9.7 \Omega$$ (4)
2.2 Transient analysis

\( C_F \) and \( R_L \) are involved in the transient of the internal voltage, so must be designed to minimize the impact of second order effects on the precision of the measure. Once the sampling switch is closed, the voltage at the pin \( V_{IN} \) will have the following evolution:

\[ V_A \]

\[ V_1 \]

\[ V_2 \]

\[ \tau_1 \]

\[ \tau_2 \]

\( V_A \) is the voltage present at the input, before the RC filter. Two transient phases occur before the voltage becomes stable. A proper design of the external components will make sure that the transient is fast and the sampled value accurate.

At the beginning of the transition, the channel selection switch is closed and the sampling switch is open. This means that \( C_F, C_{P1} \) and \( C_{P2} \) are charged to the value to sample \( V_A \), and \( C_S \) is completely discharged. Immediately after the sampling switch is closed, charge flows from \( C_{P1} + C_{P2} \) to \( C_S \). The local circuit can be simplified as follows:

\[ V_A \cdot (C_{P1} + C_{P2}) = V_1 \cdot (C_S + C_{P1} + C_{P2}) \quad (5) \]

This is an RC circuit, where the \( R \) is the series of the resistance of the channel selection and sampling switch (indicated as \( R_{CS} \) and \( R_{SW} \), respectively), and the \( C \) is the series between \( C_S \) and the parallel between \( C_{P1} \) and \( C_{P2} \). This means that the time constant of this transient is:
\[
\tau_1 = \left( R_{CS} + R_{SW} \right) \cdot \frac{C_S \cdot (C_{P1} + C_{P2})}{C_S + C_{P1} + C_{P2}} \tag{6}
\]

All the symbols in the last two equations are known parameters that can be found in the data sheet, so \( V_1 \) and \( \tau_1 \) have the following values:

\[
V_1 = 0.69 \cdot V_A \tau_1 = 9 \text{ ns}
\]

The value of \( \tau_1 \) indicates that the first transient is very fast. After it is done, charge starts flowing from \( C_F \) (that is typically bigger than the on-chip capacitance, and for this reason is considered a voltage source during this analysis) through \( R_L \). The time constant of this second transient is:

\[
\tau_2 = R_L \cdot (C_S + C_{P1} + C_{P2}) \tag{7}
\]

This transient depends from the current limiting resistor chosen, and places a restriction on its value, since should be sensibly shorter than the sampling time – not greater that one tenth of it, maximum.

Now we can determine the value of the voltage at the end of the second transient, which is the one that will actually be sampled. The difference between this value and \( V_A \) (the “real” value under measure) is the error introduced by the external network.

The charge \( Q_2 \) at the end of the second transient must be the same to the sum of the charge \( Q_F \) that was on \( C_F \) and the charge \( Q_S \) on \( C_{P1} + C_{P2} + C_S \) at the end of the first transient:

\[
\begin{align*}
Q_2 &= V_2 \cdot (C_F + C_S + C_{P1} + C_{P2}) \\
Q_F &= V_A \cdot C_F \\
Q_S &= V_1 \cdot (C_S + C_{P1} + C_{P2}) \\
Q_2 &= Q_F + Q_S \Rightarrow V_2 \cdot (C_F + C_S + C_{P1} + C_{P2}) &= V_A \cdot C_F + V_1 \cdot (C_S + C_{P1} + C_{P2}) \tag{8}
\end{align*}
\]

After replacing the value we found for \( V_1 \), the following equation can be used to determine \( V_2 \), that is the final voltage that will be sampled by the ADC:

\[
\begin{align*}
V_2 \cdot (C_F + C_S + C_{P1} + C_{P2}) &= V_A \cdot C_S + C_{P1} + C_{P2} \\
V_2 &= \frac{V_A \cdot (C_{P1} + C_{P2})}{(C_F + C_S + C_{P1} + C_{P2})} \\
V_2 \cdot (C_F + C_S + C_{P1} + C_{P2}) &= V_A \cdot (C_F + C_{P1} + C_{P2}) \tag{9}
\end{align*}
\]

The error is negligible if the voltage drop is within half a LSB:

\[
1 - \frac{V_2}{V_A} < \frac{1}{2} \text{ LSB} \tag{10}
\]

Solving the equation for \( C_F \) will provide a design constraint that must be obeyed to preserve the accuracy of the conversion:

\[
1 - \frac{C_F + C_{P1} + C_{P2}}{C_F + C_S + C_{P1} + C_{P2}} = \frac{C_F + C_S + C_{P1} + C_{P2} - C_F - C_{P1} - C_{P2}}{C_F + C_S + C_{P1} + C_{P2}} = \frac{C_S}{C_F + C_S + C_{P1} + C_{P2}} < \frac{1}{2} \text{ LSB} \tag{11}
\]

For a 12 bit converter, 1 LSB is \( \frac{1}{2^{12}} \), so that formula yields:

\[
C_S < \frac{C_F}{2^{13}} + \frac{C_S}{2^{13}} + \frac{C_{P1}}{2^{13}} + \frac{C_{P2}}{2^{13}} \Rightarrow C_F > 8192 \cdot C_S \tag{12}
\]
3 Reference voltage filtering

Filtering as much noise as possible from the reference voltage is paramount, as any variation in its value will be reflected in the conversion error. However, the series resistance of the filter will cause a drop in the voltage fed to the $V_{REF}$ pin of the SoC, which will in turn affect the conversion result.

This drop is not constant, as it depends from the current absorbed by the converters being used. The maximum current absorbed by each conversion is given in the data sheet:

<table>
<thead>
<tr>
<th>Symbol</th>
<th>C</th>
<th>ParameterConditions</th>
<th>Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{ADCREFH}$</td>
<td>CC</td>
<td>T</td>
<td>ADC high reference current (12 bit)</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>CC</td>
<td>T</td>
<td>ADC high reference current (10 bit)</td>
<td>1</td>
</tr>
</tbody>
</table>

For example, assume a design that uses four 12 bit ADC for sampling and two 10 bit in comparator mode, and a filter resistance of 47 Ω. The voltage drop due to the filter resistance will be equal to:

$$\Delta V = R \cdot \left(4I_S + 2I_C\right) = 47 \Omega \cdot \left(4 \cdot 7 \mu A + 2 \cdot 19.5 \mu A\right) = 3.15 \text{ mV}$$

(16)

Where $I_S$ is the sampling current and $I_C$ is the comparator current. Assuming a 5 V reference and considering the 12 bit ADC, a voltage drop of 3.15 mV causes an error approximately equal to 2.5 LSB, since an error of 1 LSB on a value of 5 V is equal to $5 \cdot \frac{1}{2^{12}} = 1.22 \text{ mV}$. The system designer needs to evaluate whether this error is acceptable or not. If it isn’t, the resistance can be reduced and the capacitance increased.

The final circuit will look like this:
Figure 5. Final circuit

Source

Input Filter

Limiter

5 V or 3.3 V Power Supply

Input Signal

R_s

R_f

R_l

V_in

V_DD_HV_ADR

Microcontroller

Supply Filter

5 V or 3.3 V Reference Voltage

R_ADR

C_f

2.2 µF

G_ADR

220 nF

Decoupling Capacitors

V_DD_HV_ADR_S
Appendix A

A.1 Acronyms and abbreviations

Table 2. Acronyms

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Complete name</th>
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<tbody>
<tr>
<td>MAC</td>
<td>Medium Access Control</td>
</tr>
<tr>
<td>WOL</td>
<td>Wake-up On LAN</td>
</tr>
<tr>
<td>PMT</td>
<td>Power Management</td>
</tr>
<tr>
<td>CLI</td>
<td>Command line interface</td>
</tr>
<tr>
<td>MII</td>
<td>Media Independent Interface</td>
</tr>
<tr>
<td>DMA</td>
<td>Direct memory address</td>
</tr>
<tr>
<td>MTL</td>
<td>MAC transaction layer</td>
</tr>
<tr>
<td>ISR</td>
<td>Interrupt service routine</td>
</tr>
<tr>
<td>MCU</td>
<td>Micro-Controller Unit</td>
</tr>
</tbody>
</table>

A.2 Reference documents

• RM0407 Reference manual
• OPEN Sleep/Wake-up Specification
• TN1271 Technical note SPC58xB/C/G Low Power Modes
• TN1305 Technical note Network Management Interfaces
Revision history

Table 3. Document revision history

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<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>06-Oct-2020</td>
<td>1</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
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