Application note

STEVAL-USBPD27S performance

Introduction

The STEVAL-USBPD27S reference design performance results are described herein, based on functional check and several lab tests including specific USB PD compliance tests.

Tests have been carried out to demonstrate the robustness and reliability of the power supply stage, the compliance with USB Type-C and USB Power Delivery specifications, the compliance with CoC - Tier 2 and DOE Efficiency Requirement for power supplies and the compliance with the EN55022 (Class B) standard for conducted noise emissions.

1 Power supply typical waveforms

1.1 Startup

The converter startup phase is shown in the following figures at 115 and 230 V_{AC} under no load and full load conditions.

The output voltage starts increasing after a short delay from the presence of the input voltage (< 250 ms). No abnormal oscillation is present in the output.

In figures Figure 1, Figure 2, Figure 3 and Figure 4:

- blue = V_{IN} 100 V/div
- green = V_{OUT} 2.5 V/div
- yellow = I_{OUT} 2.5 A/div

Figure 1. Startup at 90 V_{AC}, out 5 V, no load

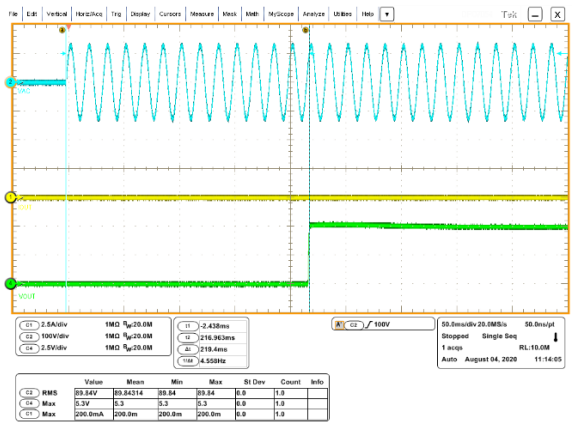


Figure 2. Startup at 90 V_{AC}, out 5 V, 5 A

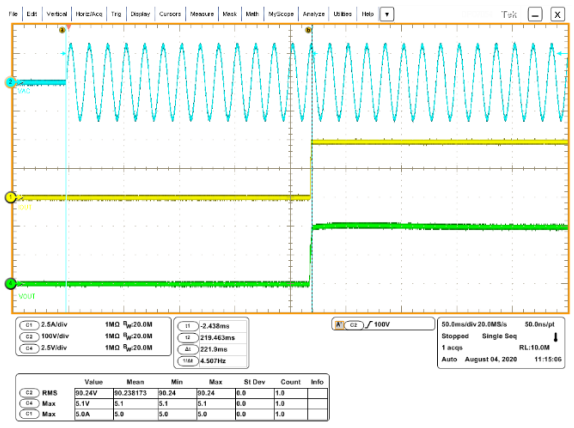


Figure 3. Startup at 115 V_{AC}, out 5 V, no load

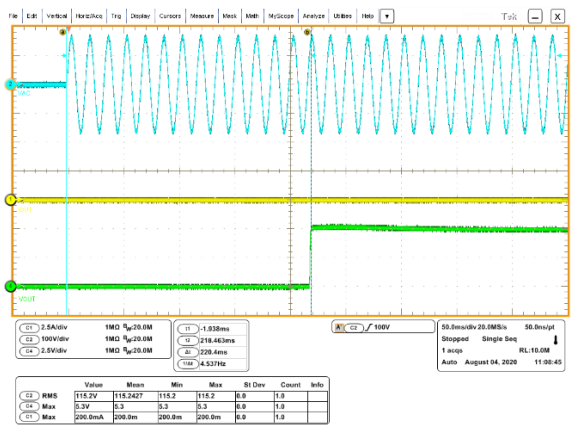
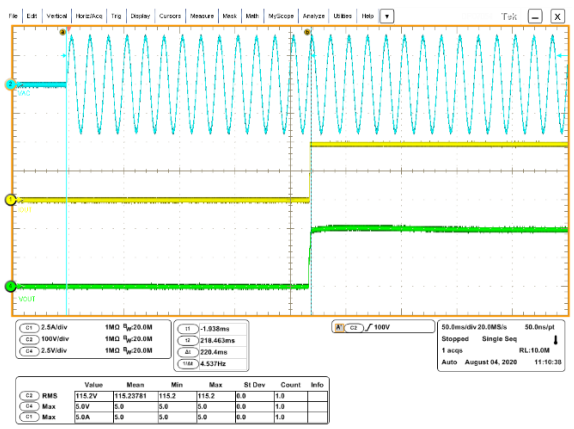


Figure 4. Startup at 115 V_{AC}, out 5 V, 5 A



In figures Figure 5, Figure 6, Figure 7 and Figure 8:

- blue = V_{IN} 300 V/div
- green = V_{OUT} 2.5 V/div
- yellow = I_{OUT} 2.5 A/div

Figure 5. Startup at 230 V_{AC}, out 5 V, no load

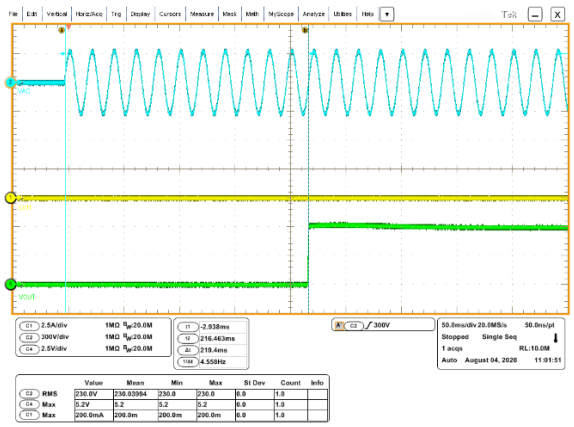


Figure 6. Startup at 230 V_{AC}, out 5 V, 5 A

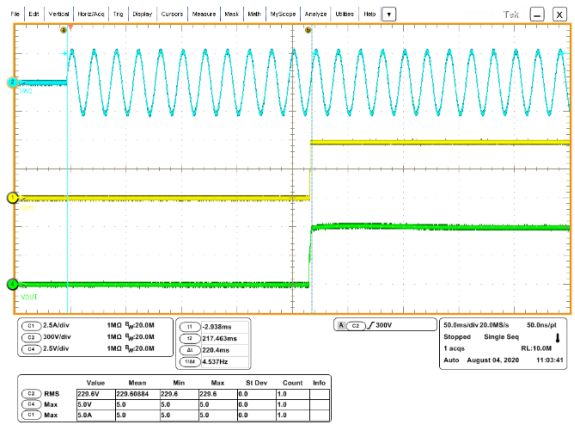


Figure 7. Startup at 265 V_{AC}, out 5 V, no load

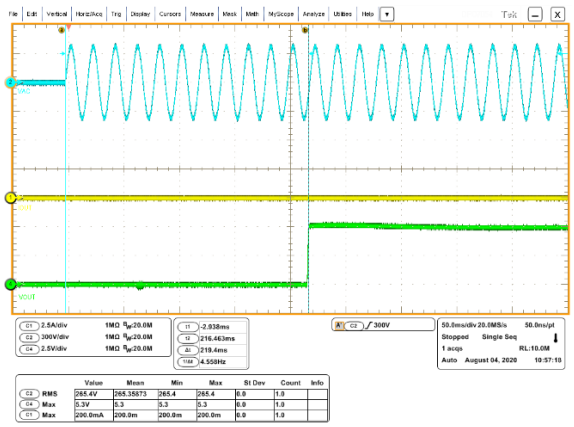
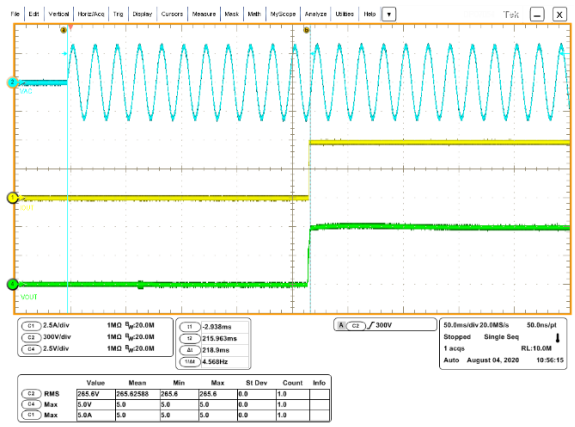


Figure 8. Startup at 265 V_{AC}, out 5 V, 5 A



1.2 Output voltage regulation for dynamic load variation

The following figures show the load transient response waveforms of the flyback converter when subjected to repetitive dynamic load transitions (zero to full load at 115 and 230 V_{AC}).

There is no abnormal oscillation in the output and the overshoot and undershoot values are acceptable.

In figures Figure 9 and Figure 10:

- green = V_{OUT} 400 mV/div
- yellow = I_{OUT} 1 A/div

Figure 9. Dynamic load at 3.3 V/5 A, V_{IN} = 115 V_{AC}

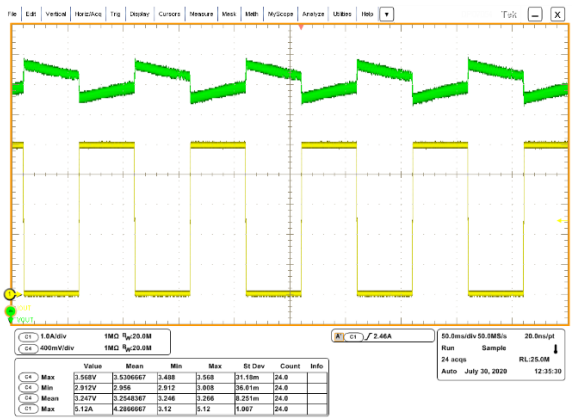
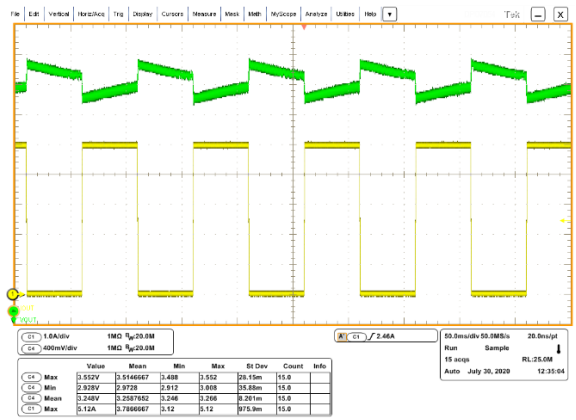


Figure 10. Dynamic load at 3.3 V/5 A, V_{IN} = 230 V_{AC}

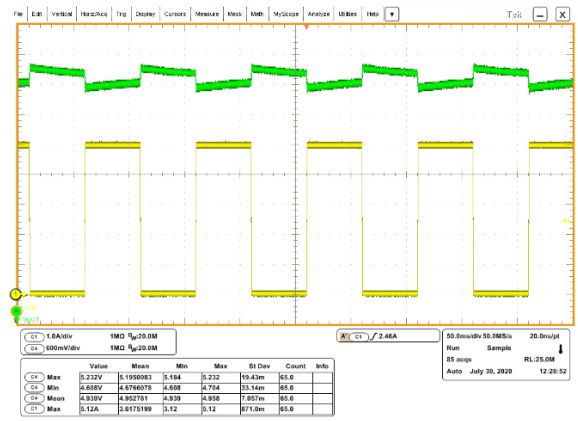


In figures Figure 11 and Figure 12:

- green = V_{OUT} 600 mV/div
- yellow = I_{OUT} 1 A/div

Figure 11. Dynamic load at 5 V/5 A, V_{IN} = 115 V_{AC}

Figure 12. Dynamic load at 5 V/5 A, V_{IN} = 230 V_{AC}



In figures Figure 13 and Figure 14:

- green = V_{OUT} 1 V/div
- yellow = I_{OUT} 1 A/div

Figure 13. Dynamic load at 9 V/3 A, V_{IN} = 115 V_{AC}

Figure 14. Dynamic load at 9 V/3 A, V_{IN} = 230 V_{AC}

In figures Figure 15 and Figure 16:

- green = V_{OUT} 1.2 V/div
- yellow = I_{OUT} 1 A/div

Figure 15. Dynamic load at 11 V/2.45 A, V_{IN} = 115 V_{AC}

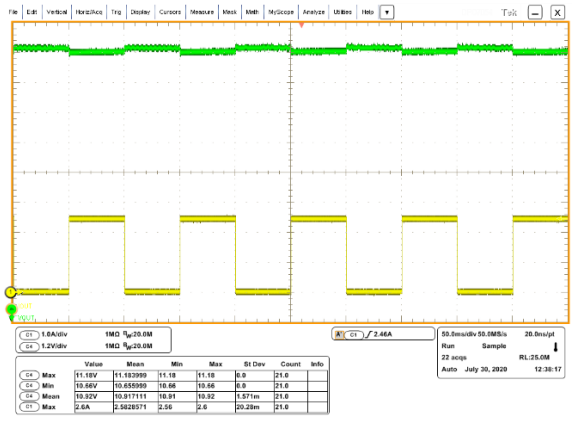


Figure 16. Dynamic load at 11 V/2.45 A, V_{IN} = 230 V_{AC}

1.3 Output voltage ripple

The output voltage ripple has been measured through an oscilloscope at four different output voltages (3.3, 5, 9 and 11 V) with two different load currents (0 A and maximum available current).

Tests have been performed with two different AC voltage inputs (115 and 230 V_{AC}) and using a commercial tool working as a sink.

The latter has been driven to request APDO3 profile, with 5 A maximum current, for 3.3 and 5 V, whereas the APDO4 has been requested for the 9 and 11 V, with 3 and 2.4 A maximum current respectively.

Table 1. Output voltage ripple test results

V_{AC} [V]	V_{OUT} [V]	Load [A]	Ripple [mV]	Max. ripple [mV] allowed by USB-PD specification
115 @ 60 Hz	3.3	0	±46.5	±165
	3.3	5	±39.25	±165
	5	0	±43.5	±250
	5	5	±43	±250
	9	0	±43.5	±450
	9	3	±45.5	±450
	11	0	±46.5	±550
	11	2.4	±45.75	±550
230 @ 50Hz	3.3	0	±32.25	±165
	3.3	5	±31.25	±165
	5	0	±29.5	±250
	5	5	±29.75	±250
	9	0	±31.75	±450
	9	3	±31.75	±450
	11	0	±44.5	±550
	11	2.4	±45.75	±550

Figure 17. Ripple at 115 V_{AC}, out 3.3 V, no load

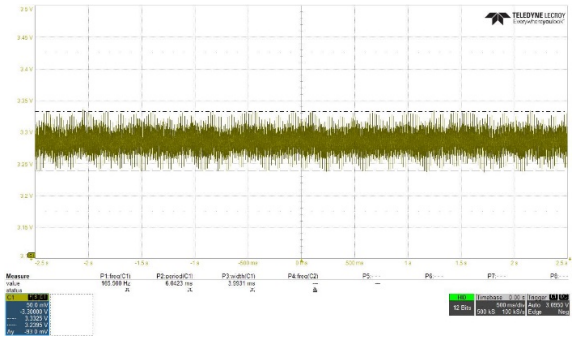


Figure 18. Ripple at 115 V_{AC}, out 3.3 V, 5 A

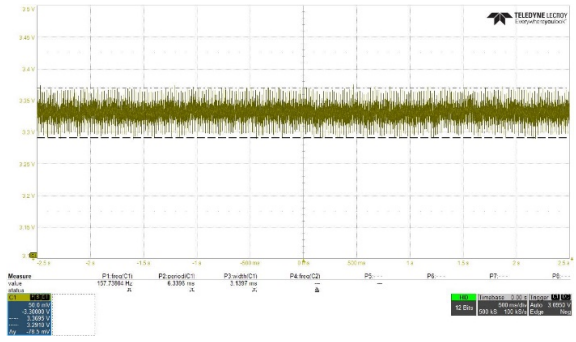


Figure 19. Ripple at 115 V_{AC}, out 5 V, no load

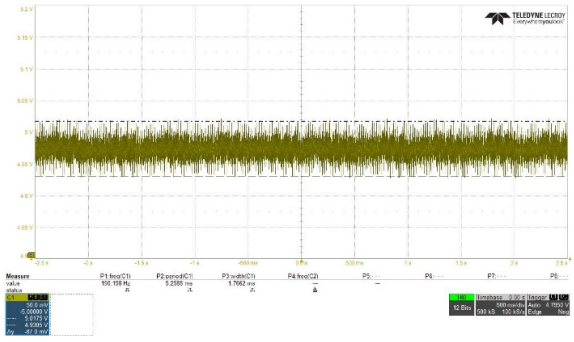


Figure 20. Ripple at 115 V_{AC}, out 5 V, 5 A

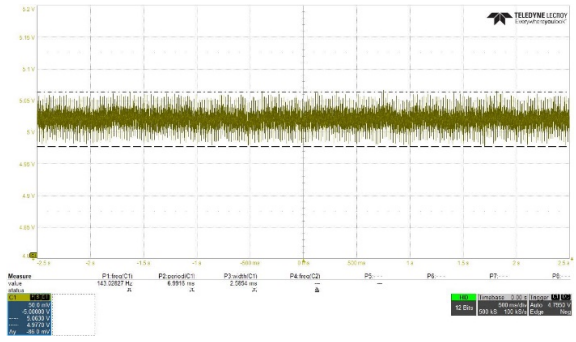


Figure 21. Ripple at 115 V_{AC}, out 9 V, no load

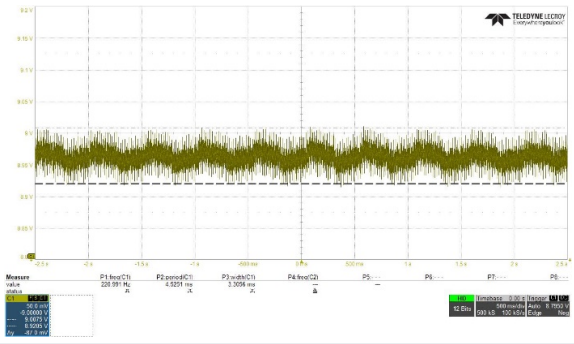


Figure 22. Ripple at 115 V_{AC}, out 9 V, 3 A

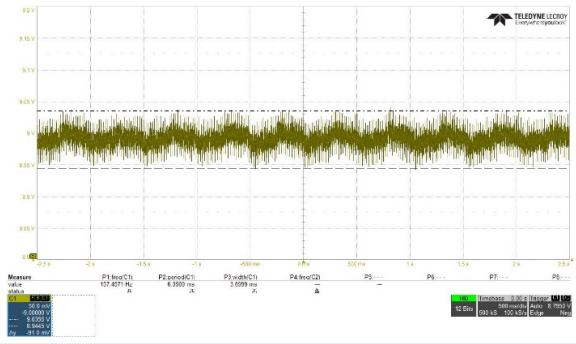


Figure 23. Ripple at 115 V_{AC}, out 11 V, no load

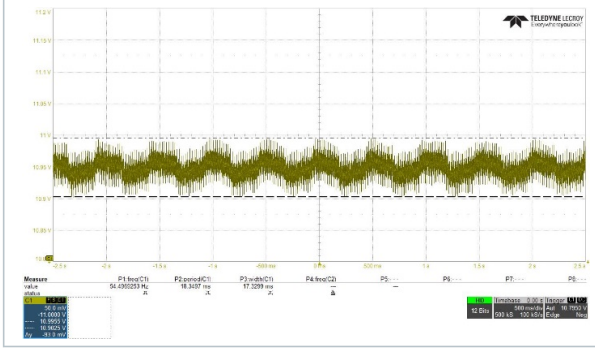


Figure 24. Ripple at 115 V_{AC}, out 11 V, 2.4 A

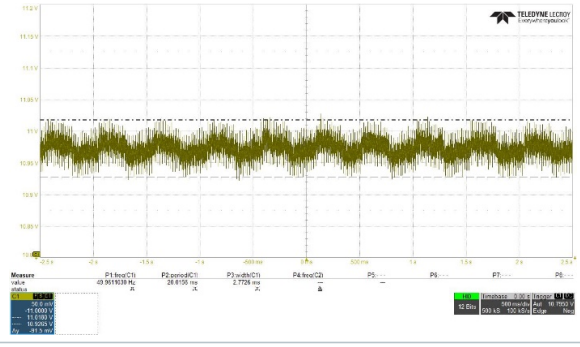


Figure 25. Ripple at 230 V_{AC}, out 3.3 V, no load

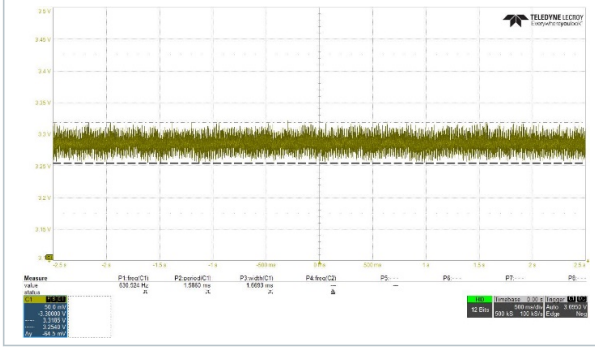


Figure 26. Ripple at 230 V_{AC}, out 3.3 V, 5 A

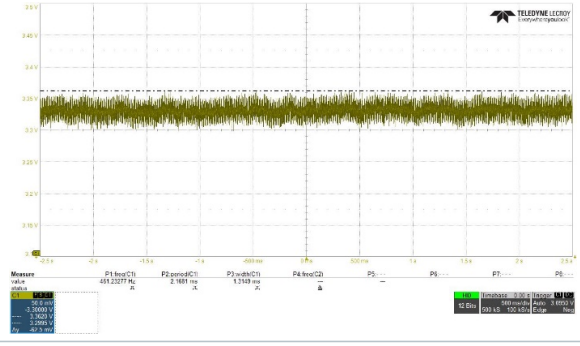


Figure 27. Ripple at 230 V_{AC}, out 5 V, no load

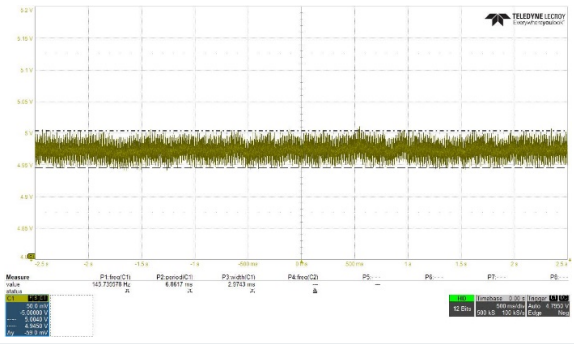


Figure 28. Ripple at 230 V_{AC}, out 5 V, 5 A

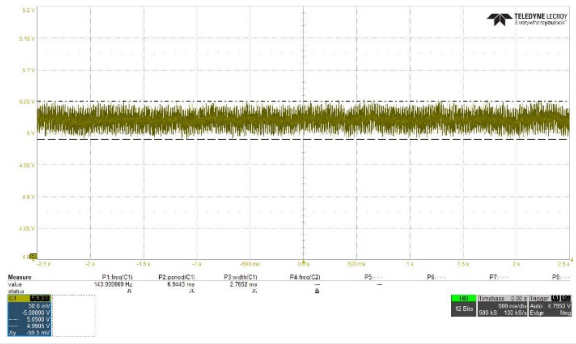


Figure 29. Ripple at 230 V_{AC}, out 9 V, no load

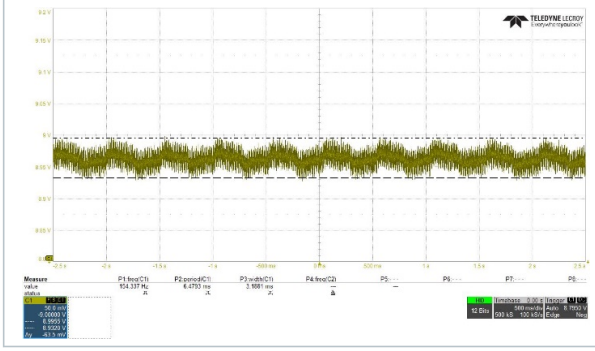


Figure 30. Ripple at 230 V_{AC}, out 9 V, 3 A

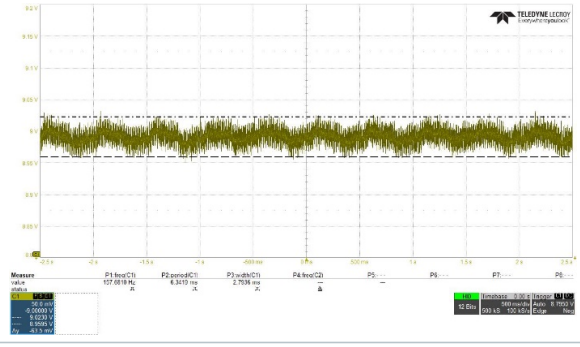


Figure 31. Ripple at 230 V_{AC}, out 11 V, no load

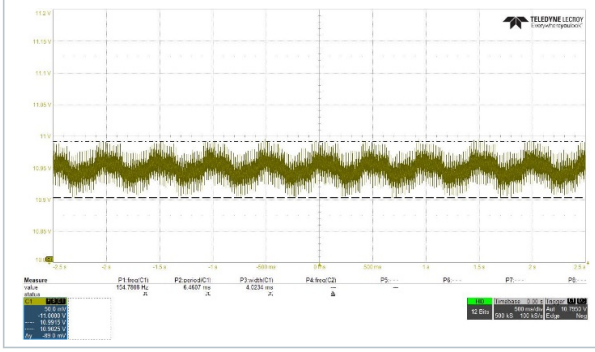
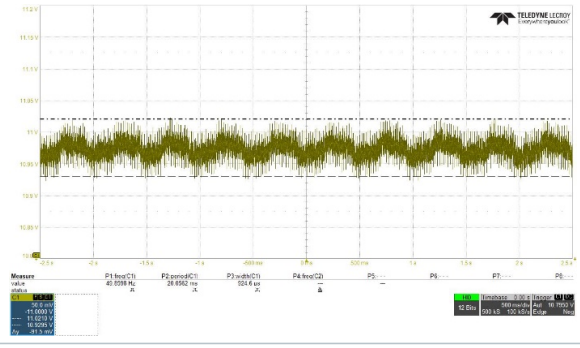


Figure 32. Ripple at 230 V_{AC}, out 11 V, 2.4 A



1.4 Voltage stress on the main power MOSFET

The following figures show the flyback converter primary MOSFET drain voltage and the current sense pin voltage waveforms at 90 and 265 V_{AC} under full load condition.

Figure 33. Primary side waveform at 3.3 V/5 A, V_{IN} = 90 V_{AC}

- Blue = V_{CS} 400 mV/div
- Green = V_{DS} 60 V/div
- V_{DSMAX} = 362.4 V

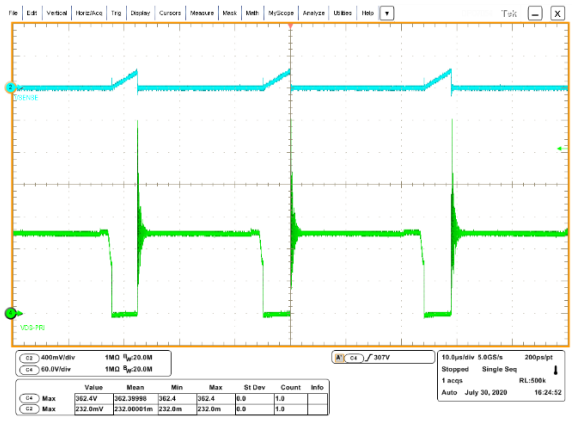


Figure 34. Primary side waveform at 3.3 V/5 A, V_{IN} = 265 V_{AC}

- Blue = V_{CS} 400 mV/div
- Green = V_{DS} 100 V/div
- V_{DSMAX} = 612 V

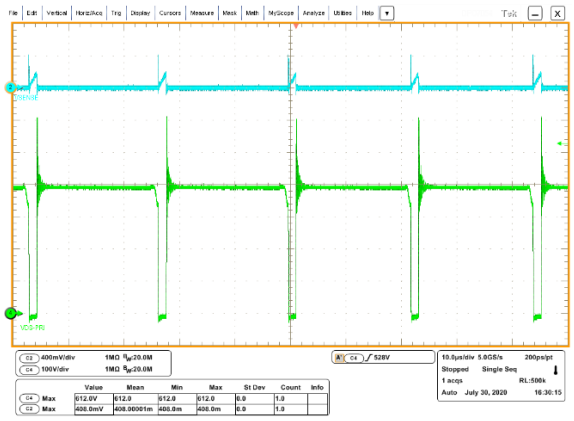


Figure 35. Primary side waveform at 5 V/5 A, V_{IN} = 90 V_{AC}

- Blue = V_{CS} 400 mV/div
- Green = V_{DS} 60 V/div
- V_{DSMAX} = 364.8 V

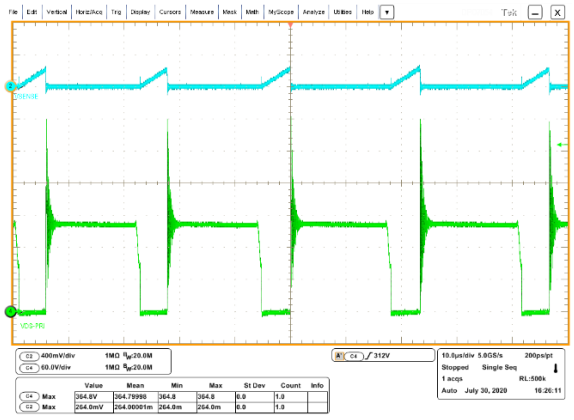


Figure 36. Primary side waveform at 5 V/5 A, V_{IN} = 265 V_{AC}

- Blue = V_{CS} 400 mV/div
- Green = V_{DS} 100 V/div
- V_{DSMAX} = 624 V

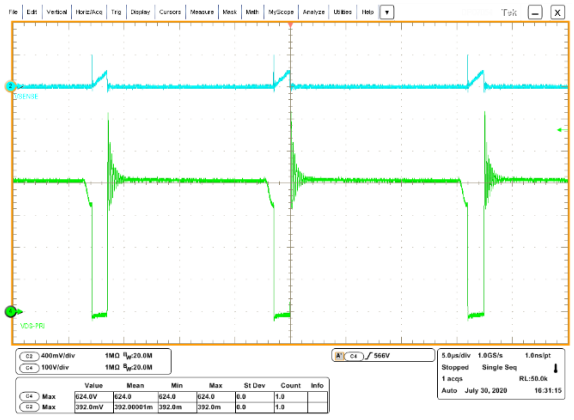


Figure 37. Primary side waveform at 9 V/3 A, V_{IN} = 90 V_{AC}

- Blue = V_{CS} 400 mV/div
- Green = V_{DS} 60 V/div
- V_{DSMAX} = 328.8 V

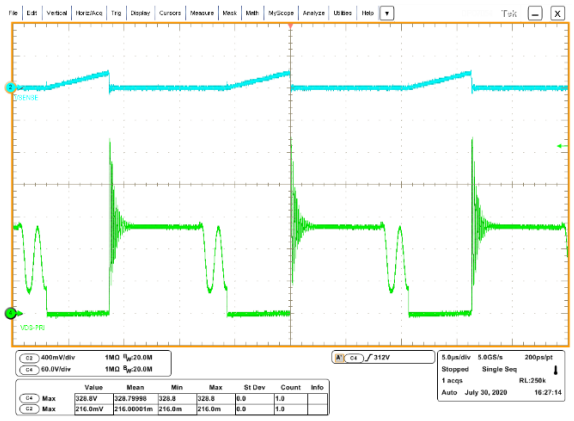


Figure 38. Primary side waveform at 9 V/3 A, V_{IN} = 265 V_{AC}

- Blue = V_{CS} 400 mV/div
- Green = V_{DS} 100 V/div
- V_{DSMAX} = 616 V

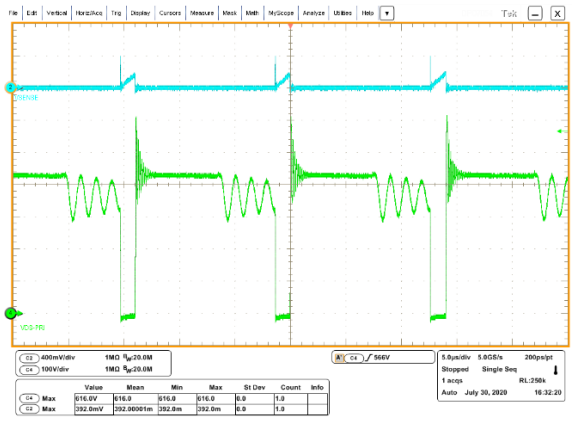


Figure 39. Primary side waveform at 11 V/2.45 A, V_{IN} = 90 V_{AC}

- Blue = V_{CS} 400 mV/div
- Green = V_{DS} 60 V/div
- V_{DSMAX} = 345.6 V

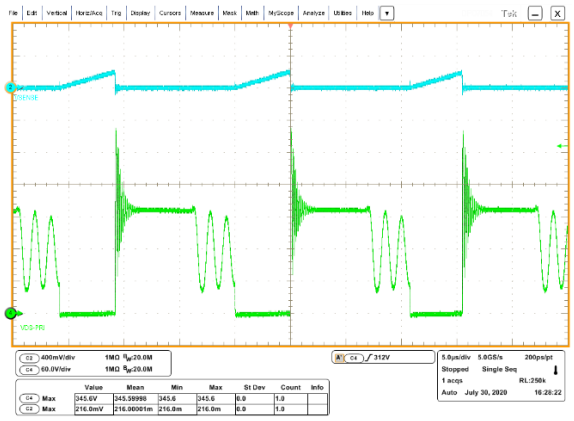
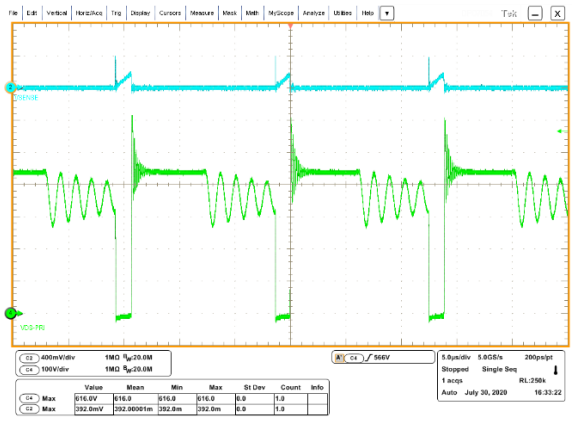


Figure 40. Primary side waveform at 11 V/2.45 A, V_{IN} = 265 V_{AC}

- Blue = V_{CS} 400 mV/div
- Green = V_{DS} 100 V/div
- V_{DSMAX} = 616 V



The following figures show the flyback converter secondary MOSFET drain voltage and the current sense pin voltage waveforms at 90 and 265 V_{AC} under full load condition.

Figure 41. Secondary side waveform at 3.3 V/5 A, V_{IN} = 90 V_{AC}

- Green = V_{DS} 9 V/div
- V_{DSMAX} = 27 V

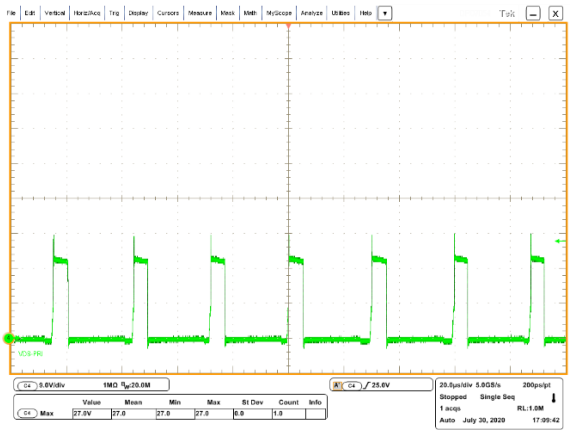


Figure 42. Secondary side waveform at 3.3 V/5 A, V_{IN} = 265 V_{AC}

- Green = V_{DS} 20 V/div
- V_{DSMAX} = 76.8 V

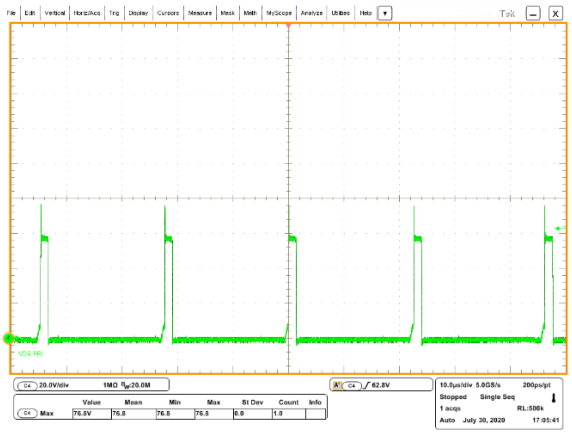


Figure 43. Secondary side waveform at 5 V/5 A, V_{IN} = 90 V_{AC}

- Green = V_{DS} 9 V/div
- V_{DSMAX} = 29.5 V

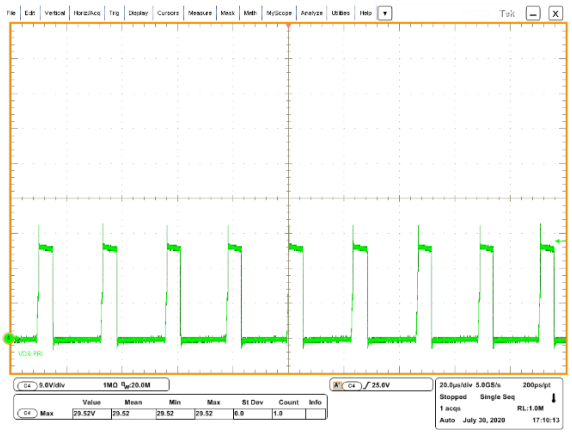


Figure 44. Secondary side waveform at 5 V/5 A, V_{IN} = 265 V_{AC}

- Green = V_{DS} 20 V/div
- V_{DSMAX} = 74.4 V

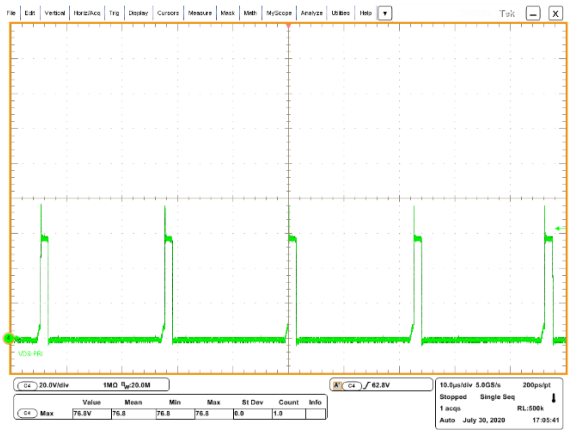


Figure 45. Secondary side waveform at 9 V/3 A, V_{IN} = 90 V_{AC}

- Green = V_{DS} 9 V/div
- V_{DSMAX} = 28.4 V

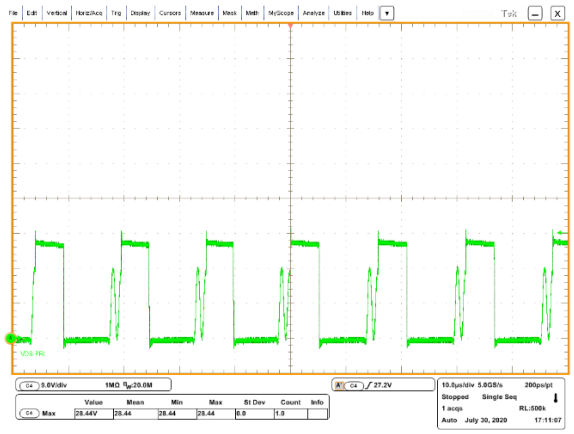


Figure 46. Secondary side waveform at 9 V/3 A, V_{IN} = 265 V_{AC}

- Green = V_{DS} 20 V/div
- V_{DSMAX} = 78.4 V

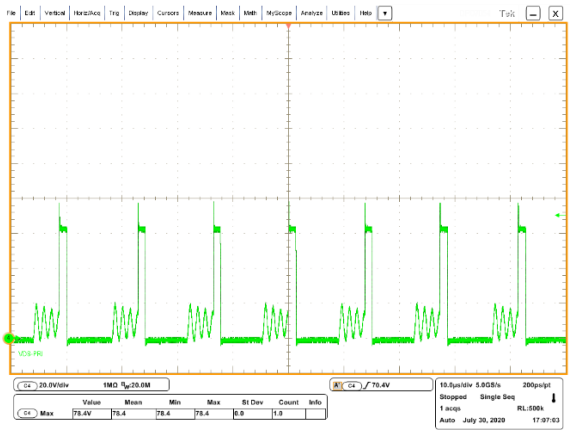


Figure 47. Secondary side waveform at 11 V/2.45 A, V_{IN} = 90 V_{AC}

- Green = V_{DS} 9 V/div
- V_{DSMAX} = 33.8 V

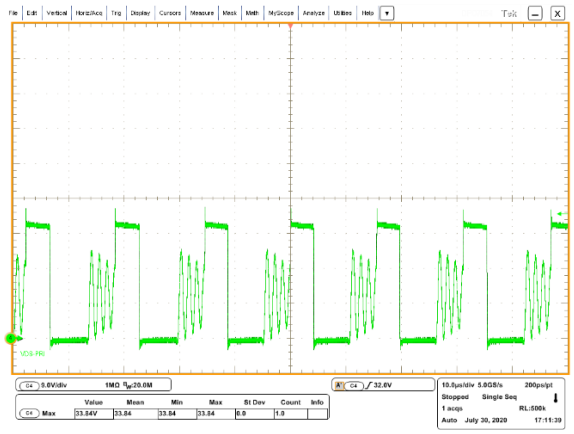
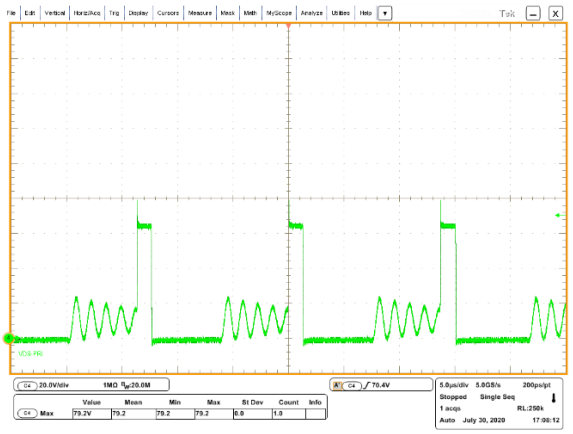


Figure 48. Secondary side waveform at 11 V/2.45 A, V_{IN} = 265 V_{AC}

- Green = V_{DS} 20 V/div
- V_{DSMAX} = 79.2 V



1.5 Synchronous rectification

Synchronous rectification (SR) uses low R_{DS_ON} MOSFET in place of a diode rectifier on the output stage to reduce losses and increase efficiency. The MOSFET is directly driven by the MCU running an SR algorithm.

When the MOSFET body diode starts to conduct, the synchronous rectification control logic generates a PWM signal to turn the MOSFET on. A sensing circuit for the V_{DS} voltage (that is, a diode and an RC network) is required to properly drive the MOSFET.

The following figures show waveforms acquired supplying the board at 264 V_{AC}, 50 Hz, reaching 11 V and sinking the maximum available power of 27 W.

Figure 49 and Figure 50 show a single period on the secondary side. The PWM is turned on when the V_{DS_SENSE} signal presents a falling edge, that is Q1 body diode is conducting. Once the PWM is turned on, the Q1 channel is conducting with its low R_{DS_on}, thus lowering the voltage drop on the device.

Q1 is turned off when V_{DS_SENSE} reaches a predefined threshold. The adaptive synchronous rectification algorithm sets the appropriate turn-off events for the given load conditions.

Figure 49. V_{DS} AND PWM_{SR} typical waveform

Yellow: V_{DS_SENSE}

Pink: V_{DS} Q1

Blue: PWM_{SR}

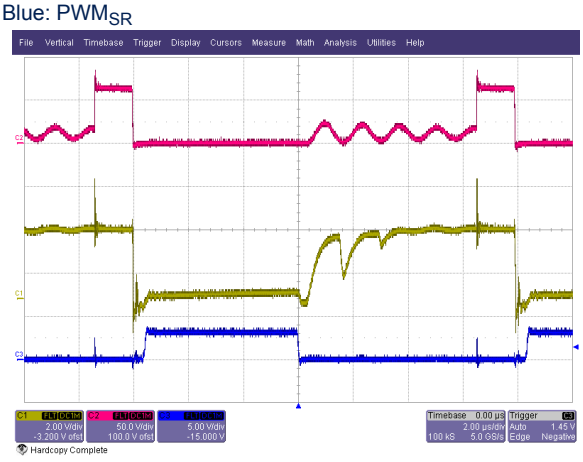
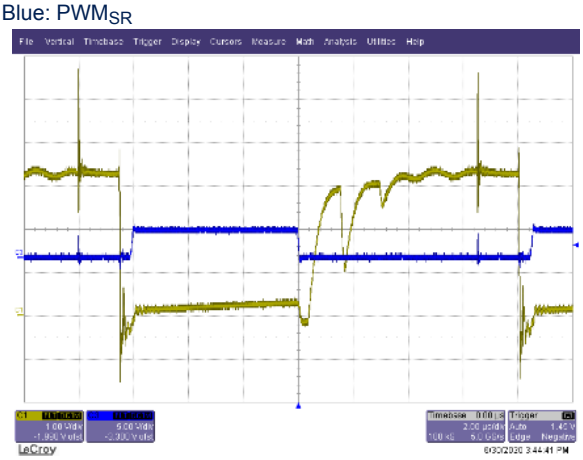


Figure 50. V_{DS} AND PWM_{SR} typical waveform

Yellow: V_{DS_SENSE}

Blue: PWM_{SR}

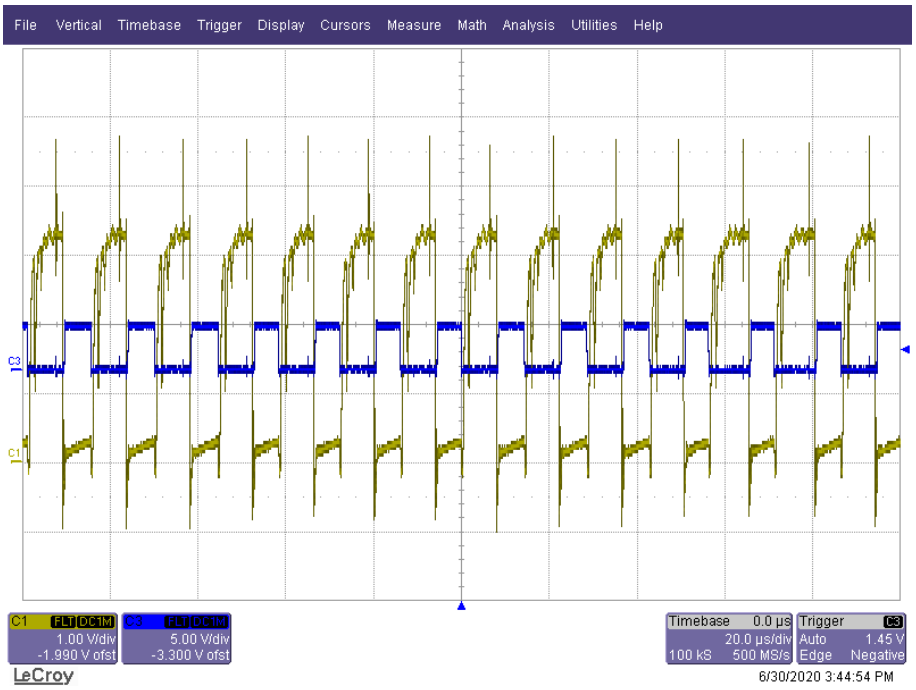


The following figure shows the behavior of the synchronous rectification under the same conditions but on a largest time frame.

Figure 51. Synchronous rectification - 11 V output, full load

Yellow: V_{DS_SENSE}

Blue: PWM_{SR}



RELATED LINKS

AN5499:How to implement adaptive synchronous rectification in flyback converters using STM32 MCUs

2 Overcurrent protection

For overcurrent protection tests, a commercial tool has been used to request the power profiles implemented by the STEVAL-USBPD27S and to sink the desired nominal current.

An electronic load requests extra current to reach 130% of the maximum load starting from 0% and 100% of nominal current.

The commercial tool to select the PDO has been connected in parallel to the electronic load.

The two nominal currents are set to 0% and 100% of the maximum currents offered by each profile. The current sunk from the STEVAL-USBPD27S and the output voltages at the Type C connector are shown in the following pictures.

Figure 52. PDO1 (5 V at 5 A) V_{AC} = 115 V, 0%, test current = 6.5 A

Yellow: output current

Pink: V_{BUS}

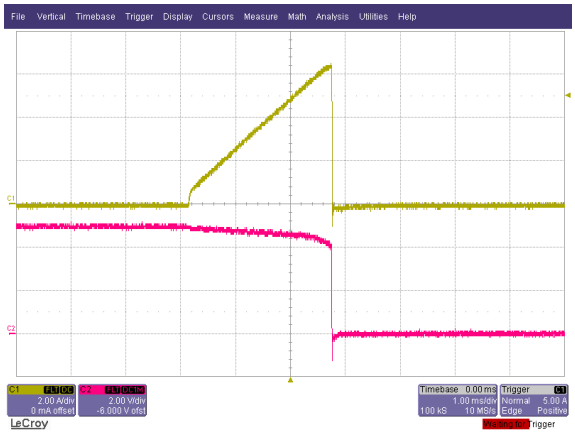


Figure 53. PDO1 (5 V at 5 A) V_{AC} = 115 V, 100%, test current = 6.5 A

Yellow: output current

Pink: V_{BUS}

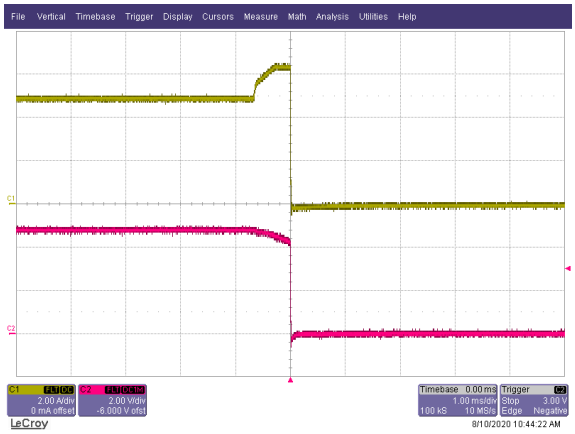


Figure 54. PDO1 (5 V at 5 A) V_{AC} = 230 V, 0%, test current = 6.5 A

Yellow: output current

Pink: V_{BUS}

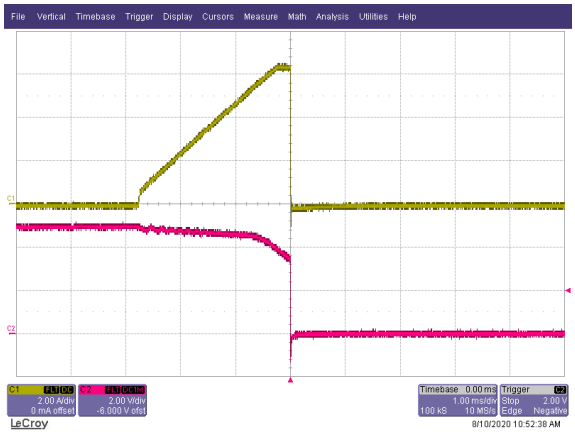


Figure 55. PDO1 (5 V at 5 A) V_{AC} = 230 V, 100%, test current = 6.5 A

Yellow: output current

Pink: V_{BUS}

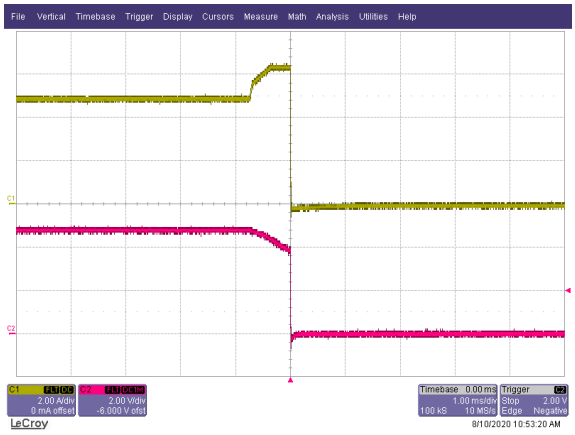


Figure 56. PDO2 (9 V at 3 A) V_{AC} = 115 V, 0%, test current = 3.9 A

Yellow: output current

Pink: V_{BUS}

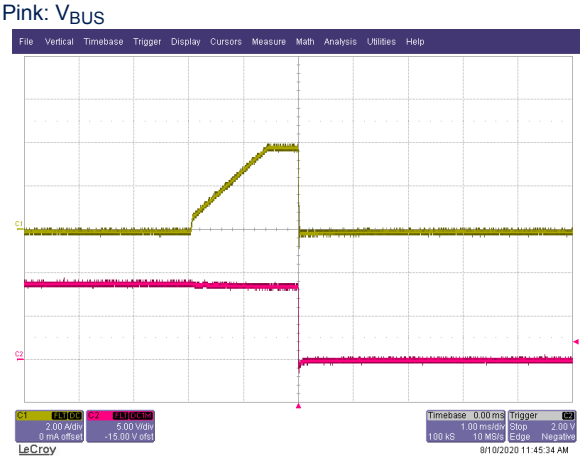


Figure 57. PDO1 (9 V at 3 A) V_{AC} = 115 V, 100%, test current = 3.9 A

Yellow: output current

Pink: V_{BUS}

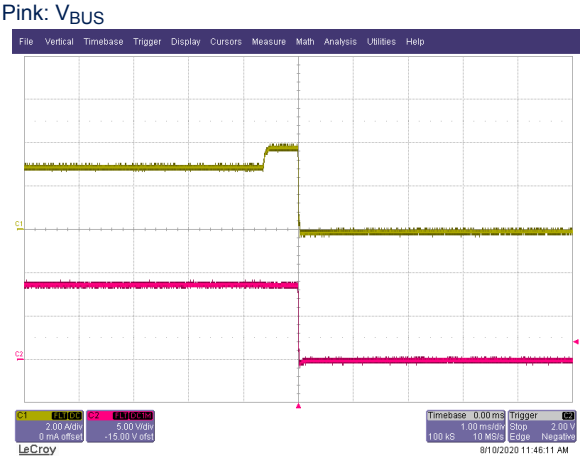


Figure 58. PDO2 (9 V at 3 A) V_{AC} = 230 V, 0%, test current = 3.9 A

Yellow: output current

Pink: V_{BUS}

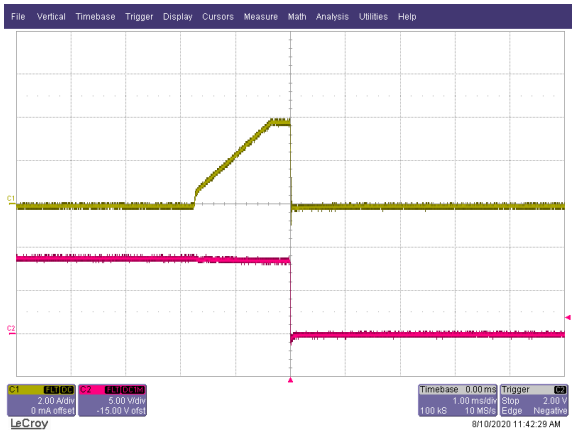
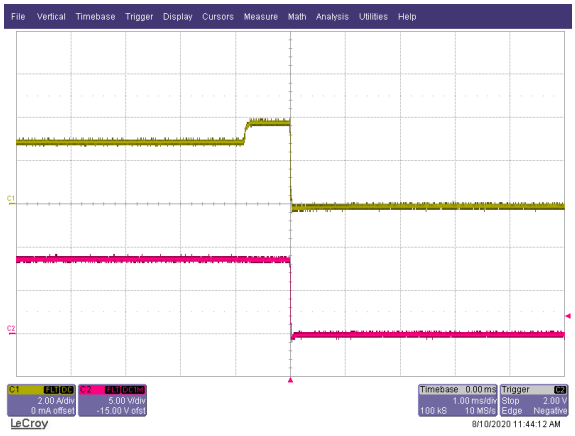


Figure 59. PDO1 (9 V at 3 A) V_{AC} = 230 V, 100%, test current = 3.9 A

Yellow: output current

Pink: V_{BUS}



Once the current reaches the faulty value, the STEVAL-USBPD27S shuts down all the ports within the time specified by specification (`tSafe0V`) that has to be less than 650 ms.

As shown, the STEVAL-USBPD27S shuts down the port in less than 1 ms and the system restarts after 8 seconds.

3 PD power adapter behavior

3.1 PD Eye diagram

One of the requirements defined in the PD specification is that the transmitted data waveform has to fulfill the eye diagram mask. Thus, a specified BIST Eye Pattern test mode has been applied to output a continuous pseudo-random bit sequence suitable to demonstrate the eye diagram.

The following figures show two eye diagrams obtained through the MQP PDT-BT2-CON1 tool and the related GraphicsUSB V6.10.02 software.

Figure 60. USBPD transceiver eye diagram - 115 V at 60 Hz

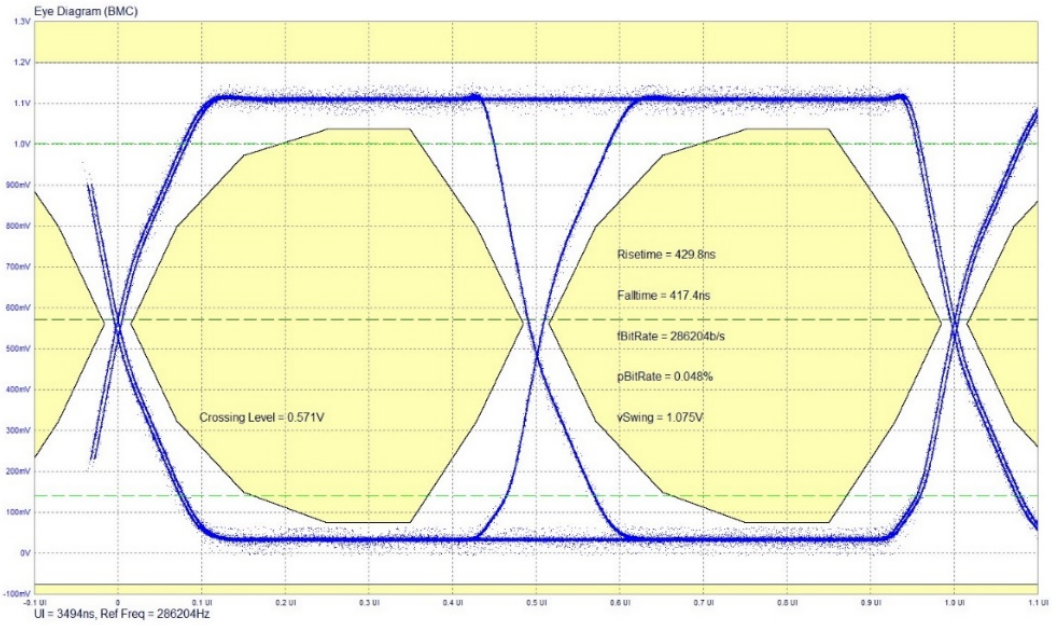
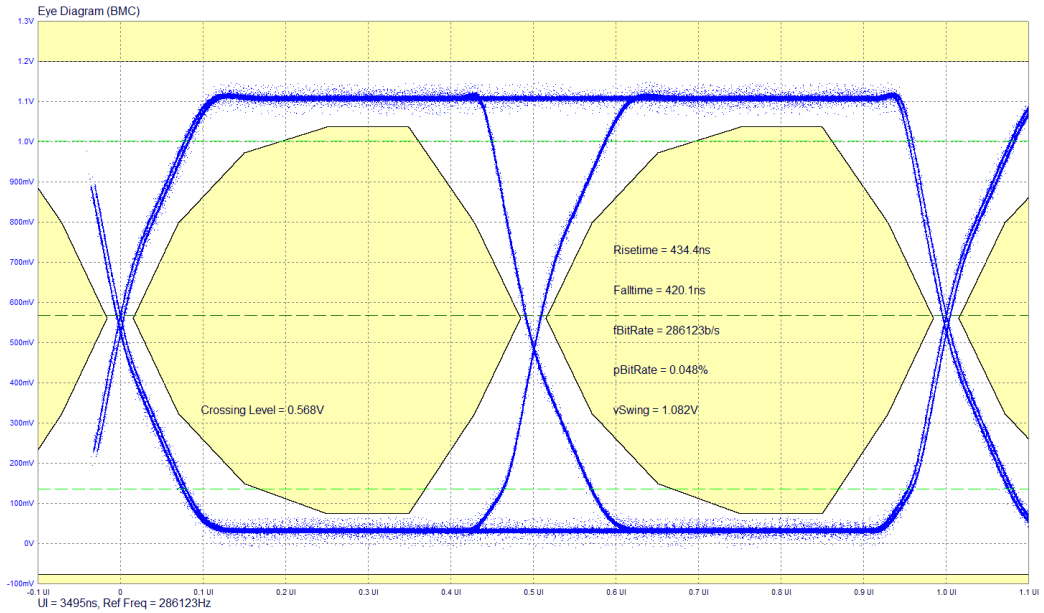


Figure 61. **USBPD transceiver eye diagram - 230 V at 50 Hz**



3.2 Voltage transitions across all profiles

The following pictures show all the voltage transitions acquired through an oscilloscope and using APDO profiles: APDO 3 for transitions from 3.3 to 5 V and APDO 4 for the other transitions.

All transitions respect USB-PD requirements (transitions time < 275 ms, maximum voltage in addition to the new voltage value during the transition = ±500 mV). For further details, refer to AN5562, freely available on www.st.com.

Figure 62. **Voltage transition from 3.3 to 5 V at 115 V_{AC}- no load**

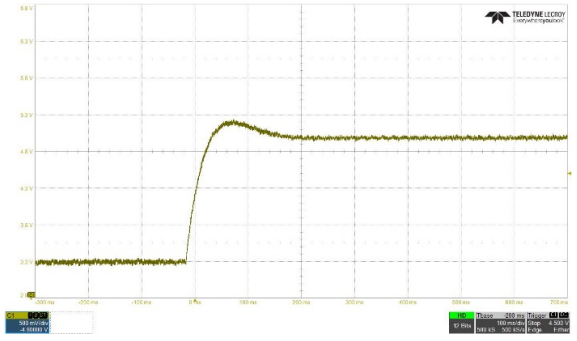


Figure 63. **Voltage transition from 3.3 to 5 V at 115 V_{AC} - 5 A**

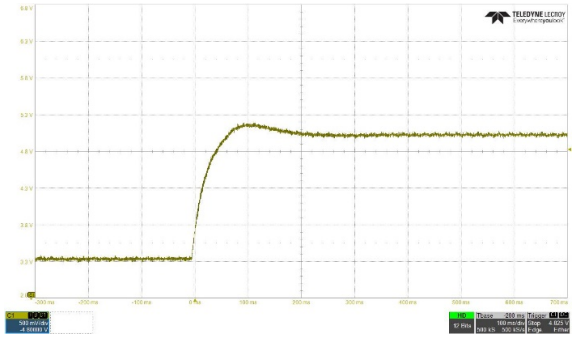


Figure 64. Voltage transition from 5 to 3.3 V at 115 V_{AC}- no load

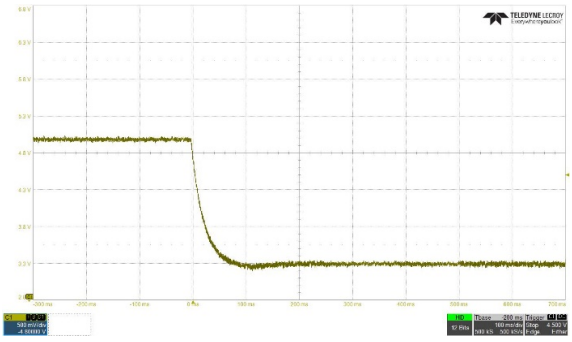


Figure 65. Voltage transition from 5 to 3.3 V at 115 V_{AC} - 5 A

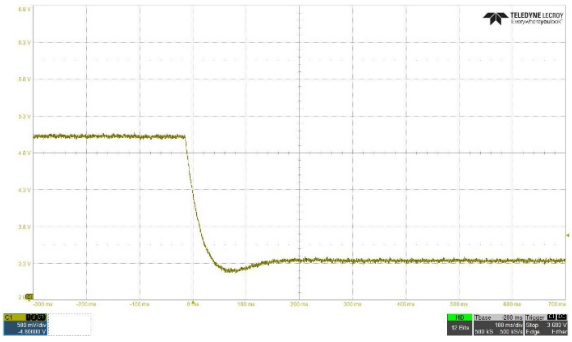


Figure 66. Voltage transition from 3.3 to 9 V at 115 V_{AC}- no load

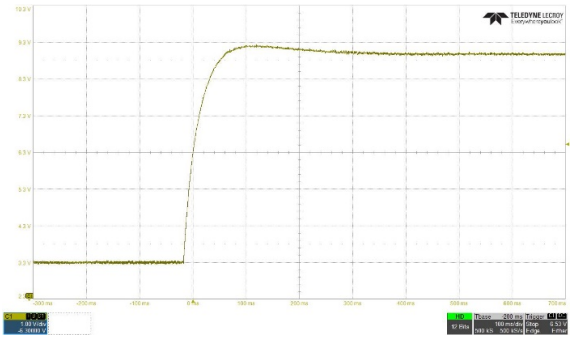


Figure 67. Voltage transition from 3.3 to 9 V at 115 V_{AC} - 3 A

Figure 68. Voltage transition from 9 to 3.3 V at 115 V_{AC}- no load

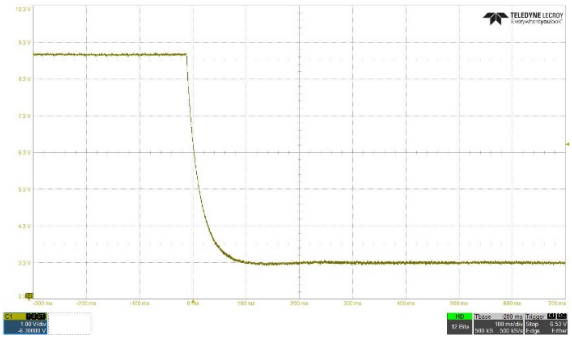


Figure 69. Voltage transition from 9 to 3.3 V at 115 V_{AC} - 3 A

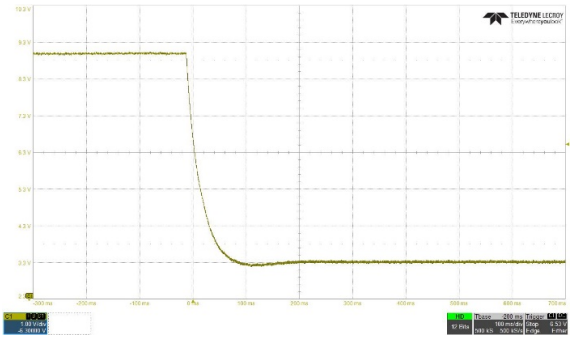


Figure 70. Voltage transition from 3.3 to 11 V at 115 V_{AC}- no load

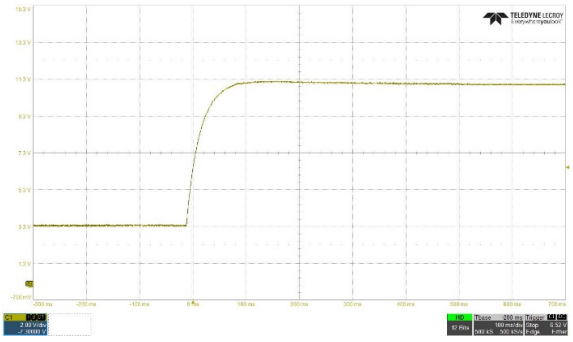


Figure 71. Voltage transition from 3.3 to 11 V at 115 V_{AC} - 2.4 A

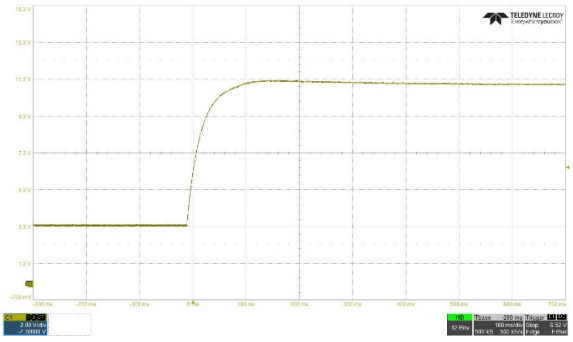


Figure 72. Voltage transition from 11 to 3.3 V at 115 V_{AC}- no load

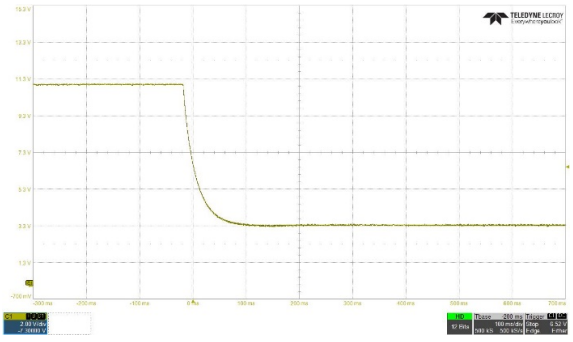


Figure 73. Voltage transition from 11 to 3.3 V at 115 V_{AC} - 2.4 A

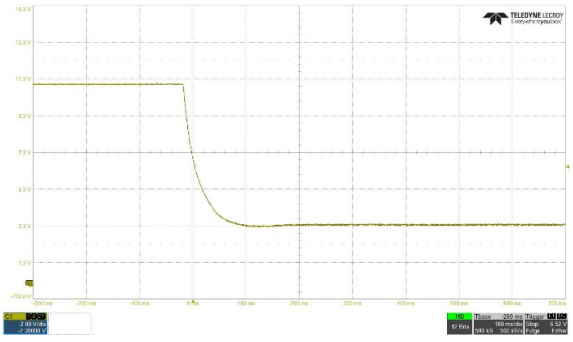


Figure 74. Voltage transition from 5 to 9 V at 115 V_{AC}- no load

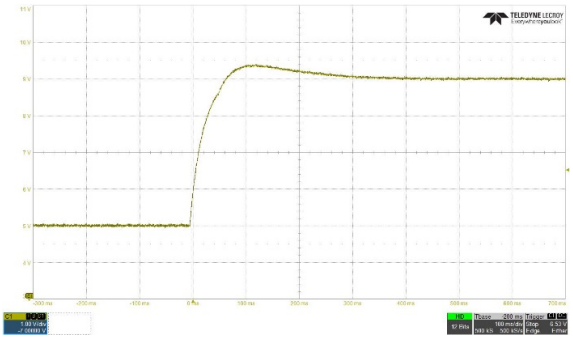


Figure 75. Voltage transition from 5 to 9 V at 115 V_{AC} - 3 A

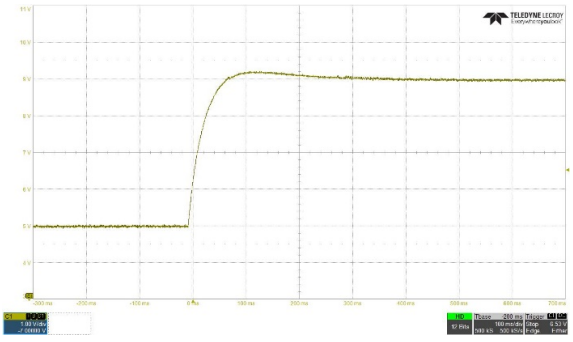


Figure 76. Voltage transition from 9 to 5 V at 115 V_{AC}- no load

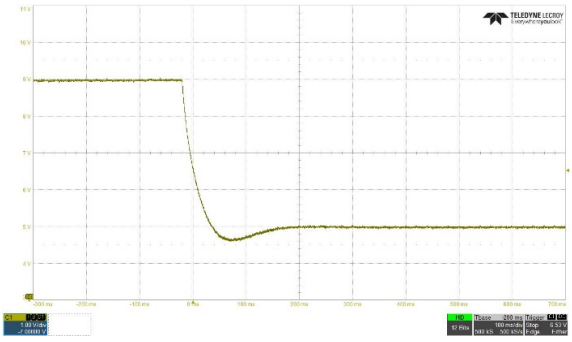


Figure 77. Voltage transition from 9 to 5 V at 115 V_{AC} - 3 A

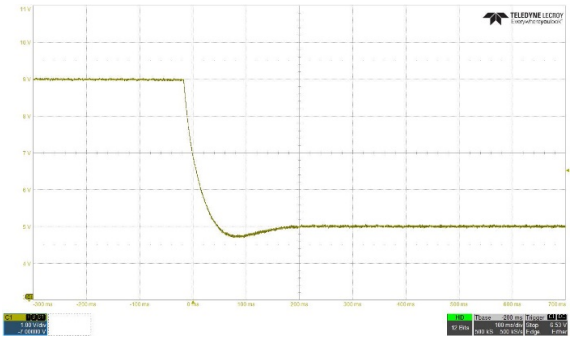


Figure 78. Voltage transition from 5 to 11 V at 115 V_{AC}- no load

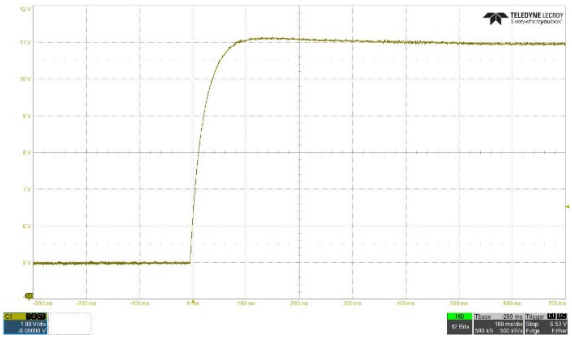


Figure 79. Voltage transition from 5 to 11 V at 115 V_{AC} - 2.4 A

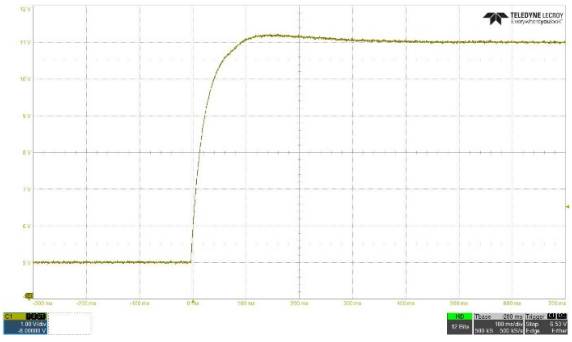


Figure 80. Voltage transition from 11 to 5 V at 115 V_{AC}- no load

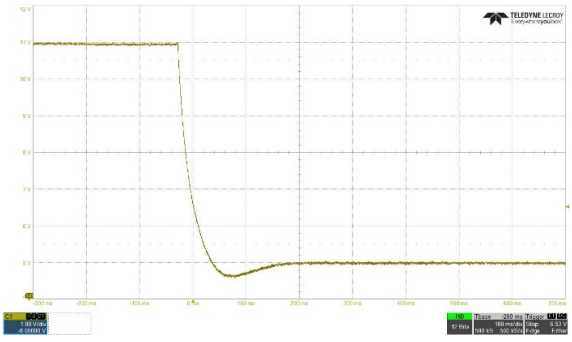


Figure 81. Voltage transition from 11 to 5 V at 115 V_{AC} - 2.4 A

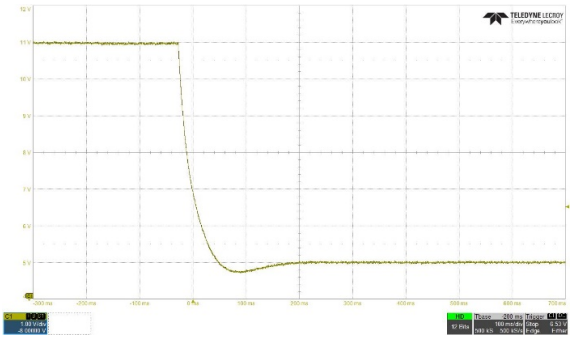


Figure 82. Voltage transition from 9 to 11 V at 115 V_{AC}- no load

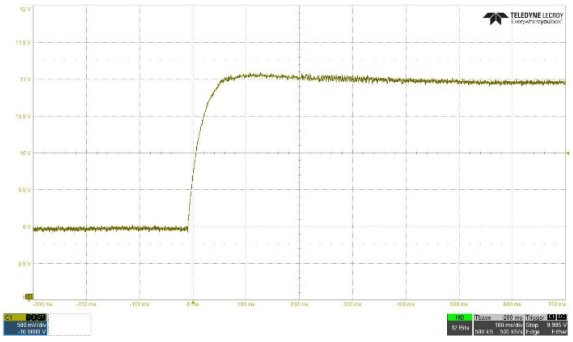


Figure 83. Voltage transition from 9 to 11 V at 115 V_{AC} - 2.4 A

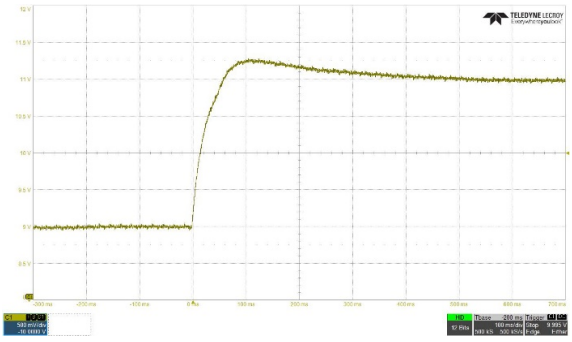


Figure 84. Voltage transition from 11 to 9 V at 115 V_{AC}- no load

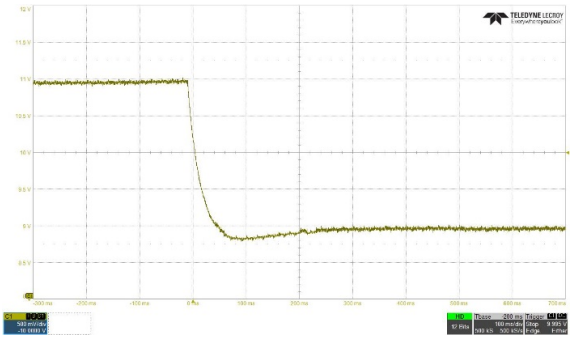


Figure 85. Voltage transition from 11 to 9 V at 115 V_{AC} - 2.4 A

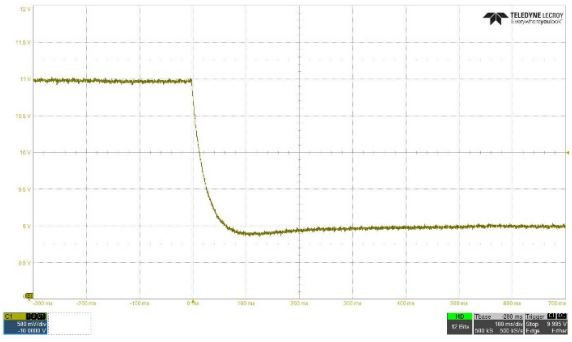


Figure 86. Voltage transition from 3.3 to 5 V at 230 V_{AC}- no load

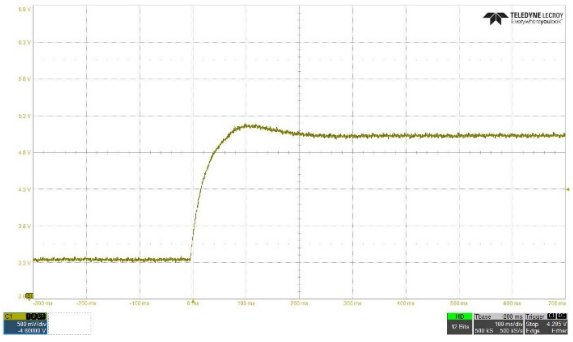


Figure 87. Voltage transition from 3.3 to 5 V at 230 V_{AC} - 5 A

Figure 88. Voltage transition from 5 to 3.3 V at 230 V_{AC}- no load

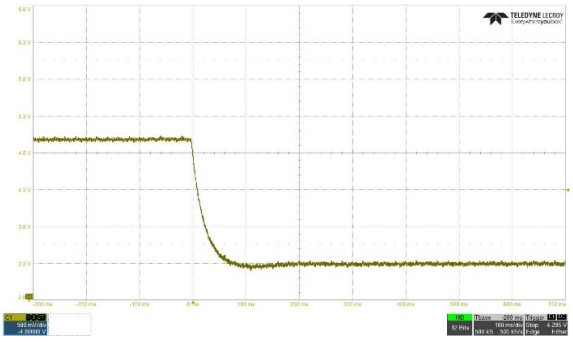


Figure 89. Voltage transition from 5 to 3.3 V at 230 V_{AC} - 5 A

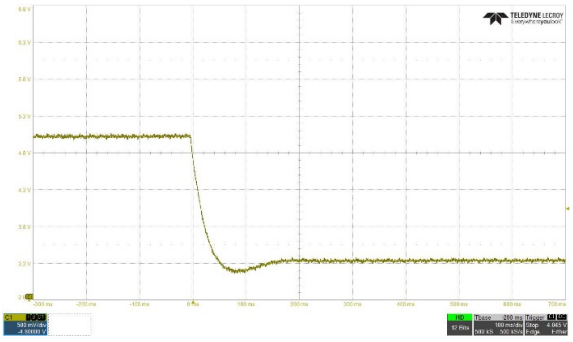


Figure 90. Voltage transition from 3.3 to 9 V at 230 V_{AC}- no load

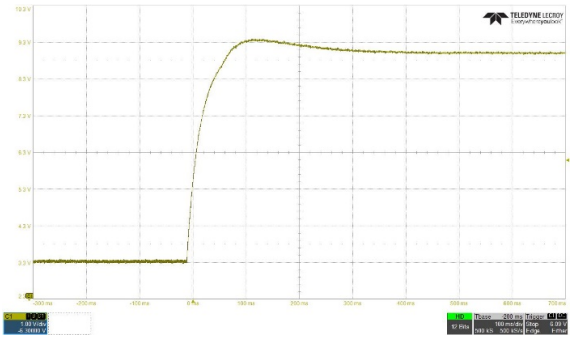


Figure 91. Voltage transition from 3.3 to 9 V at 230 V_{AC} - 3 A

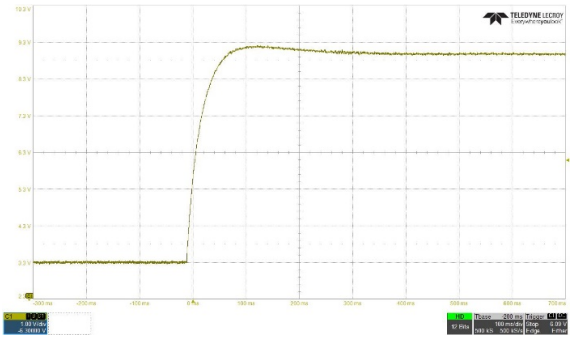


Figure 92. Voltage transition from 9 to 3.3 V at 230 V_{AC}- no load

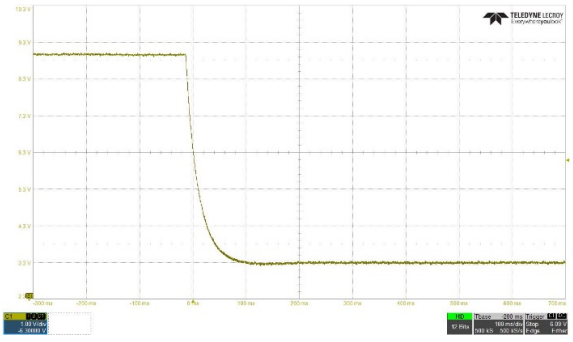


Figure 93. Voltage transition from 9 to 3.3 V at 230 V_{AC} - 3 A

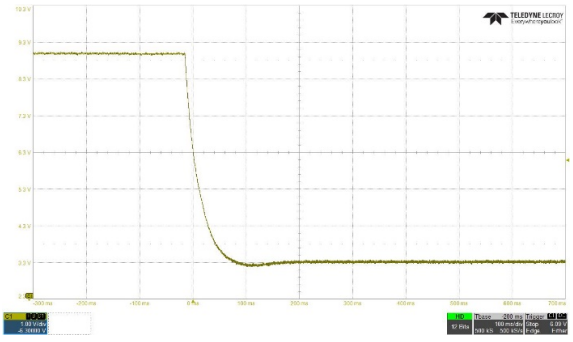


Figure 94. Voltage transition from 3.3 to 11 V at 230 V_{AC}- no load

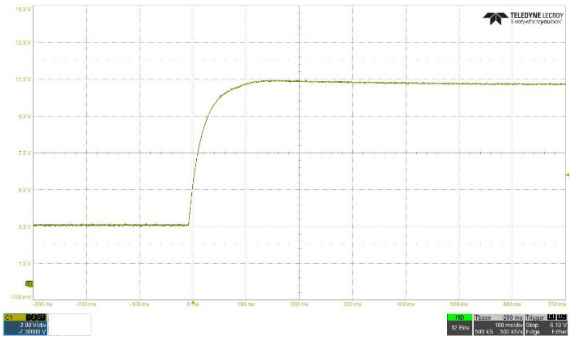


Figure 95. Voltage transition from 3.3 to 11 V at 230 V_{AC} - 2.2 A

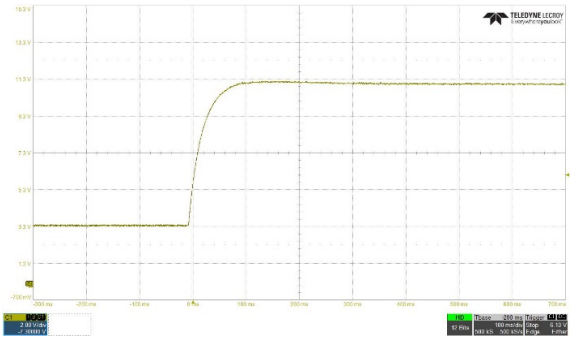


Figure 96. Voltage transition from 11 to 3.3 V at 230 V_{AC}- no load

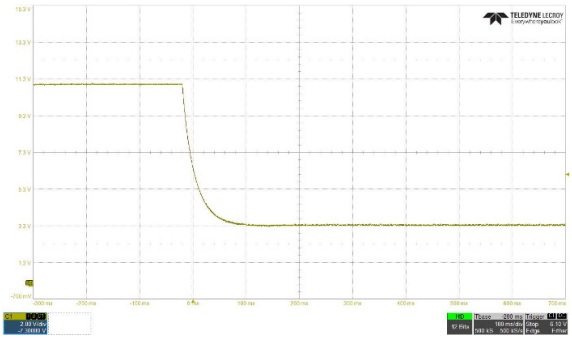


Figure 97. Voltage transition from 11 to 3.3 V at 230 V_{AC} - 2.4 A

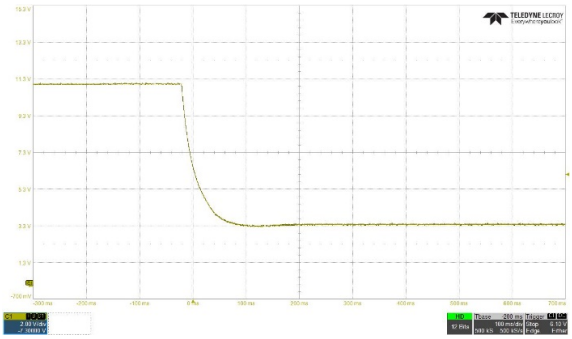


Figure 98. Voltage transition from 5 to 9 V at 230 V_{AC}- no load

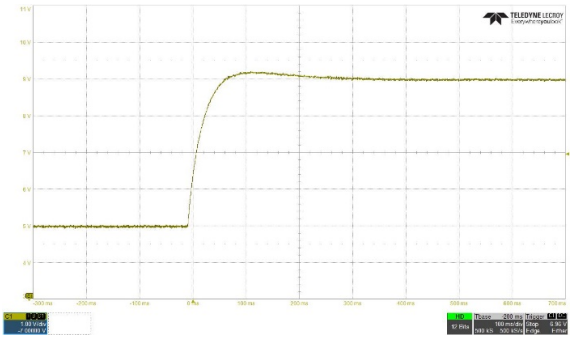


Figure 99. Voltage transition from 5 to 9 V at 230 V_{AC} - 3 A

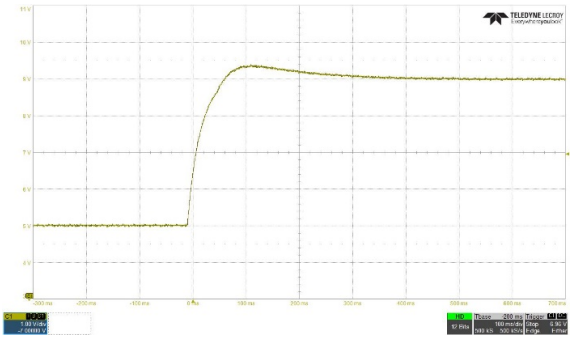


Figure 100. Voltage transition from 9 to 5 V at 230 V_{AC}- no load

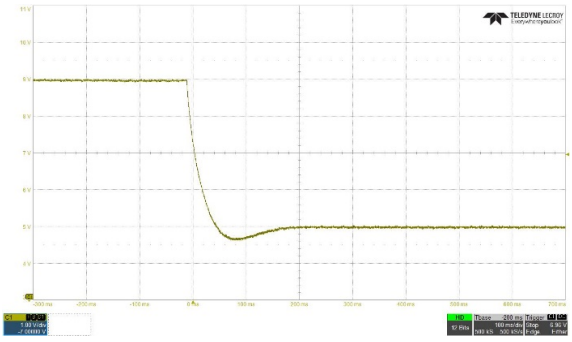


Figure 101. Voltage transition from 9 to 5 V at 230 V_{AC} - 3 A

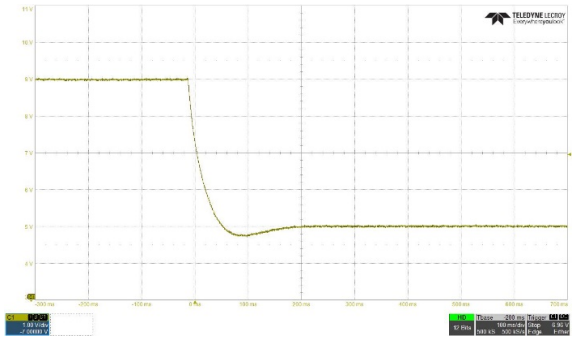


Figure 102. Voltage transition from 5 to 11 V at 230 V_{AC}- no load

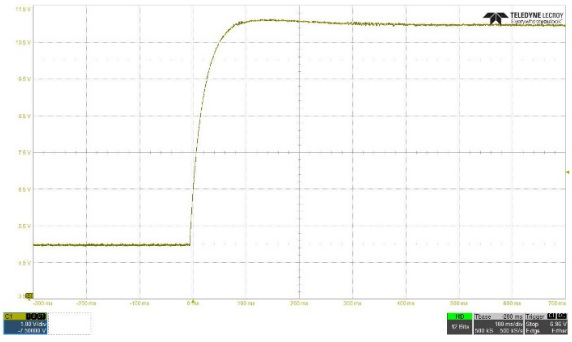


Figure 103. Voltage transition from 5 to 11 V at 230 V_{AC} - 2.4 A

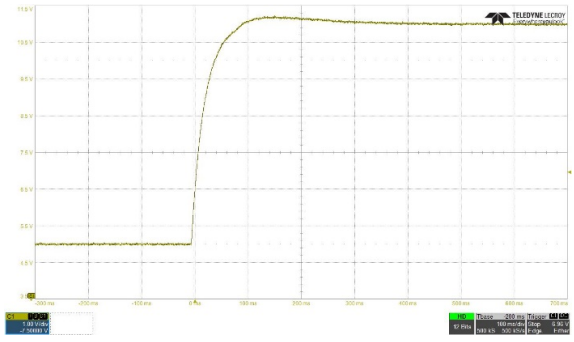


Figure 104. Voltage transition from 11 to 5 V at 230 V_{AC}- no load

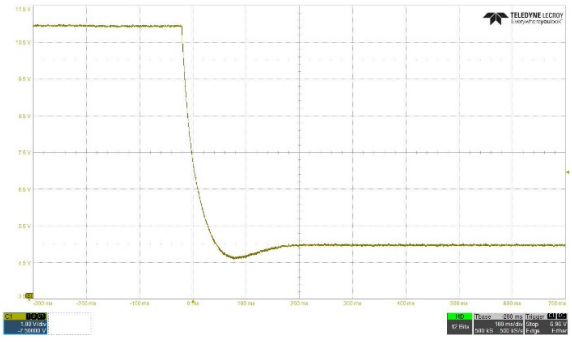


Figure 105. Voltage transition from 11 to 5 V at 230 V_{AC} - 2.4 A

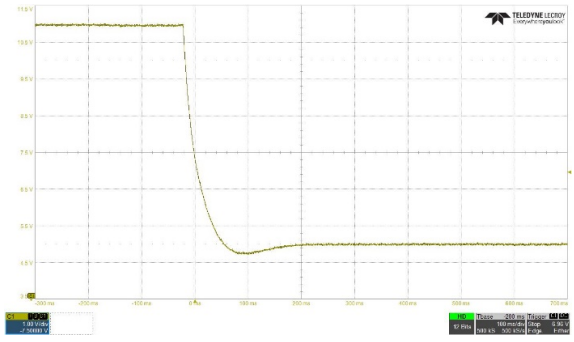


Figure 106. Voltage transition from 9 to 11 V at 230 V_{AC}- no load

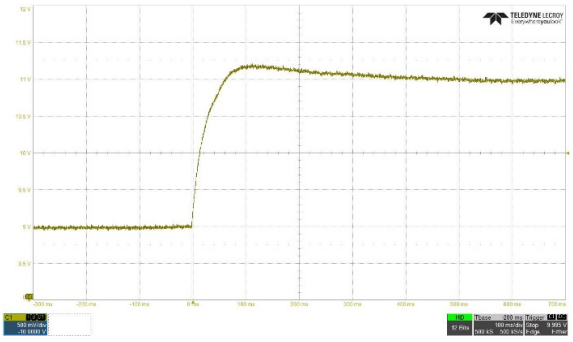


Figure 107. Voltage transition from 9 to 11 V at 230 V_{AC} - 2.4 A

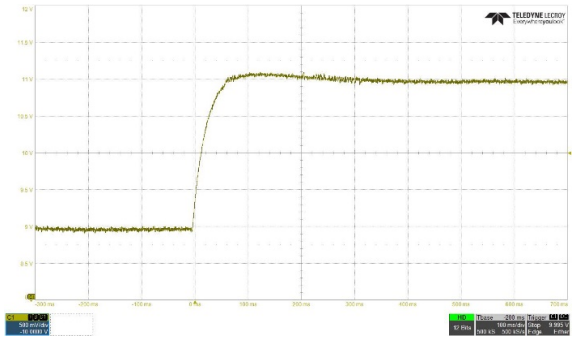


Figure 108. Voltage transition from 11 to 9 V at 230 V_{AC}- no load

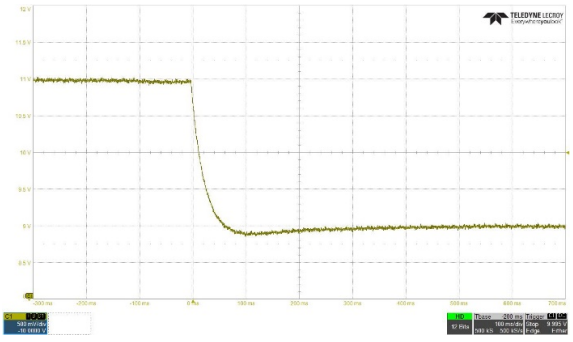
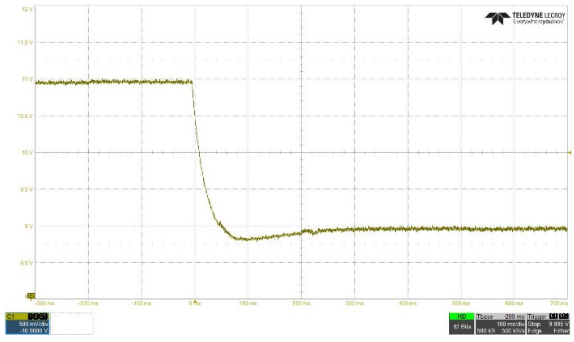


Figure 109. Voltage transition from 11 to 9 V at 230 V_{AC} - 2.4 A



3.3 PPS transitions

The STEVAL-USBPD27S is specifically designed to provide PPS profiles to control the output voltage, ensuring 20 mV steps during constant voltage operation and 50 mA steps during constant current operation.

Data listed below are based on the official “Universal Serial Bus Type-C and Power Delivery Source Power Requirements Test Specification” and, in particular, on the “SPT.6 PPS Voltage Step Test” which performs a sequence of voltage requests from the minimum to the maximum value of the requested APDO with different steps in terms of voltages and current:

- step size conditions:
  - 20 mV
  - 100 mV
  - 500 mV
- operating current conditions:
  - 1 A
  - APDO maximum current/2 + 500 mA
  - APDO maximum current

The tester applies 150 mA, 1.1 A and 2.25 A for each operating current condition. The current requested is lower than the operating current to avoid current limit operation.

Figure 110. **PPS voltage transition from 3.3 to 11 V at 230 V_{AC}, 150 mA**

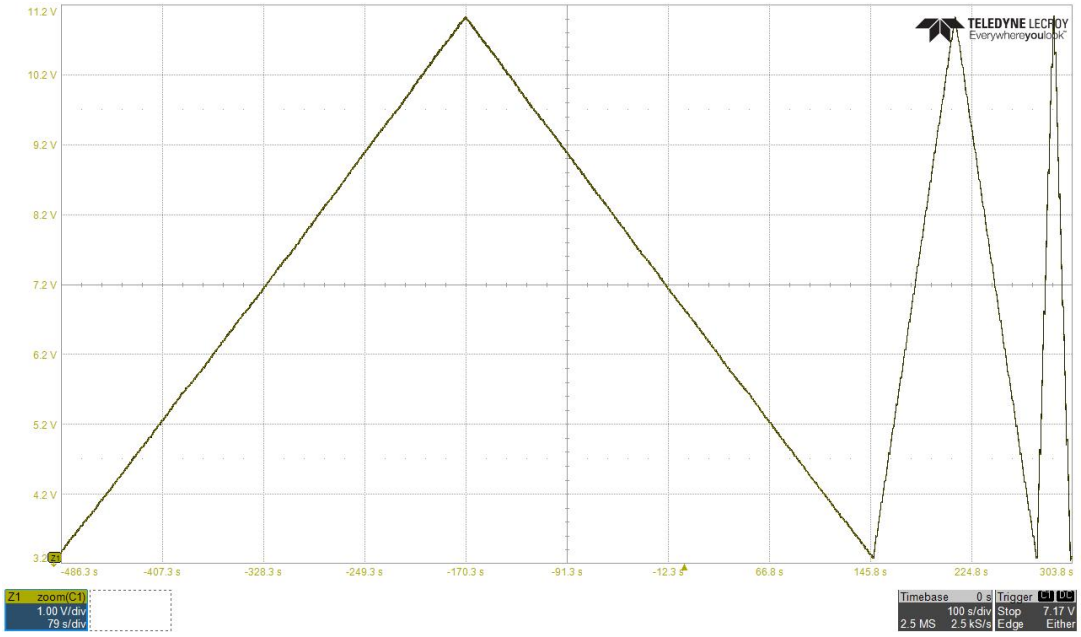


Figure 111. **PPS Voltage transition from 3.3 to 11 V at 230 V_{AC}, 1.1 A**

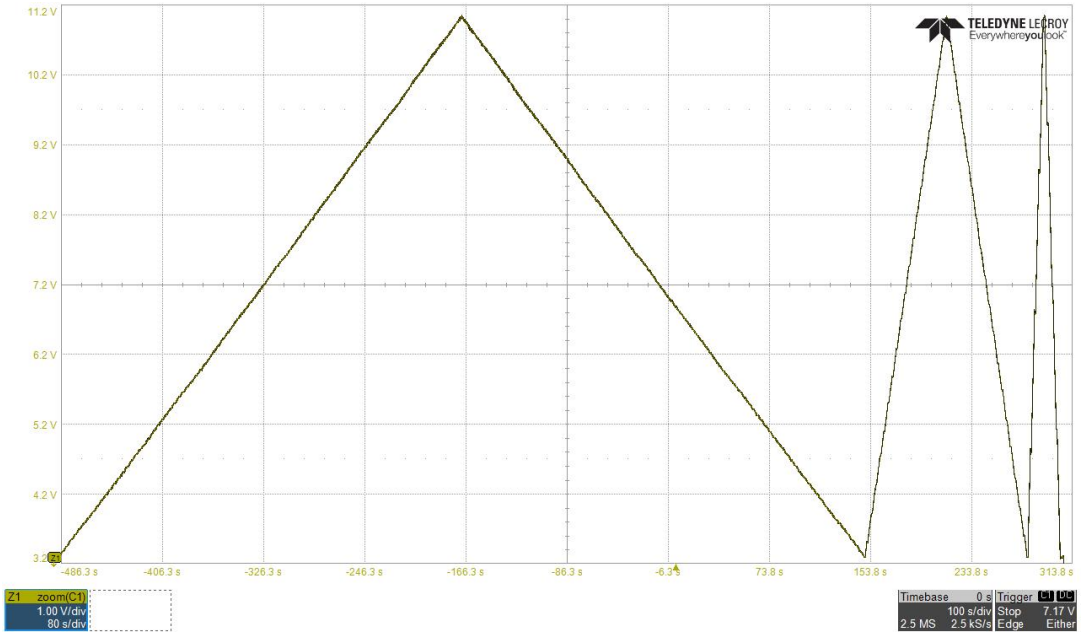
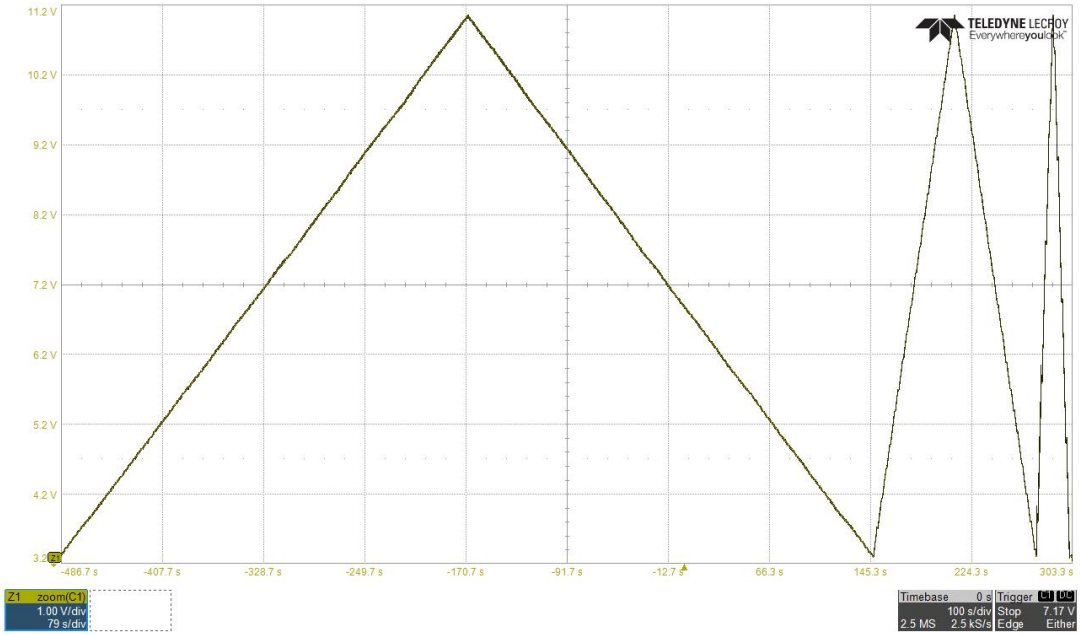


Figure 112. **PPS Voltage transition from 3.3 to 11 V at 230 V_{AC}, 2.25 A**



3.4 PPS current limit

Data listed herein are also based on the official “Universal Serial Bus Type-C and Power Delivery Source Power Requirements Test Specification" and, in particular, on the “SPT.7 PPS Current Limit Test” which performs a sequence of voltage requests and, for each request, increases the load with different current steps and operating current. When the load overcomes the operating current, the system enters Current Limit mode.

The following test conditions have been applied:

- operating current:
  - 1 A
  - (Current APDO max. current / 2) + 500 mA
  - Current APDO max. current
- operating voltage:
  - APDO min. voltage
  - (APDO min. voltage + APDO max. voltage)/2
  - APDO max. voltage
- Current step:
  - 500 mA
  - 100 mA
  - 50 mA

The following pictures show the Current Limit mode (formally a constant current operation) and data related to the two higher voltages tested using the smallest available current step (50 mA).

The first operating voltage condition, which implies the use of the available minimum voltage, is negligible for the board performance evaluation. Due to the low voltages requested by the tester, small load increases quickly activate Current Limit mode operation which tries to lower V_{BUS} and to force the system to Hard Reset as the output voltage is no longer valid (according to the specifications).

Data have been collected using an oscilloscope in XY configuration (output current vs output voltage) and a commercial tool, working as a sink. For further details, refer to AN5562, freely available on www.st.com.

Figure 113. **PPS current limit APDO1 (3.3 - 5.9 V at 5 A) - operating voltage = 4.6 V, operating current = 1 A**

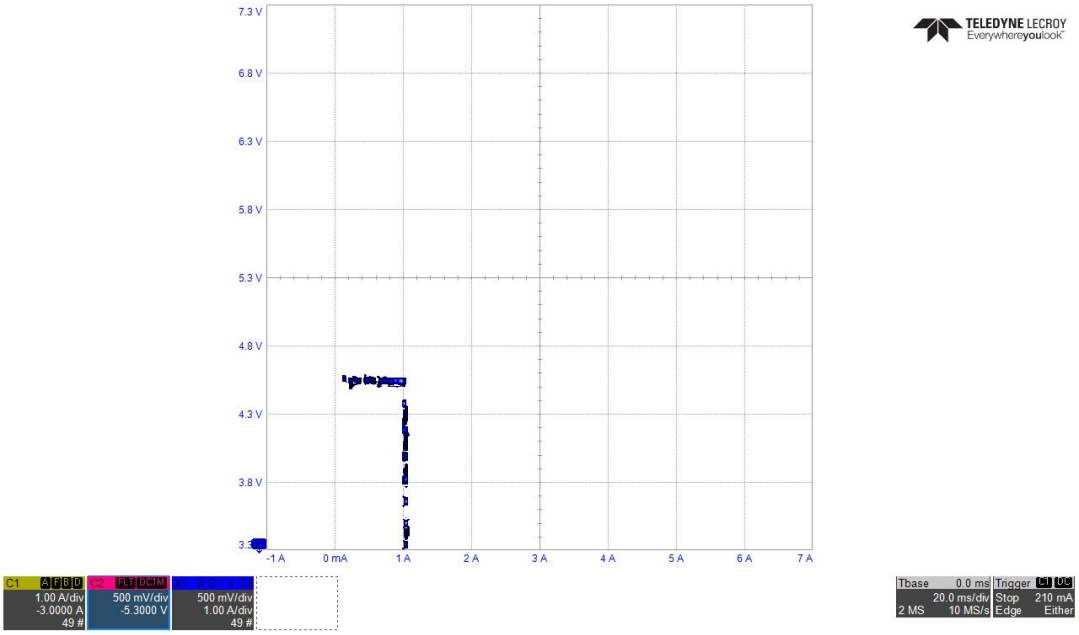


Figure 114. **PPS current limit APDO1 (3.3 - 5.9 V at 5 A) - operating voltage = 4.6 V, operating current = 3 A**

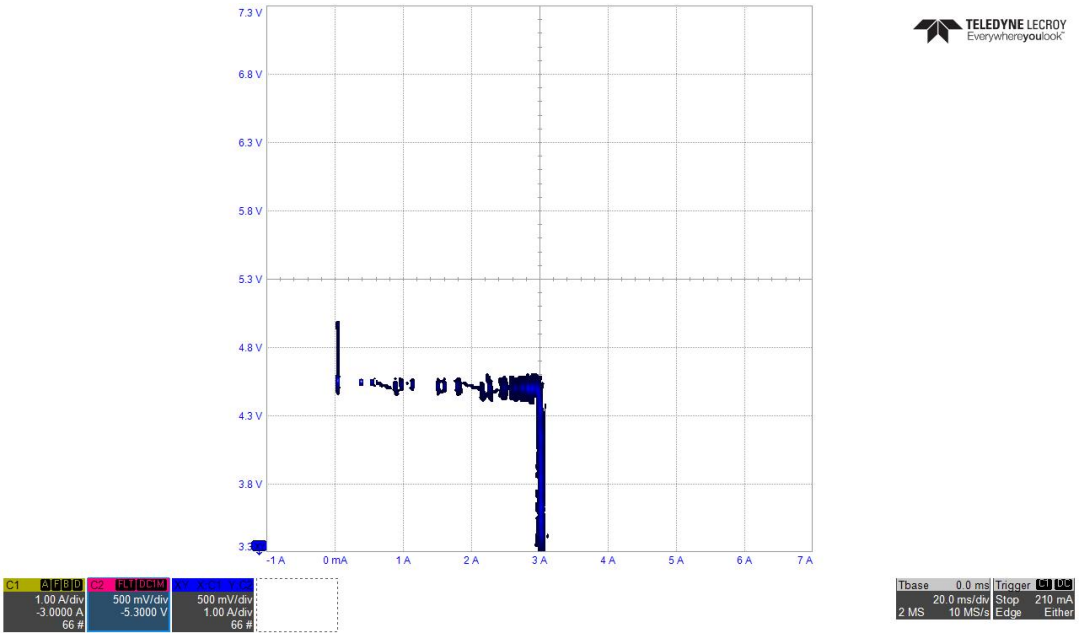


Figure 115. **PPS current limit APDO1 (3.3 - 5.9 V at 5 A) - operating voltage = 4.6 V, operating current = 5 A**

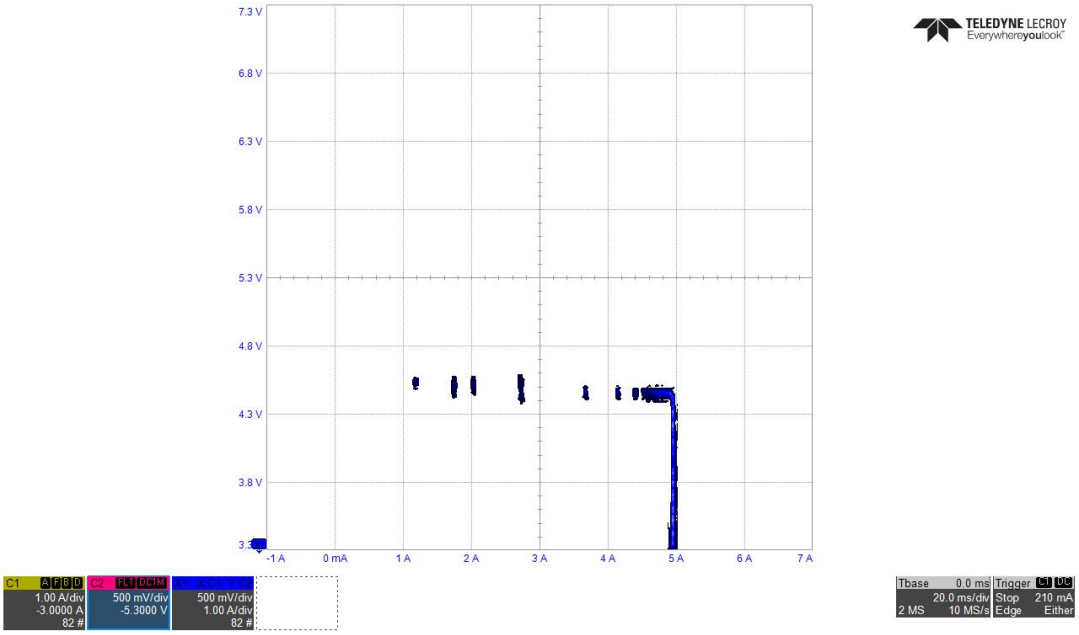


Figure 116. **PPS current limit APDO1 (3.3 - 5.9 V at 5 A) - operating voltage = 5.9 V, operating current = 1 A**

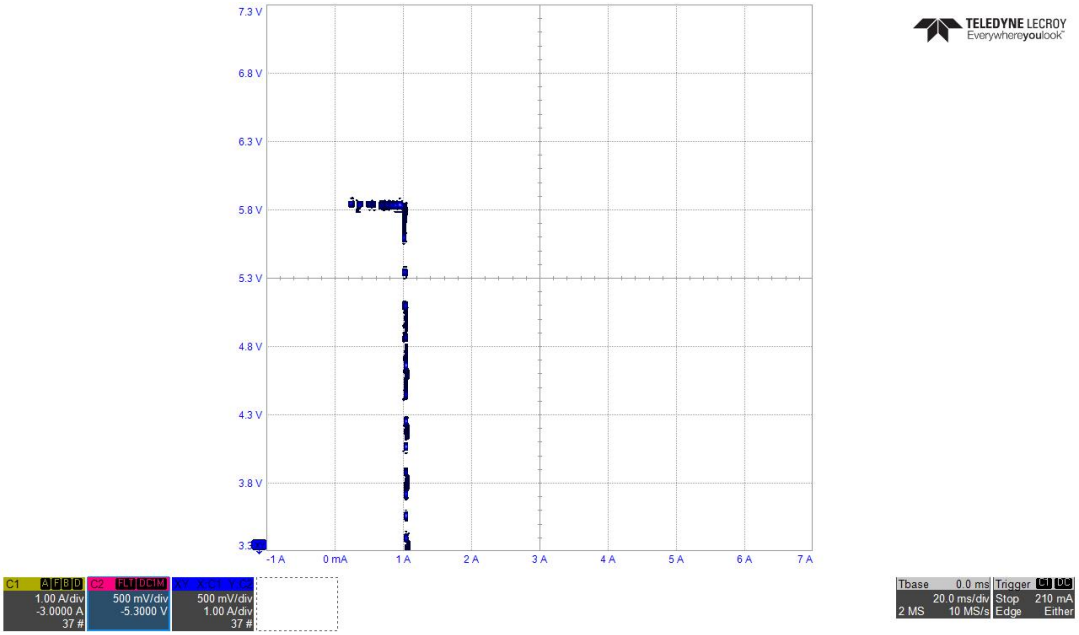


Figure 117. **PPS current limit APDO1 (3.3 - 5.9 V at 5 A) - operating voltage = 5.9 V, operating current = 3 A**

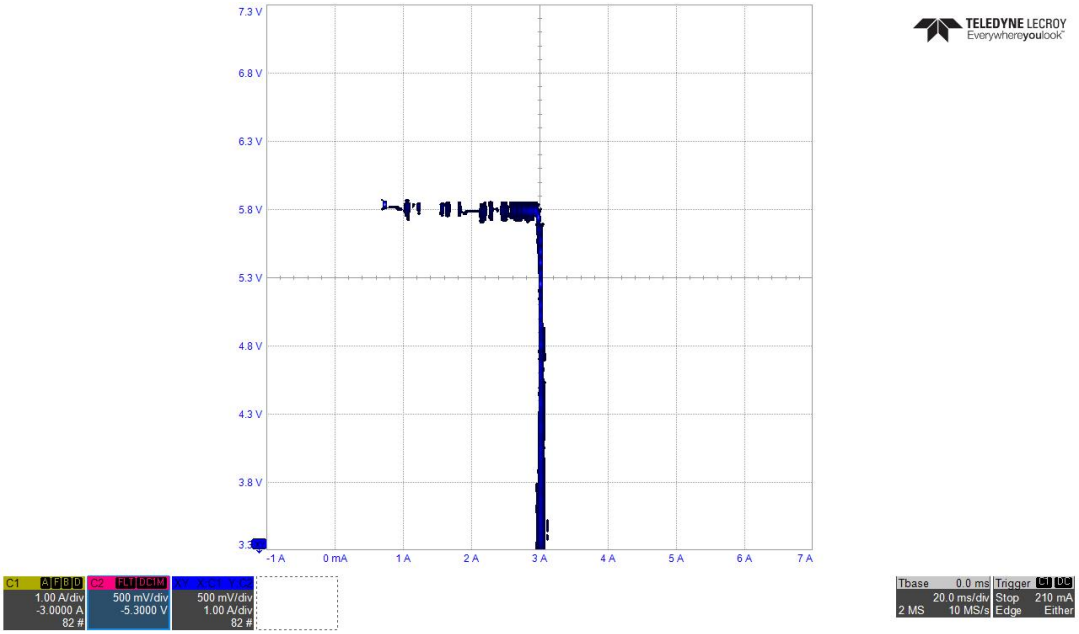


Figure 118. **PPS current limit APDO1 (3.3 - 5.9 V at 5 A) - operating voltage = 5.9 V, operating current = 5 A**

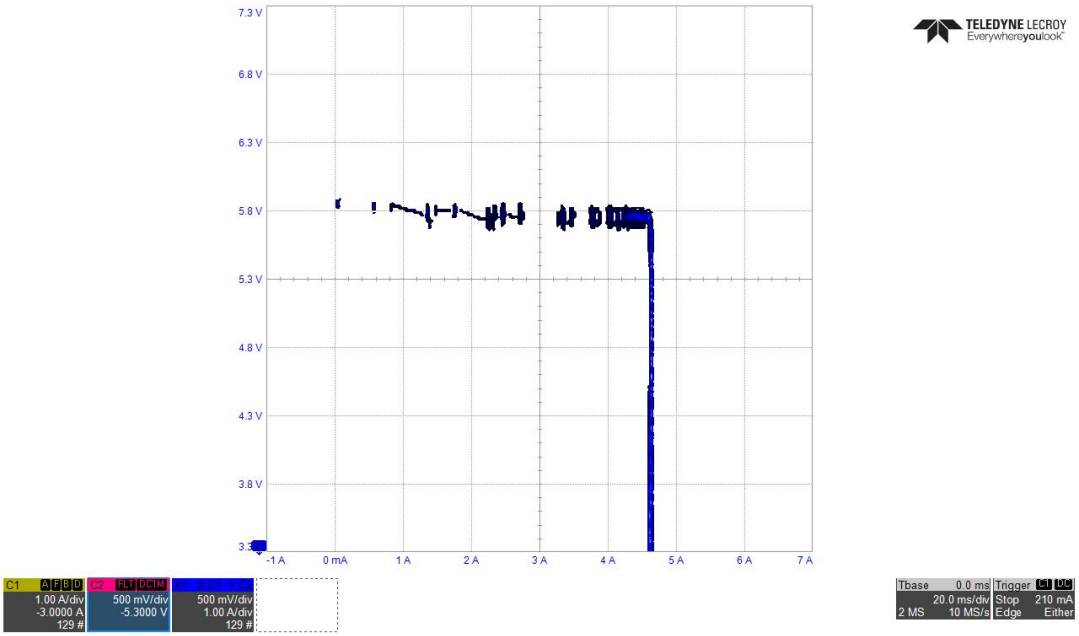


Figure 119. **PPS current limit APDO2 (3.3 - 11 V at 3 A) - operating voltage = 7.15 V, operating current = 1 A**

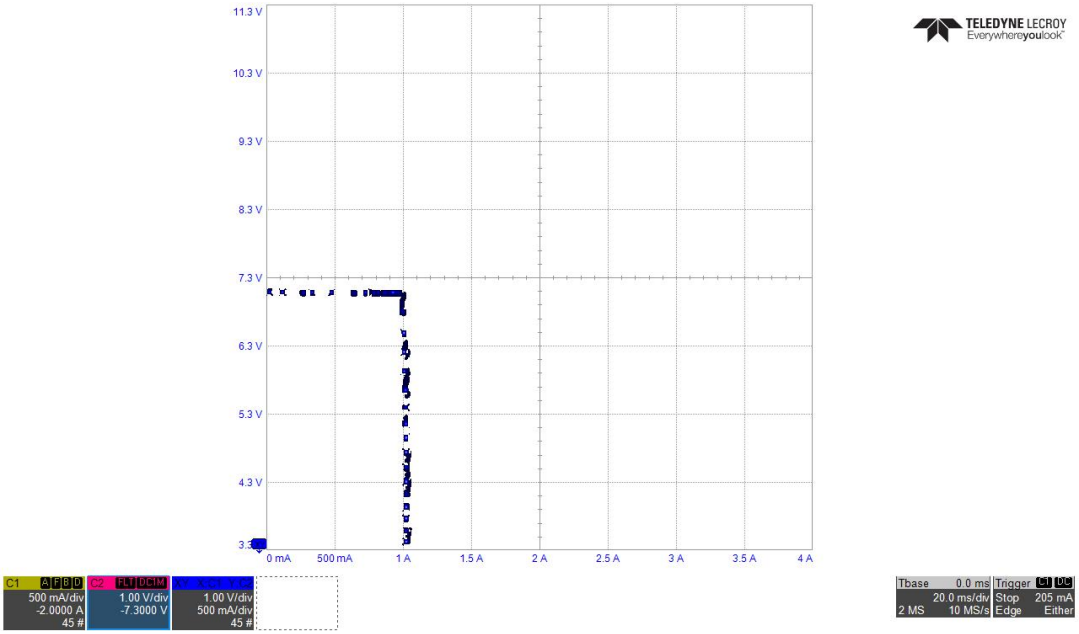


Figure 120. **PPS current limit APDO2 (3.3 - 11 V at 3 A) - operating voltage = 7.15 V, operating current = 2 A**

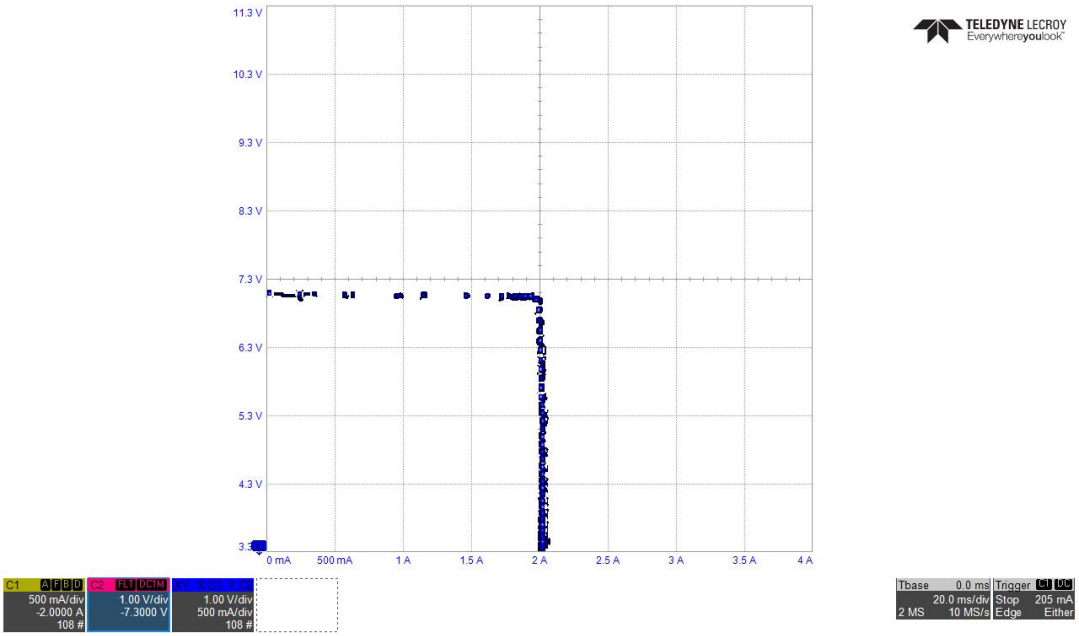


Figure 121. **PPS current limit APDO2 (3.3 - 11 V at 3 A) - operating voltage = 7.15 V, operating current = 3 A**

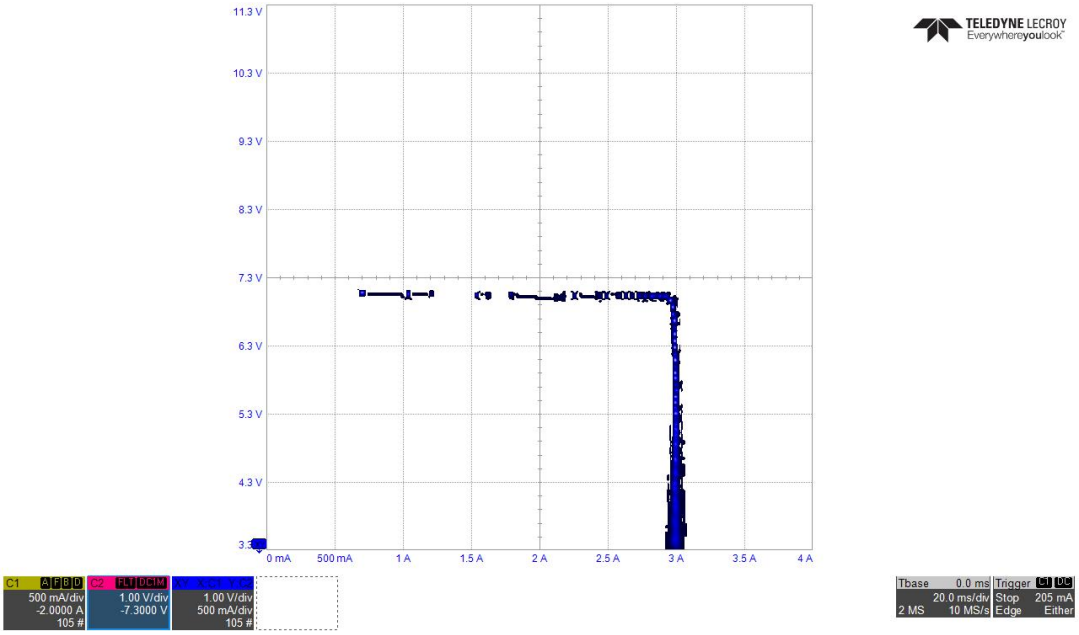


Figure 122. **PPS current limit APDO2 (3.3 - 11 V at 3 A) - operating voltage = 11 V, operating current = 1 A**

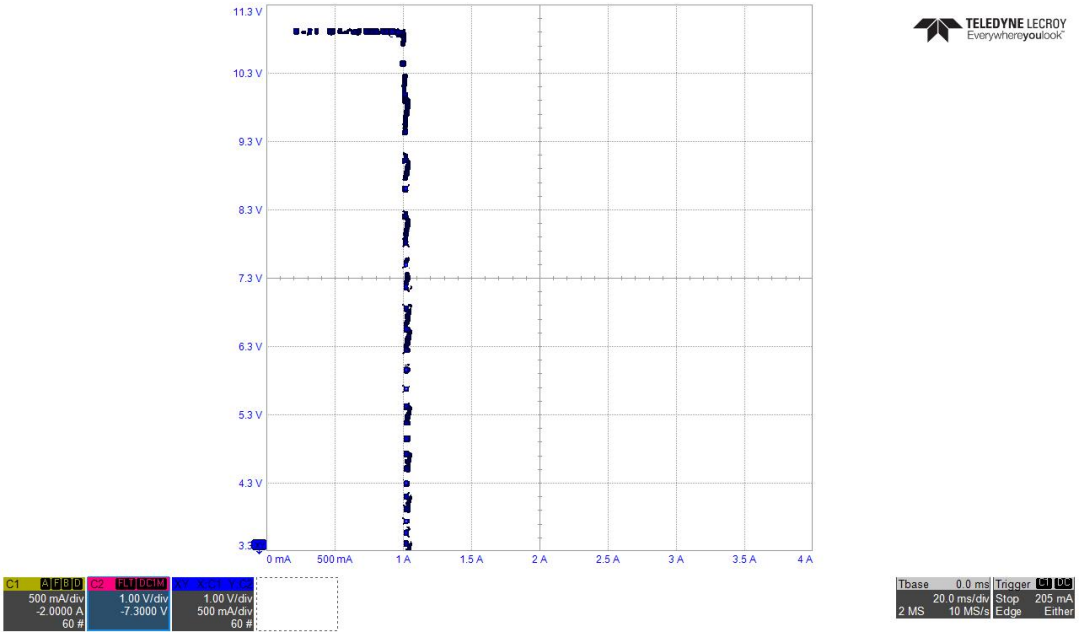


Figure 123. **PPS current limit APDO2 (3.3 - 11 V at 3 A) - operating voltage = 11 V, operating current = 2 A**

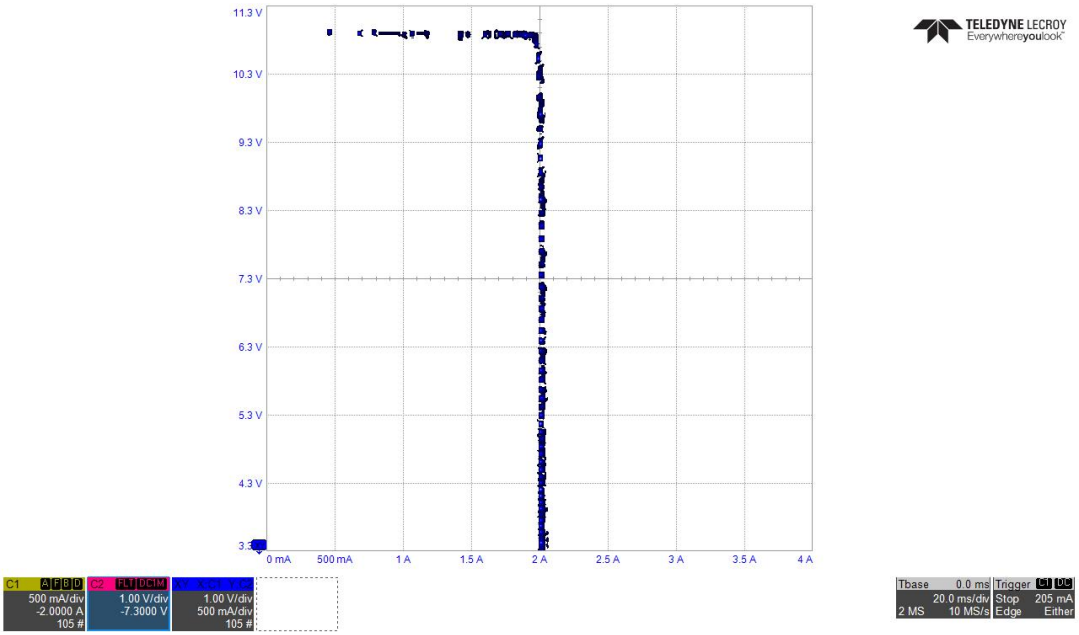
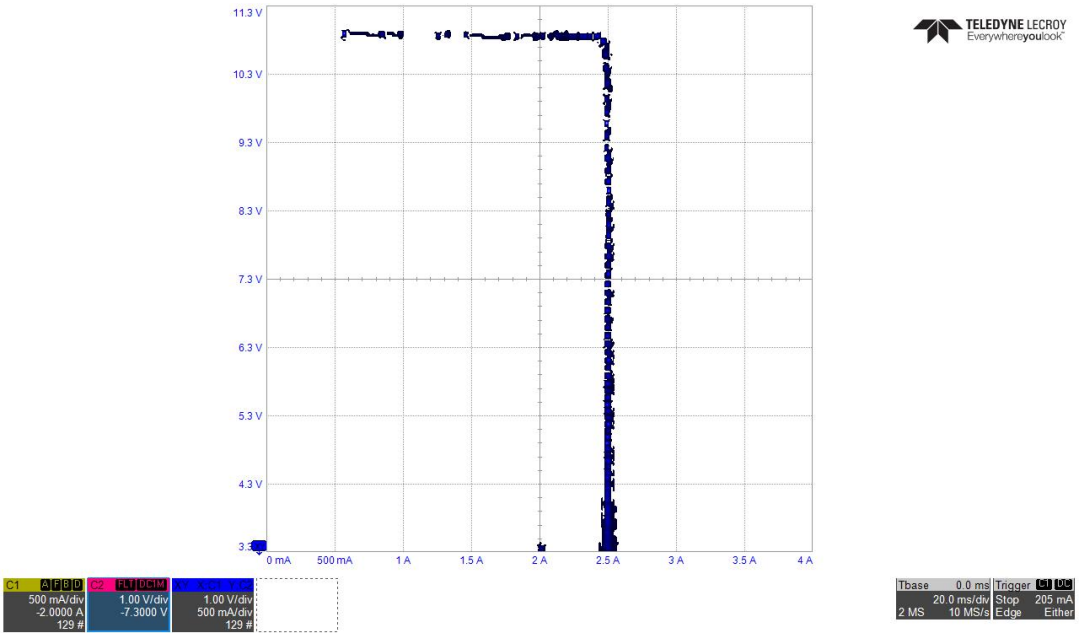


Figure 124. **PPS current limit APDO2 (3.3 - 11 V at 3 A) - operating voltage = 11 V, operating current = 2.45 A**



3.5 USB-IF PD compliance

The STEVAL-USBPD27S compliance with USB Type-C and USB Power Delivery specifications is certified by USB-IF as power brick with TID 5445. The on-board STM32G071KBU6N is certified as PD controller with TID 5444.

Table 2. USB PD official compliance test equipment

Tool name	Software	SW version
Ellisys USB Explorer 350	USB Explorer 350 Examiner	v.3.1.7488 v.3.1.7332
Teledyne LeCroy Voyager M310P	USB Compliance Suite USB Protocol Suite	v.5.01 Build 950 v.8.55 Build 3715
QuadraMAX	QuadDraw QuadraView	v.0.8.7523 v.0.8.7523

4 Efficiency measurements

In this power efficiency analysis, a commercial tool, working as sink, is used to request the power profiles offered by the STEVAL-USBPD27S and to sink the desired current. A Yokogawa WT110 digital power meter has been used to measure the power delivered to the STEVAL-USBPD27S adapter.

The output voltage has been measured at board end (on top of capacitor C24), while the current is measured by the sink. Measurements have been performed by removing RT1 NTC and after a burn-in period of 30 minutes.

A board has been selected, among a batch of 50 prototypes, to perform the following measurements. The selected board is the one with the best performance.

4.1 Four-point average efficiency

The minimum four-point average efficiency in active mode is compliant with CoC - Tier 2 and DOE requirements.

Table 3. Minimum four-point average efficiency in active mode

V_{AC} [V]	V_{OUT}[V]	Efficiency [%]	Target [%]	Δ [%]
115 at 60 Hz	3.3	86.51	82.47	4.04
	5	87.74	85.00	2.75
	5.9	88.01	85.42	2.59
	9	88.90	87.30	1.60
	11	88.60	87.30	1.31
230 at 50 Hz	3.3	84.76	82.47	2.30
	5	86.91	85.00	1.91
	5.9	88.42	85.42	3.00
	9	88.05	87.30	0.75
	11	87.78	87.30	0.48

4.2 10% efficiency

The average efficiency in active mode at 10% load of full rated output current is summarized in the table below.

Table 4. Average efficiency in active mode at 10% load

V_{AC} [V]	V_{OUT} [V]	Efficiency [%]	Target [%]	Δ [%]
115 at 60 Hz	3.3	83.90	73.08	10.82
	5	85.44	75.47	9.97
	5.9	84.97	75.86	9.11
	9	84.35	77.30	7.06
	11	82.20	77.30	4.91
230 at 50 Hz	3.3	75.48	73.08	2.40
	5	78.20	75.47	2.73
	5.9	78.33	75.86	2.47
	9	77.92	77.30	0.63
	11	76.33	77.30	-0.96

All profiles are compliant with CoC - Tier 2 requirements except for the 11 V output available on the 9 VProg at 3 A profile.

4.3 Standby consumption

The STEVAL-USBPD27S standby consumption data have been acquired with the kit supplied and no consumer attached. The solution is compliant with CoC - Tier 2.

Table 5. STEVAL-USBPD27S standby consumption

V_{AC} [V]	P_{IN} [mW]	Target [mW]	Δ [mW]
115 at 60 Hz	<30	<75	45
230 at 50 Hz	<40		35

5 Thermal measurements

A thermal analysis of the board has been performed with an infrared thermal imaging camera. The test was conducted with the output voltage profile selected to 9 V under full load condition. The board has been submitted to the minimum and maximum voltages, 90 V_{AC} and 265 V_{AC}.

Figure 125. Thermal image at 90 V_{AC}, out: 9 V – 3 A (T_{AMB} = 25°C) - top view

HS1=107.3°C, HS2=86.1°C

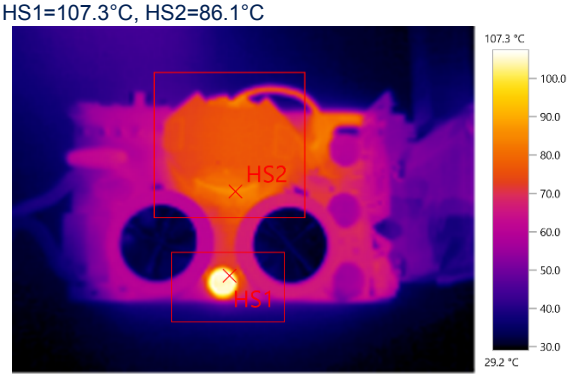


Figure 126. Thermal image at 90 V_{AC}, out: 9 V – 3 A (T_{AMB} = 25°C) - side view

HS1=108.1°C, HS2=89.1°C

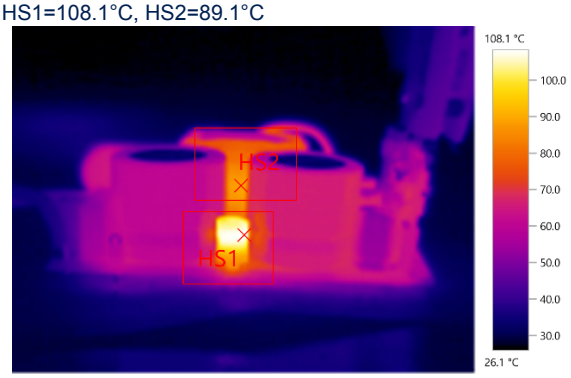


Figure 127. Thermal image at 90 V_{AC}, out: 9 V – 3 A (T_{AMB} = 25°C) - side view

HS1=87.4°C

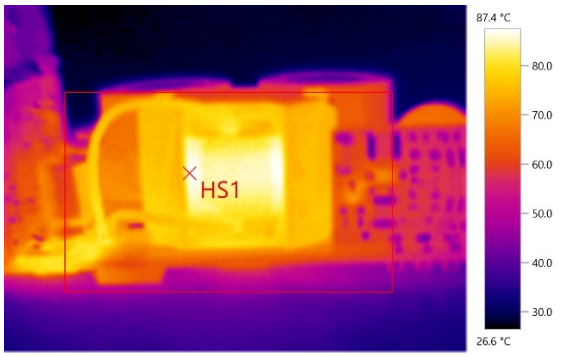


Figure 128. Thermal image at 90 V_{AC}, out: 9 V – 3 A (T_{AMB} = 25°C) - STM32 board view

HS1=73.4°C, HS2=62.4°C, HS3=68.1°C

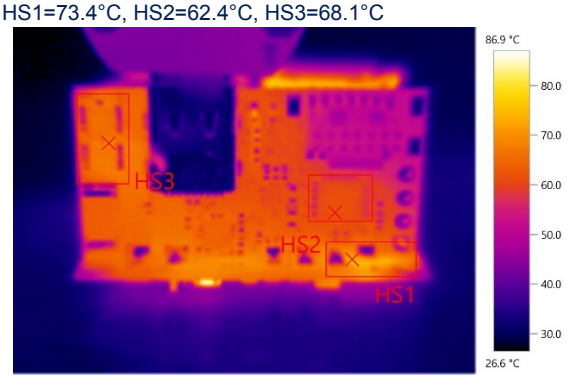


Figure 129. Thermal image at 90 V_{AC}, out: 9 V – 3 A (T_{AMB} = 25°C) - STCH03 board view

HS1=71.5°C

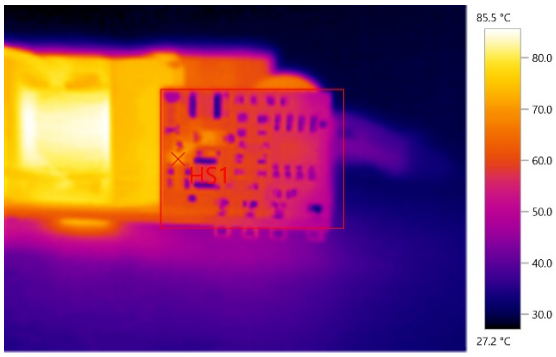


Figure 130. Thermal image at 90 V_{AC}, out: 9 V – 3 A (T_{AMB} = 25°C) - bottom view

HS1=78.1°C, HS2=87.8°C, HS3=88°C, HS4=90.1°C

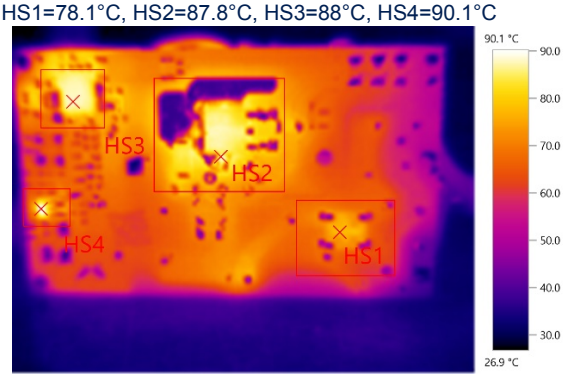


Figure 131. Thermal image at 265 V_{AC}, out: 9 V – 3 A (T_{AMB} = 25°C) - top view

HS1=98.2°C, HS2=87.4°C

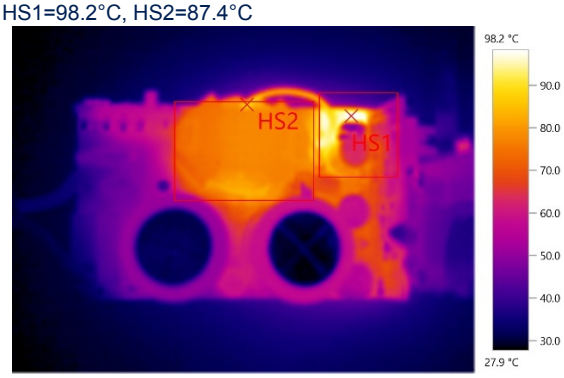


Figure 132. Thermal image at 90 V_{AC}, out: 9 V – 3 A (T_{AMB} = 25°C) - side view

HS1=88.9°C

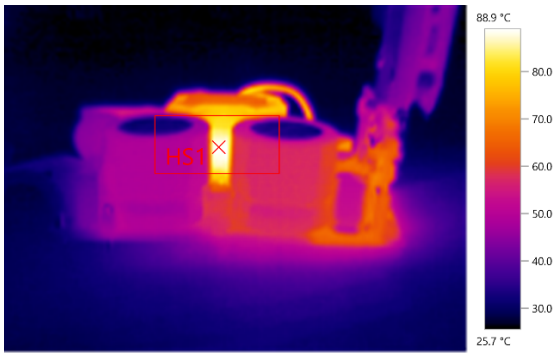


Figure 133. Thermal image at 265 V_{AC}, out: 9 V – 3 A (T_{AMB} = 25°C) - side view

HS1=88.8°C, HS2=88.5°C

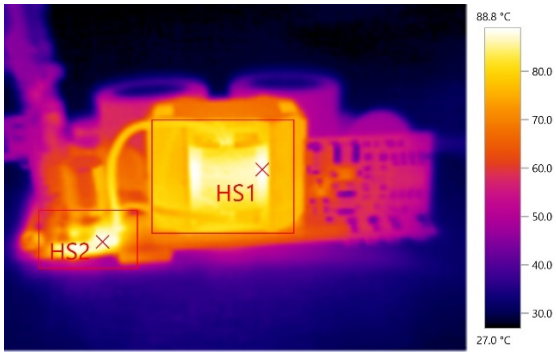


Figure 134. Thermal image at 90 V_{AC}, out: 9 V – 3 A (T_{AMB} = 25°C) - STM32 board view

HS1=88.1°C, HS2=66°C, HS3=67.2°C

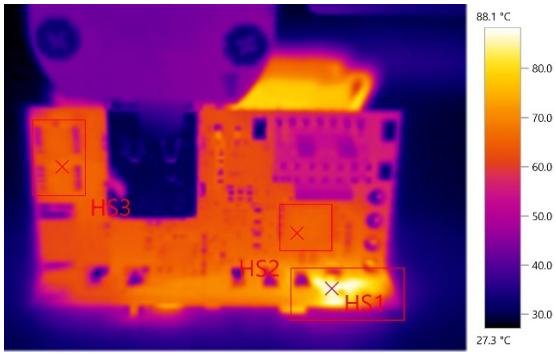


Figure 135. Thermal image at 265 V_{AC}, out: 9 V – 3 A (T_{AMB} = 25°C) - STCH03 board view

HS1=68.2°C

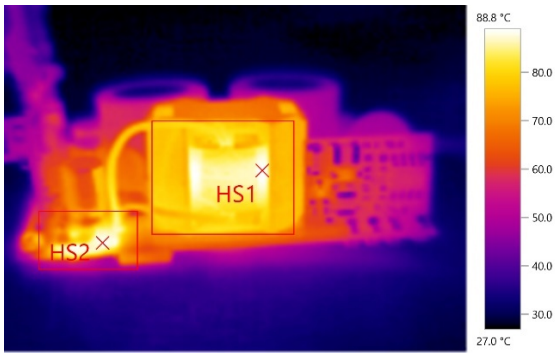
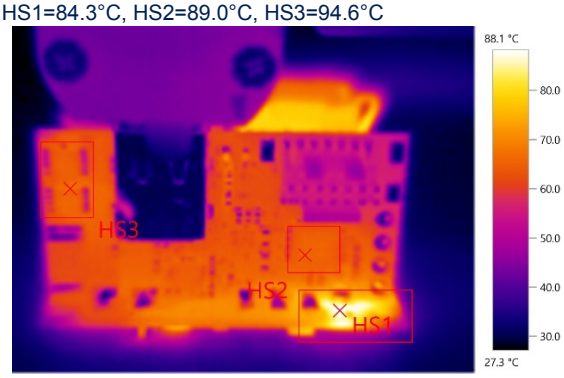


Figure 136. Thermal image at 90 V_{AC}, out: 9 V – 3 A (T_{AMB} = 25°C) - bottom view

HS1=84.3°C, HS2=89.0°C, HS3=94.6°C



Important:
To increase thermal dissipation, it is recommended to fill the internal components with thermal silica gel, apply thermal pads and use a large metal heatsink around the board body.

6 EMI measurements

The STEVAL-USBPD27S has been tested to verify conducted noise emissions and compliance with the EN55022 (Class B) standard using average detectors with input voltages of 115 V_{AC} and 230 V_{AC}. Tests have been carried out with a commercial tool, working as sink, used to request power profiles and to sink the desired current.

The tests have been performed at half and full power requesting both 9 V PDO (to reach the maximum power) and 5 V PDO (o reach the maximum current available, 5 A).

Agilent E7402A EMC Spectrum Analyzer, EMCO MODEL 3816/2 LISN and ARCOL VRH320 10R – 5.7 A variable wire resistor have been used.

Conducted tests demonstrate that the STEVAL-USBPD27S is compliant with EN55022 (Class B) standard.

Figure 137. Conducted noise emissions at 115 V_{AC} (output: 9 V - 1.5 A) - online

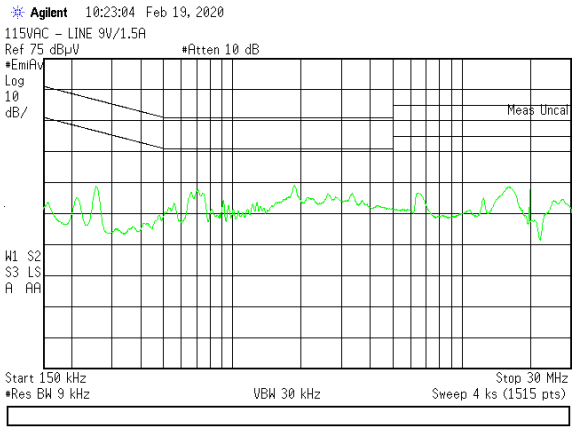


Figure 138. Conducted noise emissions at 115 V_{AC} (output: 9 V - 1.5 A) - neutral

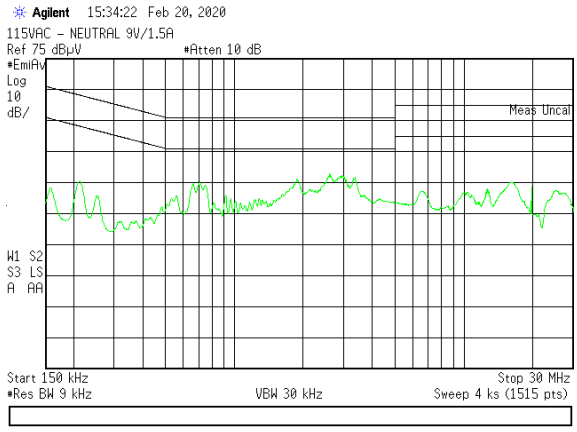


Figure 139. Conducted noise emissions at 115 V_{AC} (output: 9 V - 3 A) - online

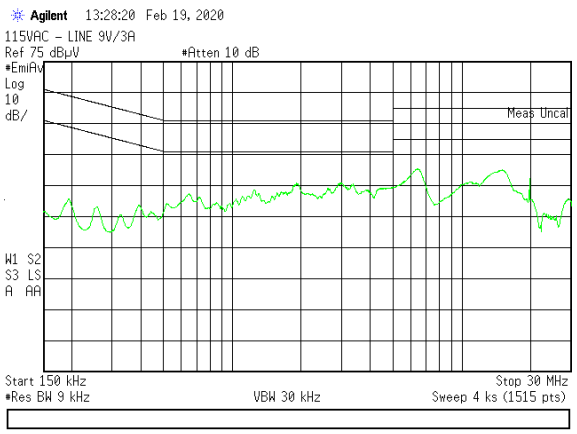


Figure 140. Conducted noise emissions at 115 V_{AC} (output: 9 V - 3 A) - neutral

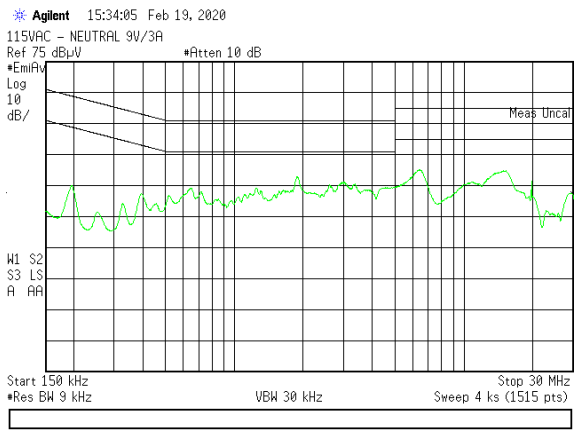


Figure 141. Conducted noise emissions at 115 V_{AC} (output: 5 V - 2.5 A) - online

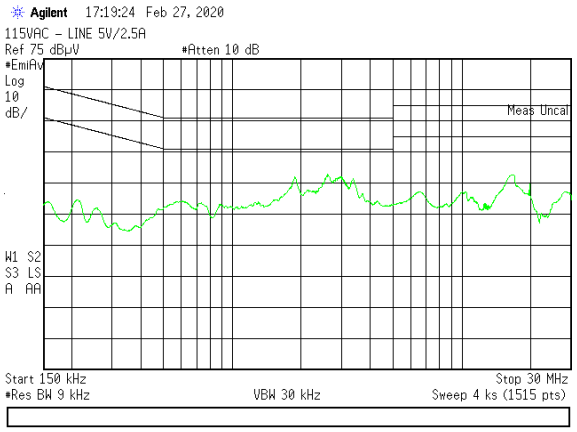


Figure 142. Conducted noise emissions at 115 V_{AC} (output: 5 V - 2.5 A) - neutral

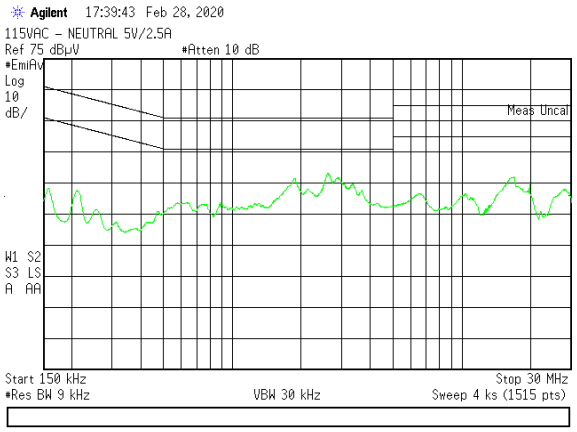


Figure 143. Conducted noise emissions at 115 V_{AC} (output: 5 V - 5 A) - online

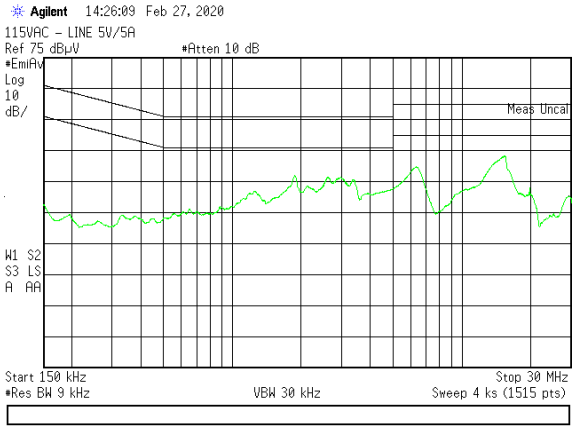


Figure 144. Conducted noise emissions at 115 V_{AC} (output: 5 V - 5 A) - neutral

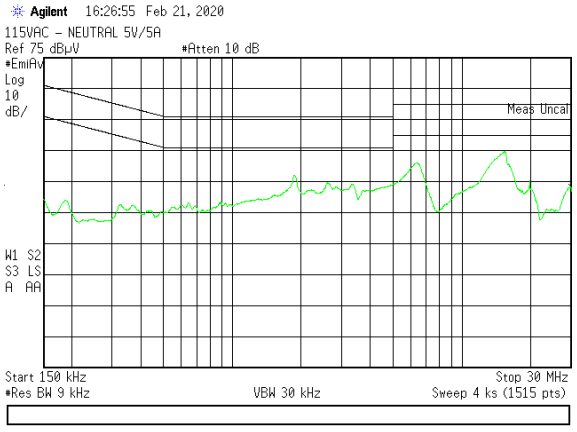


Figure 145. Conducted noise emissions at 230 V_{AC} (output: 9 V - 1.5 A) - online

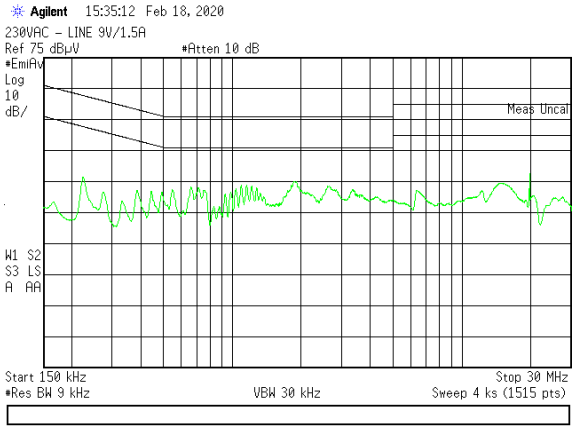


Figure 146. Conducted noise emissions at 230 V_{AC} (output: 9 V - 1.5 A) - neutral

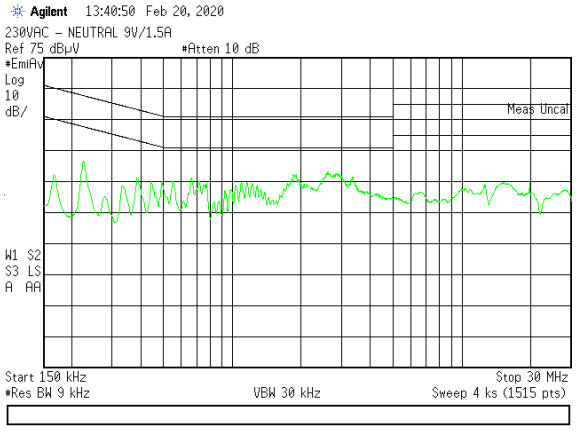


Figure 147. Conducted noise emissions at 230 V_{AC} (output: 9 V - 3 A) - online

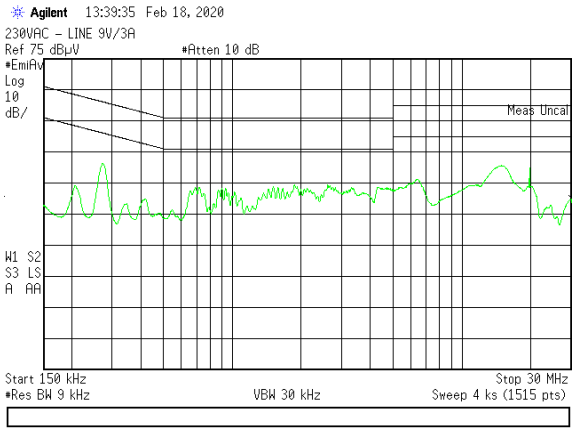


Figure 148. Conducted noise emissions at 230 V_{AC} (output: 9 V - 3 A) - neutral

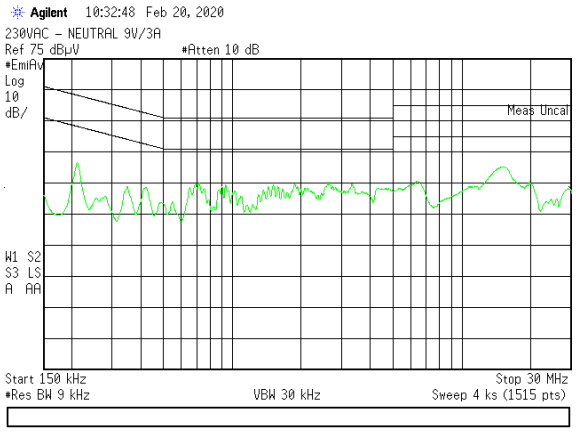


Figure 149. Conducted noise emissions at 230 V_{AC} (output: 5 V - 2.5 A) - online

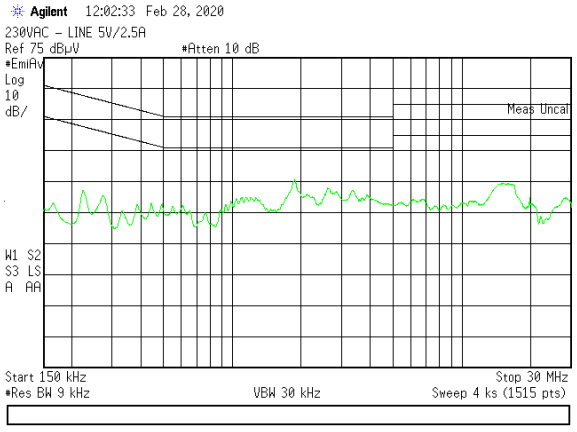


Figure 150. Conducted noise emissions at 230 V_{AC} (output: 5 V - 2.5 A) - neutral

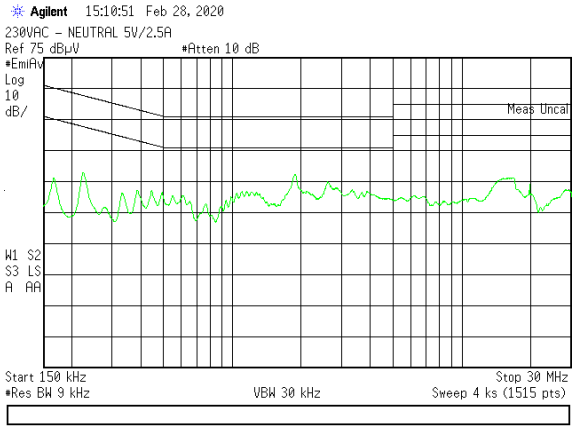


Figure 151. Conducted noise emissions at 230 V_{AC} (output: 5 V - 5 A) - online

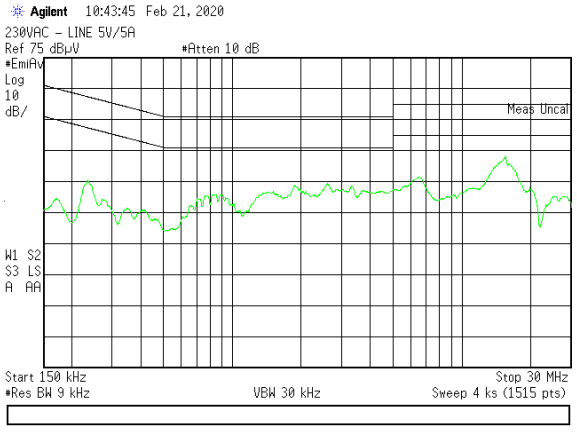
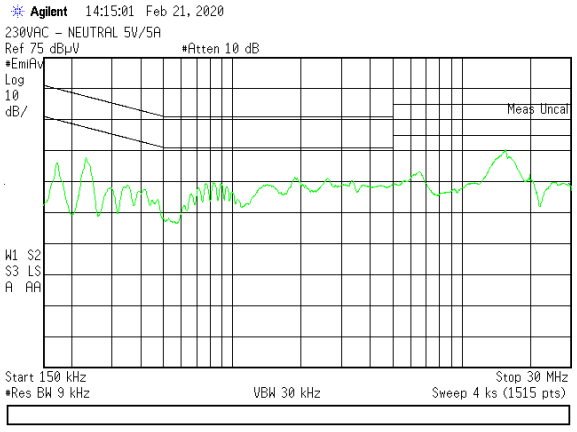


Figure 152. Conducted noise emissions at 230 V_{AC} (output: 5 V - 5 A) - neutral



7 Conclusions

The test results shown demonstrate the good performances achieved by the STEVAL-USBPD27S.

The board design is robust and reliable from an electrical point of view. The AC-DC stage works in safe and comfortable conditions, ensuring tight output voltage regulation under any condition.

Performed power related tests demonstrate that the STEVAL-USBPD27S is compliant with USB PD 3.1 and CoC - Tier 2 and DOE Efficiency Requirement.

The board is also compliant with the EN55022 (Class B) standard related to conducted noise emissions using average detectors.

Revision history

Table 6. **Document revision history**

Date	Version	Changes
28-Oct-2020	1	Initial release.
05-Nov-2020	2	Updated Section 3.5 USB-IF PD compliance.
16-Mar-2021	3	Updated Section 4.1 Four-point average efficiency and Section 4.2 10% efficiency.
01-Sep-2021	4	Updated Section 3.2 Voltage transitions across all profiles, Section 3.5 USB-IF PD compliance and Section 7 Conclusions.

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