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**List of software parameters to check in
case of switch:**

From M24128S-FCU to M24128X-FCU

- This document provides a list of software parameters to check in case of switch from M24128S-FCU to M24128X-FCU.

List of software parameters to check

Parameter	M24128S-FCU	M24128X-FCU	Action needed	Remarks
Datasheet	 M24128S-FCU	 M24128X-FCU	FYI	Available on ST.COM web site : - M24128S-FCU - M24128X-FCU
Chip enable address	Fixed : 001	Default : 000	Yes	At factory delivery not compatible, but M24128X offers the configurable chip enable address C2,C1,C0 (factory delivery value = 000). The chip enable address (C2,C1,C0) can be modified in the chip enable register. The register can be written & read with specifics command “write chip enable register“ & “read chip enable register“.
Software Write Protect register	Available (Protection by quarter)	Available (Protection of full plan)	Yes	M24128S offers the software write protection by <u>quarter</u> with the <i>write protect register</i> . M24128X offers the software write protection on the <u>entire</u> memory(not by quarter) with <i>the chip enable register</i> . Same address for both register (1xxx.xxxx.xxxx.xxxx) On M24128X, the software write protection is managed by SWP bit only. When SWP=0, the memory is not protected against update. When SWP=1 the memory is fully protected against update. Updating the SWP to a new value is a reversible action.
Chip enable register management	Not Available	Available	Yes	With the M24128X, the user writes & reads the <i>chip enable register</i> with the specific commands “write chip enable register” & ”read chip enable register”. Can be updated: - The C2,C1,C0 bits for the chip enable address - The SWP bit for the protection of the memory array

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