Study of gate leakage mechanism in advanced charge-coupled MOSFET (CC-MOSFET) technology

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Abstract

In this work we present an alternative method to evaluate the ability to charge trap of the thermal silicon oxide grown on n+-polysilicon in charge-coupled MOSFET devices. By interpreting the current conduction mechanism through the polysilicon-oxide by Frenkel–Poole model, we were able to evaluate and quantify the amount of charge trapped in it. We propose this approach as a very simple methodology to recognize the properties and quality of insulation of the thermal silicon oxide grown on n+-polysilicon devices.

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1. Introduction

As the demand for low power and fast switching Power MOSFET in the low-voltage wireless application is rapidly increasing, the introduction of charge-coupled MOSFET (CC-MOSFET) has enabled Si Power MOSFET technology roadmap to be further "scaled" to meet the demand [1,2]. Unlike conventional Power MOSFET where gate leakage (IGSS) current is through gate oxide, charge coupling MOSFET (CC-MOSFET) has an additional leakage path through the inter-poly oxide. CC-MOSFET devices require an additional insulation between gate and source electrodes. It is expected that the polyoxide between the two electrodes should have low leakage current and high dielectric breakdown. However it is well known that thermal oxide grown on n⁺—polycrystalline highlight a high leakage current due to the thickness uniformity [3] and local field enhancement [4–6] at the polysilicon—polyoxide interface. The electrical polyoxide properties have been shown to be largely dependent on process fabrication like poly deposition temperature doping process, and thermal oxidation method [7–8]. In this paper we analyze the transport carrier mechanism through the polyoxide layer by the Frenkel–Poole model. Using the Frenkel-Poole model we are able to find the trapped charge density into the polyoxide layer responsible of the barrier height reduction and the gate current leakage reduction after gate voltage pulse.

2. Experimental

CC-MOSFET (Area ~ 8 mm²) device was fabricated as Fig. 1 shows. Gate oxide was thermally grown with a thickness of 47nm while inter-poly oxide layer was 150 nm. The buried n⁺ poly-Si and gate electrode n⁺ poly are deposited with the same recipe at 600 °C and highly doped. Together with the CC-MOSFET, a separate DUT (Area ~ 0.04 mm²) structure was fabricated which has buried poly electrically disconnected from the source electrode as Fig. 2 shows.
With this DUT, we are able to decouple the individual contribution (leakage from gate oxide or inter-poly oxide) to total leakage and subsequently, monitored by IGSS measurements.

3. Results

Fig. 3 shows the I–V characteristics of CC-MOSFET with high IGSS issue.

To decouple the dominant leakage path, further I–V characteristics were performed on the DUT (see Fig. 4).

The IGSS current was dominated by inter-poly oxide which highlights a bad insulation property. This is well-supported by the behavior of the inter-poly oxide current when a rectangular pulse signal was applied on the gate electrode. Fig. 5 shows 12 different virgin CC-MOSFETs on which we had applied a rectangular pulse signal on the gate electrode with a pulse height (from 10 V to 22 V). Every pulse reduces the IGSS and pushes the onset of tunneling leakage to higher $V_{\text{Gate}}$ due to the charge trapped into the polyoxide.

The polyoxide leakage decreases after every rectangular pulse because the trapped charge into the polyoxide dielectric is an electrostatic shield to the electrons injected during the next pulse. If $E_{\text{inj}}$ is the electrical field injection without charge trapped, $E_{\text{eff}}$ is the effective electrical field which electrons injected into polyoxide feeling due to the presence of the electrical charge trapped during the previous pulse. We can describe this effect by the equation:

$$E_{\text{eff}} = \frac{E_{\text{inj}}}{\varepsilon_0 \varepsilon_{\text{ox}}}$$

where $n_T$ is the trapped charge density, $\varepsilon_0$ and $\varepsilon_{\text{ox}}$ are the vacuum permittivity and the oxide dielectric constant respectively and $x^*$ is the effective centroid of the trapped charge.

The fresh curve in Fig. 5 refers to virgin device so that we can suppose that they are initially empty, without charge trapped. The other I–Vs refer to curves which have trapped some amount of charge due to gate voltage pulse.

The main transport mechanism through the polyoxide is depicted by Frenkel–Poole model because the trapped charge is dependent from the temperature. In fact Fig. 6 shows an example of recovery of the electrical...
characteristics by the temperature after a rectangular gate voltage pulse of 30 V (10 ms). If we hold the device under storage at high temperature (150 °C) for ~1000 h it is possible to recover completely the original high gate leakage current (fresh device).

The annealing at low temperature was performed without polarization so that the electrons emission were not stimulated from any electric field.

The Frenkel–Poole transport is modeled by

$$ J \sim \frac{E}{C_24} \frac{e}{C_0} \frac{q}{q} \frac{\phi_B}{\phi_B} \frac{K_T}{C_0/C_1} \sqrt{1} $$

where $\phi_B$, $q$, $T$ and $K$ are the trap barrier height, the elementary charge and the Boltzmann respectively and $\Delta \phi_B$ is given:

$$ \Delta \phi_B = \sqrt{qE \pi \varepsilon_\text{o} \varepsilon_\text{ox} x} $$

where, $E$, $\varepsilon_\text{o}$, and $\varepsilon_\text{ox}$ are, the electric field at the interface of the poly/polyoxide stack, the oxide dielectric constant, and the permittivity of vacuum, respectively.

In the first approximation we can suppose that the external pulse does not change the barrier height $\phi_B$ but modify $\Delta \phi_B$ because the state of occupation of the traps change so that initially the polyoxide will be much more conductive because we will have a large number of empty or neutral traps, but little by little the traps will be filled and the current leakage should reduce because we will have progressively saturated some amount of traps and reduced some preferential conductive paths through the polyoxide.

Supposing that close the poly/polyoxide interface the field electric is:

$$ E = E_\text{ext} + \frac{qN(x)}{\varepsilon_\text{o} E_\text{ext}} $$

where $N(x)$ are the empty traps’ density and $E_\text{ext}$ is the external electric field we can rewrite Eq. (1) as

$$ J \sim \frac{E}{C_24} \frac{e}{C_0} \frac{q}{q} \frac{\phi_B}{\phi_B} \frac{K_T}{C_0/C_1} \sqrt{1} \left( E_\text{ext} \frac{qN(x)}{\varepsilon_\text{o} E_\text{ext}} \right) $$

Fig. 3. I-V characteristic of CC-MOSFET with high IGSS leakage current.

Fig. 4. I-V characteristics on a virgin DUT device in charge separation mode.

Fig. 5. IGSS inter-poly oxide characteristics after different pulse heights of same width 10 ms. The first characteristic is the fresh curve without any pulse, from second curve to tenth the pulse height, $V_g$, increase of 1 V, on the latest two curves the pulse steps have been of 2 V (10 ms).

Fig. 6. Leakage current dependence by the temperature.
After pulse we have trapped \( n_t \) electric charge so that the current density will be:

\[
\frac{J_{\text{pulse}}}{E} e^\frac{-x}{\alpha} = e \left( \frac{x}{\alpha} \right) \sqrt{\left( \frac{q}{\pi \epsilon_0 \varepsilon_{\text{ox}}} \right) \left( 1 + \frac{qN(x)x^2}{4\epsilon_0 \varepsilon_{\text{ox}} E_{\text{ext}}} \right)}
\]  

(3)

where \( \langle N(x) - n_t \rangle \) is the net empty traps.

If

\[
E_{\text{ext}} \gg \frac{qN(x)x^2}{\epsilon_0 \varepsilon_{\text{ox}}}
\]

The above relations could be written:

\[
\sqrt{\left( \frac{q}{\pi \epsilon_0 \varepsilon_{\text{ox}}} \left( E_{\text{ext}} + \frac{qN(x)x^2}{\epsilon_0 \varepsilon_{\text{ox}}} \right) \right)} \approx \sqrt{\left( \frac{qE_{\text{ext}}}{\pi \epsilon_0 \varepsilon_{\text{ox}}} \right) \left( 1 + \frac{qN(x)x^2}{2\epsilon_0 \varepsilon_{\text{ox}} E_{\text{ext}}} \right)}
\]

The same about \( J_{\text{pulse}} \).

With this approximation in mind from Eqs. (2) and (3) we have

\[
\left( \frac{kT}{q} \right) \ln \left( \frac{J_{\text{pulse}}}{J_{\text{off}}} \right) \sim \frac{qn_t x^*}{V_{\text{gate}}} = \beta \frac{Q_{\text{off}}}{V_{\text{gate}}}
\]  

(4)

where \( \beta \left[ V^{-1/2} \text{ cm}^2 \text{ C}^{-1} \right] \) is given

\[
\beta = \frac{q}{kT} \left[ \frac{E_{\text{ox}}}{4\pi \varepsilon_0 \varepsilon_{\text{ox}}} \right]^{1/2}
\]

In other words by the above I–V characteristics we are able to know the charge density trapped, \( Q_{\text{off}} \), during every pulse. Fig. 7 shows the result.

We evaluate the trapped charge estimating the area subtended from \( \ln(1/J_{\text{pulse}}) \) curves as shown in Fig. 7 and then we have a valuation of the charge trapped applying relation (4). Fig. 8 shows the result.

The values in Fig. 8 have been fitted with a Gaussian curve. With this method, we have an evaluation and a control of the trapped charge into the polyoxide during every pulse. These values are consistent with the values that are commonly derived in other techniques [5,10].

4. Conclusions

By charge separation method we have analyzed all the electrical contributions to the total gate leakage current through a CC-MOSFET device during IGSS electrical configuration and we have observed that the main contribute to total leakage current is due to the polyoxide leakage current. We have found that the gate leakage current is reduced after consecutive pulses and its characteristic is partially recovered by thermal treatment. We have modeled this behavior due to a modification of the barrier height caused from the trapped charge. Supposing that we use a Frenkel–Poole transport mechanism, we were able to fit the model which links the gate pulses and the amount of trapped charge density. Quantifying the amount of trapped charges in the polyoxide allows us to measure the insulation quality of the oxide layer grown on n + polysilicon.

References


Fig. 7. Charge density trapped after every \( V_g \) pulse.

Fig. 8. Charge trapped after every rectangular pulse.