

Capability of SiC MOSFETs under Short-Circuit tests and development of a Thermal Model by Finite Element Analysis

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Abstract. The aim of this paper is to analyze the SiC MOSFETs behavior under short circuit tests (SCT). In particular, the activity is focused on a deep evaluation of short circuit dynamic by dedicated laboratory measurements conducted at different conditions supported and compared by means of a robust physical model developed by Finite Element Approach.

Introduction

Currently, SiC power devices are demonstrating superior performances compared to Si ones, thanks to their better electrical and thermal properties. Consequently, SiC MOSFETs are substituting standard Si devices in applications where high switching frequency and reduced energy losses are required. This technological evolution in field of semiconductor has to cope reliability requirements since standards need to be satisfied in exacting fields, such as: automotive, aircraft, industry and renewable energy. For example, typical power converters and their relative power electronics components have to: respect precise safety rules, operate in harsh conditions and be robust to critical events, among them the most critical is the short circuit [1].

Since few special equipment are able to thermally monitor power pulses of microseconds [2], therefore the temperature rising inside the structure and in the neighboring layers can be estimated, for very fast pulses, mainly by simulations. Moreover, the temperature estimation and its correlation with known critical values would allow to explain failure modes observed experimentally.

In this context, simulation tools and methodology are playing an important role since the understanding of the phenomenology occurring inside the structure under extreme test conditions, can address to an intrinsic strengthening of the technology itself saving development times [3], [4].

In this paper, we provide a general description of experimental Short Circuit tests performed on 650V, 45mΩ SiC Power MOSFET samples, together with relevant failure analysis and modeling strategy.

Short Circuit Test Analysis and Simulation

At the beginning, before Short Circuit test (SCT), the samples gate oxide integrity has been performed at the Curve Tracer, Fig. 1(a). After this verification, the DUT has been dynamically characterized, evaluating its switching properties. Fig. 1(b) shows the equivalent circuit for typical switching characterization and Fig. 1(c) the relevant experimental waveforms: V_{gs} , V_{ds} , I_d and power profile P_{off} during device turn off at $V_{DD}=400V$, 20A load current, $V_{gs}=-5/20V$ with $R_g=4.7\Omega$. Turn off switching energy, E_{off} , has been also calculated, obtaining about 25μJ.

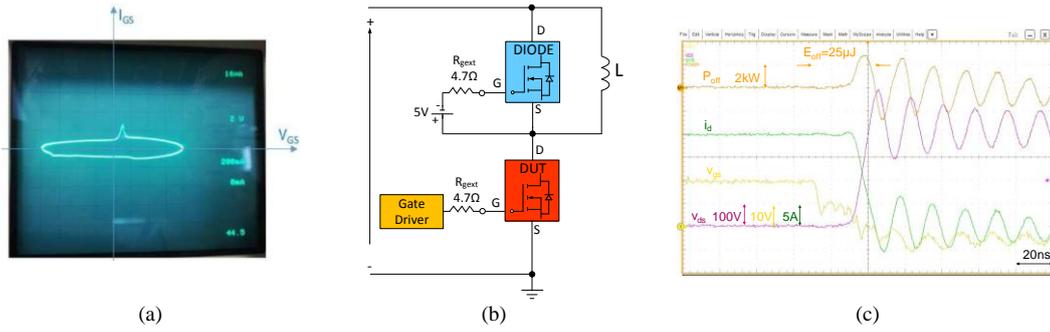


Fig. 1 (a) Gate oxide measurement, (b) Equivalent circuit for switching characterization and (c) typical turn off waveforms

The test bench used for experimental SCT is shown in Fig. 2(a) and its relative equivalent circuit is reported in Fig. 2(b).

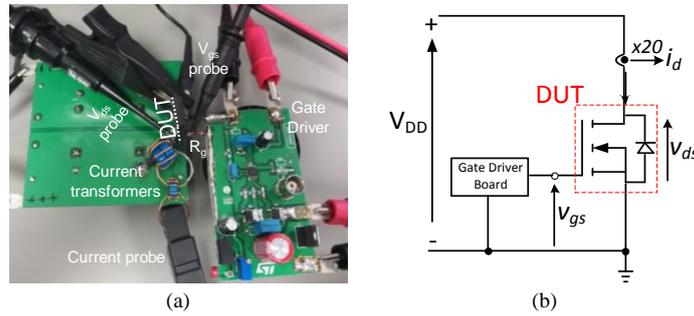


Fig. 2 Experimental set up: (a) test bench, (b) equivalent circuit

In Fig. 3(a) the short circuit experimental waveforms are shown at failure condition for sample 1. The failure point is achieved by a sequence of single pulses with a time width increment of 250ns. From one pulse to another a delay time of 5s has been observed. The device performs properly the short circuit test with the pulse of $t_{sc}=5.75\mu s$ at conditions of $V_{DD}=400V$, $V_{gs}=0/20V$ and $R_g=4.7\Omega$.

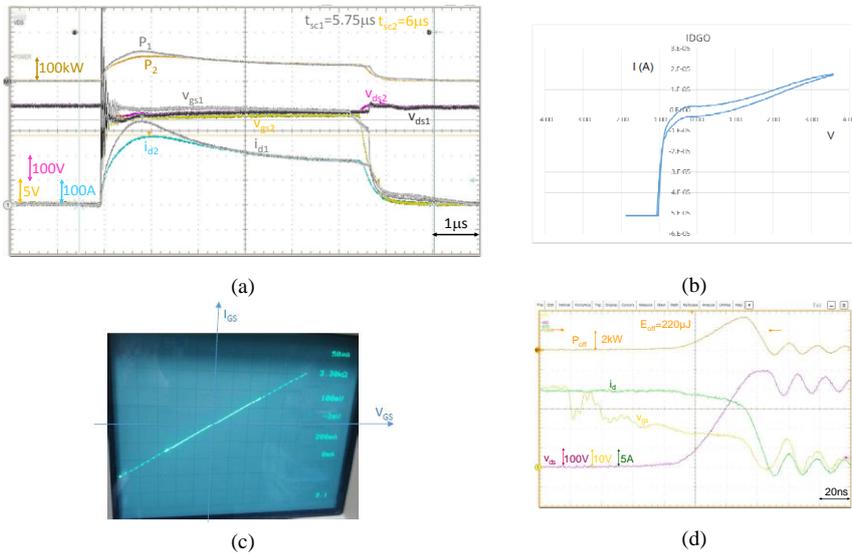


Fig. 3 (a) Dynamic waveforms of experimental short circuit tests, (b) and (c) gate oxide electrical characterization (d) Turn off switching after gate oxide degradation due to short circuit tests.

At this time pulse is not possible to highlight the failure, which will be verified at the next time step ($t_{sc}=6\mu s$) where the gate oxide is irreversibly damaged. A drain current I_d and V_{gs} reduction is observed Fig. 3(a). In Fig. 3(b) the observed damage, due to high Short Circuit Energy (E_{sc}) is the gate oxide failure and it is also confirmed with curve tracer test of Fig. 3(c). The observed gate oxide degradation implies slight variation of dynamic performance in terms of E_{off} for sample 1 and remarkable change for sample 2 as shown in Fig. 3(d).

Subsequently, the failed device has been handled to perform failure analysis highlighting defect localization by photo emission from back and front side and performing cross section analysis on “hot spot” by Focused Ion Beam technique. The physical defect shown in Fig. 4 consists in polysilicon layer melting which is coherent with the electrical scrap.

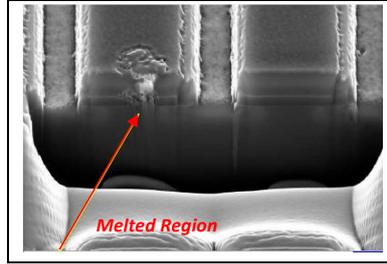


Fig. 4 Physical analysis after degradation.

In Table I experimental results are summarized for two samples among the tested devices. From measurements it appears that different levels of damage have been generated. Sample 1 shows an intrinsic gate-source resistance of 3.3k Ω , which anyway does not affect the MOSFET function apart from an abnormal continuous gate current absorption. On sample 2 the intrinsic gate-source resistance is much lower and the amount of absorbed gate current increases with respect to standard operative conditions. Both samples still maintain their functionalities, even if in the most damaged one the switching energy has dramatically increased, as can be appreciated from Fig. 3(d)

Table 1 Short circuit final results and sample characteristics.

DUT	V _{th} [V] @ 1mA		RDSON [m Ω] @ V _{GS} =20V I _D =20A		Gate oxide Integrity		E _{OFF} [μ J] @ V _{DS} =400V, V _{GS} =-5/20V R _G =4.7 Ω , I _D =20A		t _{sc} [μ s]
	Before	After	Before	After	Before	After	Before	After	
1	2.74	2.4	46.4	46.5	Good	Fail. R _{GS} =3.3k Ω	25	28	6
2	2.57	0	44	/	Good	Fail. R _{GS} =18 Ω	26	220	5.75

Consequently, to explain the failure mechanism, structural simulations, Fig. 5(a), in SC static conditions have been performed by Silvaco tools and voltage/current density profiles inside the SiC structure have been extracted as shown in Fig. 5(b). In Atlas (Silvaco tool for device simulation) the FE device has been biased up to 20V in the gate and 400 V on drain contact. The conduction model has been fine-tuned by using experimental data set in order to have a good fit either threshold voltage or I-V characteristics also in saturation conditions. Key parameters to gain a good match between experimental data and simulation output are the density of state energy profile localized at gate oxide Silicon Carbide interface, the anisotropic mobility values and the electron saturation velocity. Conduction model fine tuning is really important in the proposed modeling strategy since it permits to provide an accurate distribution of the dissipated power along the die during SCT.

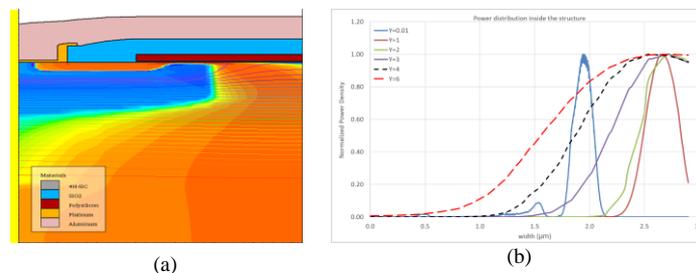


Fig. 5 Silvaco tools: (a) Simulated Vertical Section and (b) Power profile distribution.

The proposed methodology consists in providing to the physical model, developed using a Finite Element Method, the experimental time-dependent power profile according to the distribution coming from structural simulation performed with Silvaco tool. The model has been specially developed to study such events, as short circuit, which last very few microseconds, to understand and to explain what happens inside the SiC MOSFET structure during short power pulses

considering also the Silicon Carbide thermal properties (thermal conductivity and heat capacity) as function of temperature. Using this new model, the thermal behavior inside the structure has been studied and the temperatures in the junction and surrounding layers have been evaluated. In Fig. 6(a) the thermal map and Fig. 6(b) heat flux are reported at instant when the temperature peak is reached, highlighting where the maximum temperature is located (Fig. 6(a)) and how the heat is propagating across the structure (Fig. 6(b)). The thermal distribution allows to detect which part of the device is mainly involved in the SCT explaining the failure mode experimentally observed. The Fig. 6(c) shows the temperature profile vs time for different layers: the peak temperature values, referred to the top layers of the structure, are aligned with currently known critical values [6].

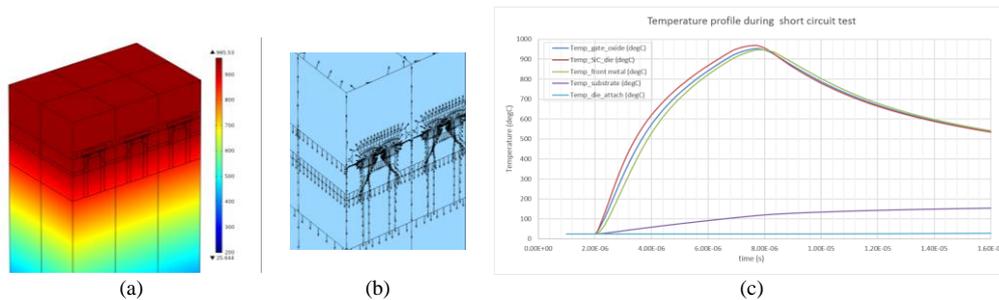


Fig. 6 (a) 3D Thermal map, (b) heat flux and (c) temperature profile during short circuit.

Conclusions

In the present work, a Finite Element Model which takes into account the physical structure of MOSFET and the experimental test data, has been created. This technique is able to estimate the temperature distribution in the junction and surrounding layers for fast power pulses and especially for Short Circuit Test conditions explaining the observed failure. The proposed approach cannot predict current filamentation in the device as no electro-thermal interaction is taken into account [5].

The achieved result, in terms of modeling strategy implementation, is very important, since few equipment can accurately detect the temperature for so brief time pulses and all the typical models developed for full devices in package or systems cannot be efficiently used for this kind of event.

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