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4H-SiC Defects Evolution by Thermal Processes

N. Piluso[1,a *], M.A. Di Stefano[1,b], S. Lorenti[1,c] and F. La Via[2,d]

[1]STMicroelectronics, Stradale Primosole, 50, 95100 Catania, Italy

[2]IMM-CNR, VIII Strada, 5, 95121 Catania, Italy

[a]nicolo.piluso@st.com, [b]maria.distefano@st.com, [c]simona.lorenti@st.com, [d]francesco.lavia@imm.cnr.it

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Abstract. 4H-SiC defects evolution after thermal processes has been evaluated. Different annealing temperatures have been used to decrease the defect density of epitaxial layer (as stacking faults) and recover the damage occurred after ion implantation. The propagation of defects has been detected by Photoluminescence tool and monitored during the thermal processes. The results show that implants do not affect the surface roughness and how a preliminary annealing process, before ion implantation step, can be useful in order to reduce the SFs density. It shown the effect of tuned thermal process. A kind of defect, generated by implant and subsequent annealing, can be removed by an appropriate thermal budget, while others can increase. A fine tuning of thermal process parameters, temperature and timing, is useful to recover the crystallographic quality of the epilayer and increase the yield of the power device.

Introduction

During last two decades, Silicon Carbide has attracted wide interest being an excellent material for high-power, high-temperature, and high frequency devices. The optimization of bulk and epitaxial growth process in 4H-SiC are successfully reducing crystallographic (Dislocations and stacking faults) and surface defects (as Triangles, Carrots, Comets, Pits). However, many of these defects are highly damaging for power devices, increasing the leakage current and altering the I-V relation, reducing the reliability of the devices [1,2,3,4]. In addition to the crystallographic quality of the starting substrate and the optimization of the epitaxial growth should be taken into account the thermal processes that induce the propagation of defects or their removing.

A strong effort has been done in order to study and manage the evolution of crystallographic defects (stacking faults propagation) propagated by epitaxial growth and agglomeration of defects coming from the damage occurred by ion implantation. Crystallographic defect as Stacking faults (SFs) have been widely studied in literature [5]. Previous authors [6] have shown the effects of annealing processes on several kind of SFs. SFs are detrimental for the proper functioning of the device, e.g. the degradation of SiC bipolar devices is caused by the formation of single Shockley faults in the drift layer during current conduction [7, 8].

Another source of defects, involving the epitaxial layers, is the ion implantation process [9,10,11]. The advantage of ion implantation is the wide range of doping concentration (n- and p-type) that can be obtained. The drawback is the damage occurred into the epilayer that can lead to a partially amorphous shallow region (more than 200nm). In order to recover the lattice damage thermal process are needed. A fine tuning of thermal process parameters, temperature and timing, is mandatory to recover the crystallographic damage and increase the yield of the power device.

Being the thermal process required for any SiC power device the overall effect on epilayer should be studied.

Experimental setup

The epitaxial layers studied have been grown on low-pressure, hot-wall Chemical Vapor Deposition reactor by Tokyo Electron Limited (TEL) with the rotating susceptor. The homo-epitaxial growth was carried out using the Silane/Propane system for Si and C supply, respectively. A high purity

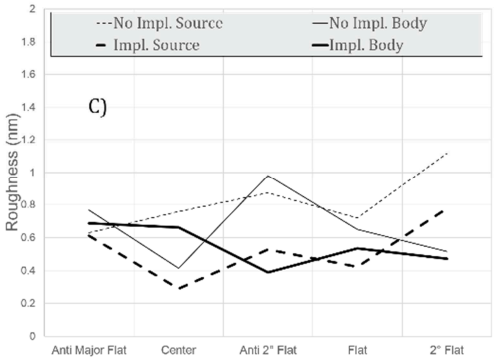

Fig. 1 Distribution of the roughness along the samples implanted and not implanted

industrial grade H_2 was used as a carrier gas as well as reducing agent for the growth of epitaxial layers. 10% N_2 gas was added as a dopant. The n-doped epitaxial layers (10^{16} at/cm^3) were grown on the Si-face (0001) 4H-SiC, n-type (~ 10^{18} at/cm^3) substrates with 4° off axis.

The epitaxies were implanted with typical doses used for MOSFET application (10^{13} - 10^{14} cm^2 for source region and 10^{12} - 10^{13} cm^2 for body region with implantation energy of several keV). Before the implantation the post-annealing oxidation process, performed at 1150°C in N_2O, has been made in order to determine the epitaxial defects evolution during the gate oxide formation. After the implantation the thermal process has been studied by performing the annealing with temperature ranging from 1650°C to 1750° for 30 minutes.

The samples have been characterized by Atomic Force Microscopy (AFM) for the inspection of the surface roughness, by KLA-Tencor Candela (CS920) for the study of defect density (in particular stacking faults) and photoluminescence tool for the study of the post-annealing defects propagation. Laser sources used in PL characterization were HeCd (325nm) and Nd:YAG (266nm) with a spot diameters ranging from 6 to 10 μm.

Results and Discussion

One of the main value that must be kept under control is the roughness of the surface after the annealing process. The evaluation of surface roughness of the samples, before and after implantation and the annealing, is shown in Fig. 1. The sample does not show relevant variation of surface roughness that lead to conclude that the implantation process does not degrade the surface of the epilayer.

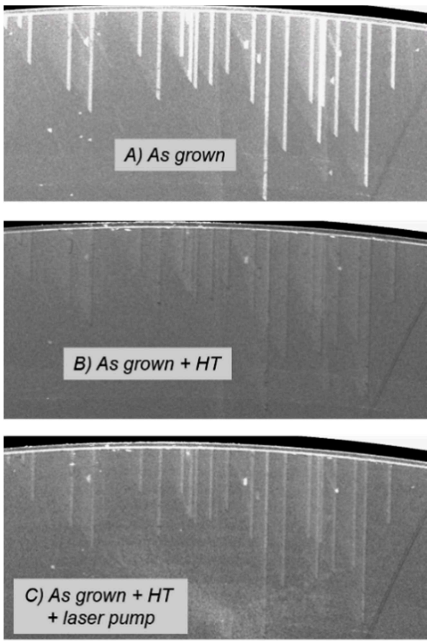

Fig. 2 A) PL signal from wafer as grown. **B)** PL signal from wafer after HT process. **C)** PL signal from wafer after laser pump

The result obtained is mainly due to the optimization of the Carbon cap layer used to protect the surface during the thermal process. Fig. 1 shows the distribution of the surface roughness on the samples pre and post implantation and annealing. The mean values were ranging from 0.3 to 1.2 nm.

The annealing processes used to study SFs evolution are: 1) annealing at 1650°C (**HT**) in Argon for 30 min; 2) post-oxidation-annealing (**POA**) that consist in an annealing at 1150°C in N_2O for 4h. Fig. 2A shows a huge density of Bar Stacking Faults (BSSFs) [12] located at the top of the as grown wafer. After the **HT** process the most of BSSFs seem disappear; the PL signal decreases suggesting a crystallographic rearrangement (Fig. 2B). The wafer has been subsequently exposed with to a high power laser (Nd:YAG with laser source of 266nm and power density of 70 W/cm^2) in order to evaluate the reappearance of stacking faults or their permanent closure [6]. The Fig. 2C clearly shows the reappearance of several SFs located at the same spatial position and, in general, a slight increase of PL signal of the BSSFs. Fig. 3 shows the evolution of a defect after **POA** process. The appearance of a defect (Fig.3B) on the surface is ascribed to the annealing process. A careful inspection of the defect generated induces to think to a threading screw dislocation (TSD) propagated along the epitaxial layer and, further the annealing process, up to the surface. As it is well known, the TSD, which originate from the substrate, can be converted in

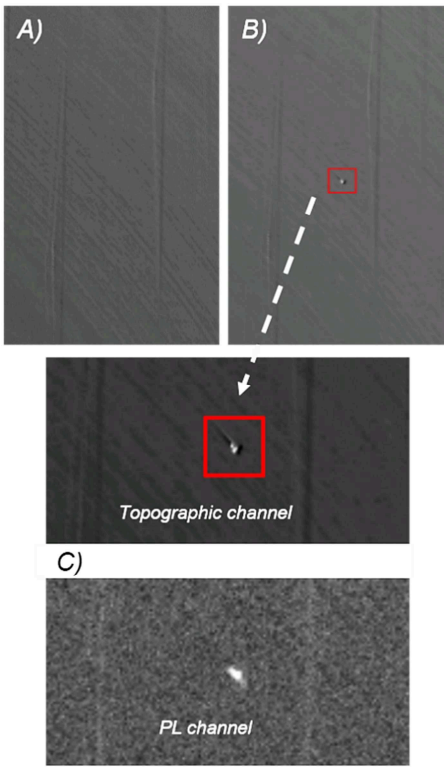

Fig. 3 A) Wafer as grown. **B)** Wafer after POA process. **C)** Detail of defect from topographic and PL channel after POA process

surface defect as Frank Stacking faults (or Carrot) [13,14], that probably is what has been detected after the **POA** process (Fig. 3C). The occurrence of this kind of defect is typically below 2% of the total amount of defects revealed before the process.

The effect of the implants [15] and annealing process [16] is a crucial point for the defects propagation on epilayer. In MOSFET devices defects introduced by the implantation process can strongly affect the electrical characteristics and the reliability of these devices. The effect of the annealing temperature has been evaluated by ranging the post-implantation annealing temperature from 1650°C to 1750°C. Fig. 4 shows the results obtained for two different implants: body (p-type) and source (n-type). The PL signal related to defects created at 2.6 eV is detected for both implants. Additional peak for body implants is revealed at 1.7eV (Fig. 4A).

The PL spectra coming from samples implanted with source dose show how the annealing process determines an increase of the PL peak revealed at high energy, suggesting a propagation of this defect with the increasing of temperature. All samples underwent a dry oxidation process (10 hours in Argon) after the implantation and before the annealing process in order to remove point defects. A reference sample, without oxidation step, is plotted. The sample without oxidation step shows a lower intensity of the 2.6eV peak than the other samples, however, it shows the lowest intensity of the gap signal, suggesting a low level of recrystallization after annealing process. A similar behavior is observed for the defect peak at 2.6eV for the body implanted samples, suggesting the propagation and the consolidation of this defect with the increasing of temperature. Conversely, the defect located at 1.7eV shows a decreasing intensity with the temperature. The sample without oxidation step shows the highest intensity of the defect peak located at 1.7eV. The sample annealed at 1750 °C shows a high value of the band-gap signal and does not show the defect peak at 1.7 eV that seems to be totally removed from epilayer. The defects generated by ion implantation seems to be related to point defects $EH_{6/7}$ (revealed at 1.7eV) and $Z_{1/2}$ (revealed at 2.6 eV). This reinforces the belief that the implantation makes amorphous a thin layer of the epitaxy (up to 200 nm); the subsequent annealing recovers the crystal lattice and generate point defects that tend to agglomerate. By increasing the temperature the defect $EH_{6/7}$ is disappearing, while defect $Z_{1/2}$ is propagating. As suggested by Danno et. al. [17], $Z_{1/2}$ and $EH_{6/7}$ centers may be related to different charge states of the same defect (probably carbon vacancy).

Conclusions

4H-SiC defects evolution after thermal processes have been evaluated. Different annealing temperatures have been used to decrease the defect density of epitaxial layer (SFs) and recover the damage that occurred after ion implantation. SFs density can be decreased with a typical thermal process performed at 1650°C in Argon for 30 minutes, before ion implantation. The oxidation process, before the annealing process, seems to be inefficacy to remove the defects generated by implantation. Such a step should be performed after the annealing process, not before. PL signal of the defect located at 2.6eV increases with the annealing temperature. The overall remove of the PL signal related to the defect located 1.7eV, as a results of the thermal process, is shown. The disappearing of the defect at 1.7 eV and the simultaneous rise of the 2,6 eV defect suggests a variation of the charge status of the defect and not its removal [17]. Currently, two studies are in

progress to prospect and optimize the annealing processes: 1) variation of the temperature and the time of the **HT** annealing in order to verify if the closure of defects (SFs) can be permanent; 2) Define a multi-step post implantation annealing process (with several temperatures) in order to study the evolution of the defect observed at high energy (2.6eV).

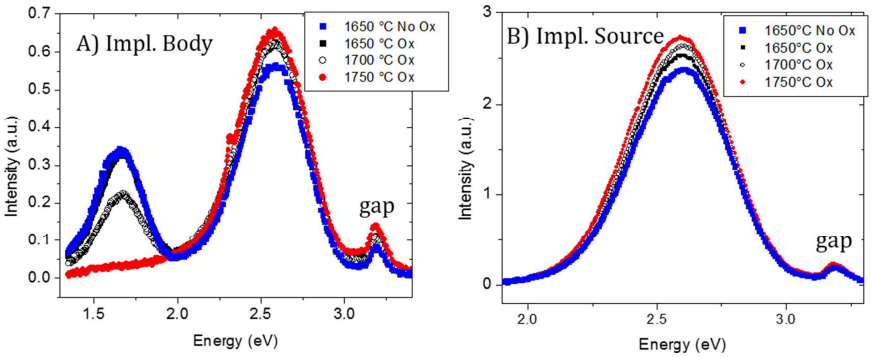

Fig. 4 A) PL signal from body implanted zone for three annealing temperature.
B) PL signal from source implanted zone for three annealing temperature

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