TO-LL and MDmesh M6 the latest breakthrough in high-level telecom SMPS

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Abstract

This paper presents the ST's new SMD package TO-LL (TO-lead less) and its benefits in terms of thermal management, PCB area, switching performance and parasitic inductance on the leads. Thanks to this innovative SMD package and the latest Super Junction technology from ST, MDmesh M6 for PFC and MDmesh DM6 for LLC, it is possible to increase the overall power efficiency, reduce total weight and dimension and increase the power density. The evaluation begins with an overview of SMD packages and concludes with an application analysis on 1.5kW SMPS, evaluating both PFC and LLC stages. Moreover, a thermal analysis between a solution with through-hole packages and one with SMD packages was performed, to show the advantages deriving from the adoption of surface mount device.

1 Introduction

Nowadays, the demand for more efficient and compact switch-mode-power-supplies (SMPS) for telecom and server applications is increasing. The combined trends of continuous reduction in the volume and size of power converters and the increase in the required output power represent challenging issues in modern SMPS designs. When addressing the high-power density requirement, even in an SMPS with high peak efficiency, a typical problem is the heat generated in the limited available volume, especially at full load. For this reason, SMD packages are substituting the classic through-hole packages in order to reduce occupied space on PCB, but the high-power demands of typical telecom SMPS (1.5 kW for half bridge or 3 kW for full bridge) and the need for appropriate thermal dissipation calls for new and improved SMD packages, such as the TO-LL.

2 Overview of the SMD package for power MOSFETs

This overview covers the most common SMD packages for Silicon power MOSFETs: PowerFLAT™ 8x8, PowerFLAT™ 5x5, D^2PAK, DPAK and TO-LL. Table 1 shows the occupied PCB area and $R_{thj\text{-}pcb}$.

From Table 1, it is clear that the TO-LL offers the best trade-off between heat management, occupied space on PCB and current capability.

Package	Area (mm^2)	Package height (mm)	$R_{thj\text{-}pcb}$ (°C/W)
TO-LL	115.6	2.30	46
PowerFLAT 8x8	64	0.85	50
PowerFLAT 5x5	25	0.80	58.5
D^2PAK	164.3	4.6	35
DPAK	66.6	2.4	50

Table 1 Packages occupied area on PCB and $R_{thj\text{-}pcb}$

In fact, the TO-LL can have the same die size as the D^2PAK, but with 30% less PCB space, and compared with the PowerFLAT™ 8x8, the TO-LL package has better thermal capability due to its lower $R_{thj\text{-}pcb}$ (assuming that the dissipation area is the same, as stated in the datasheet) [1].

The $R_{thj\text{-}pcb}$ values shown in Table 1 refer to when the device is mounted on a FR-4 board of 1 $inch^2$ with a 2 oz copper (datasheet conditions).

From above mentioned packages only the TO-LL has the kelvin pin, not all devices assembled in PowerFLAT 8x8 have the kelvin connection. The kelvin pin is used as the reference ground for the driver in order to optimize the behavior during switch-on and switch-off.

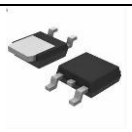

Figure 1 DPAK

Figure 2 D²PAK

Figure 3 PowerFLAT 8x8

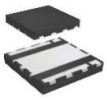

Figure 4 PowerFLAT 5x5

Figure 5 TO-LL

Another key characteristic is the creepage between the drain and source pads. The creepage is defined as the shortest path between two conductive materials measured along the surface of an isolator which is in between. Maintaining a certain creepage distance addresses the risk of tracking failures over lifetime. The generation of a conductive path along the isolator surface due to the high voltage applied over long time is more related to the RMS value and depends also on environmental condition.
The creepage distance relies on:

- Operative voltage
- Allowable overvoltage
- Pollution of the environments
- Isolation

Table 2 reports the creepage value for the packages under investigation.

Package	Creepage (mm)
TO-LL	2.7
PowerFLAT 8x8	2.75
PowerFLAT 5x5	0.71
D²PAK	3.65
DPAK	1.8

Table 2 Creepage distance for the package under analysis

3 TO-LL features and benefits

The main features of this package are:

- Reduced space on PCB vs D²PAK with same die area inside
- Kelvin source pin added
- Increase thermic management
- Reduced thickness, 2.3 mm
- High creepage, 2.7 mm

And the main benefits:

- Increase power density
- Improving of turn-on and turn-off energy
- Compact SMPS for telecom
- MOSFET BVdss from 600 up to 850 V

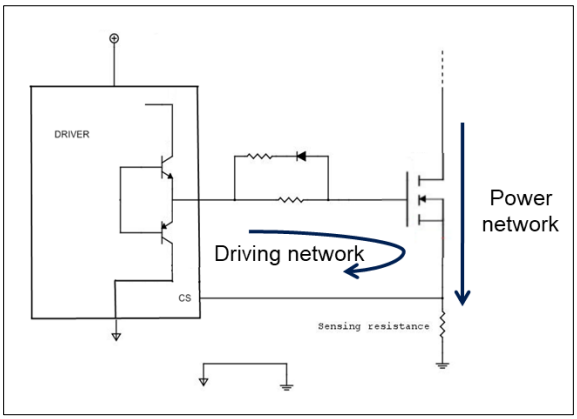

Figure 6 Typical driving with a 3 pin MOSFET

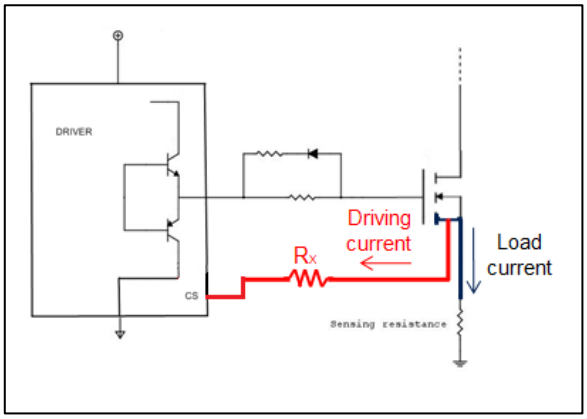

Figure 7 Driving with the addition of the kelvin pin

4 MDmesh™ M6 and DM6 benefits in SMPS

The latest ST super-junction technologies are the MDmesh M6 and MDmesh DM6 with fast recovery diode [7]. The M6 is ideal for hard switching applications, and it will be evaluated in the PFC section, instead DM6 with its fast diode is ideal for bridge topologies and it will be evaluated in the LLC section. M6 and DM6 are the right choice to improve efficiency and robustness in high-level converters. With an optimized threshold voltage for soft switching,

good switching behavior for hard and soft switching, low gate charge for operation at high frequencies, capacitance profiles and threshold voltage optimized for high efficiency even at light load conditions, the MDmesh M6 and DM6 series improve converter efficiency.
Moreover, the DM6 thanks to its improved intrinsic diode reverse recovery time (t_{rr}) and Q_{rr} and higher dV/dt capability, it improves the reliability and robustness of the entire system even in non-standard working conditions.

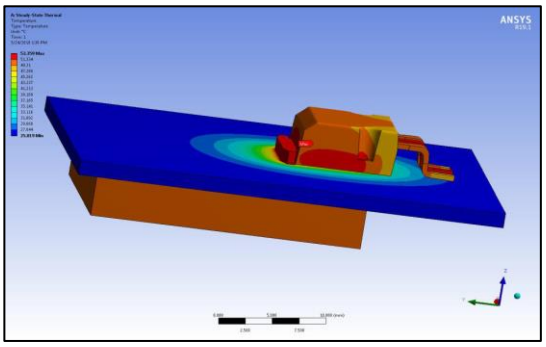

Figure 8 D²PAK and thermal vias

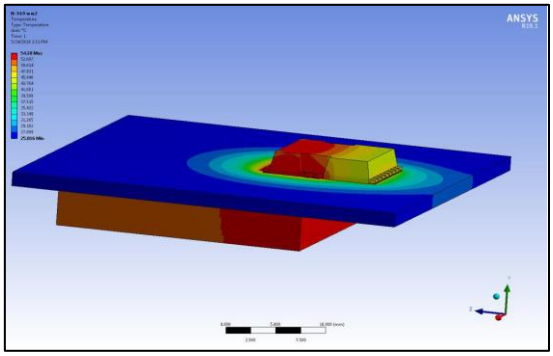

Figure 9 TO-LL and thermal vias

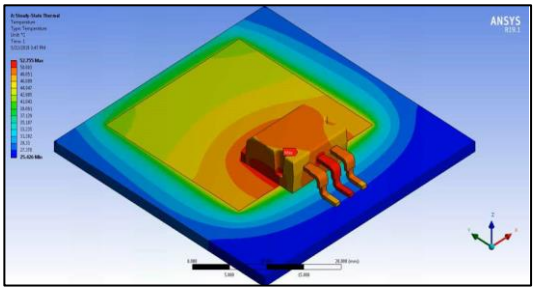

Figure 10 D²PAK and copper layer dissipation

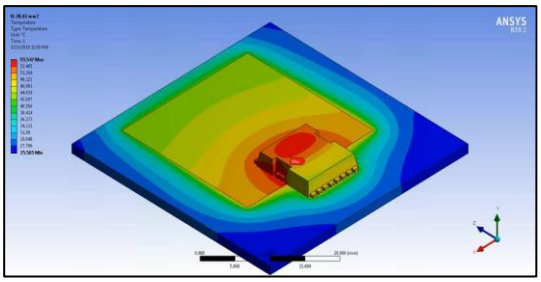

Figure 11 TO-LL and copper layer dissipation

5 Thermal analysis

Before mounting the TO-LL in the final application, a thermal simulation was performed with ANSYS, in order to understand the most powerful layout condition to dissipate and manage the heat linked with the power losses, as shown in Figures 8 to 11. The heat sink used in the first two conditions (fig 8 and 9) has this dimension: 25.4 x 25.4 x 5 mm, indeed in the other two cases (Fig. 10 and 11) the copper area is 25.4 x 25.4 mm with a thickness of 70µm made by copper.
Inside the two packages, TO-LL and D²PAK, the same die is mounted. Table 3 reassumes the $R_{thj\text{-}pcb}$ with this solution, moreover, an additional forced air flow or a water-cooling system are evaluated in order to better manage the heat dissipation [2].

D²PAK		TO-LL	
Thermal vias			
Rthj-pcb (°C/W)	28.36	Rthj-pcb (°C/W)	29.18
Thermal vias + water cooling			
Rthj-pcb (°C/W)	2.23	Rthj-pcb (°C/W)	2.06
Copper layer dissipation			
Rthj-pcb (°C/W)	27.76	Rthj-pcb (°C/W)	30.55

Table 3 Values of $R_{thj\text{-}pcb}$ in different configuration, results of the ANSYS simulations

According to these results, the PCB where the SMD packages are mounted use a combination of the copper layer and thermal vias.

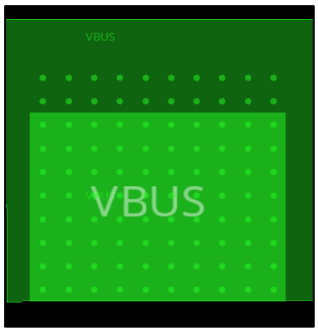

Figure 12 Copper layer and vias configuration for the board used in the test

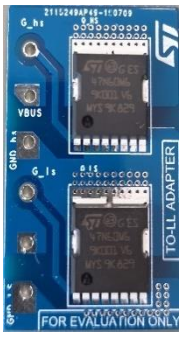

Figure 13 Daughter board with the TO-LL mounted

A double copper layer, one on the TOP side of the PCB and other one on the BOTTOM side, connected with a matrix made by 8x10 vias, with a diameter of 0.3 mm as shown in Figure 12.
The total copper area is 12x12 mm for both TOP and BOTTOM side. The copper thickness is chosen to 2 oz.

Adopting this solution, all the SMD packages under test, TO-LL, D^{2}PAK and PowerFLAT 8x8 are characterized, in order to obtain the $R_{thj\text{-}amb}$ with these specific layout conditions, using the daughter board shown in Figure 13.
To characterize the thermal resistance, a fixed power supply in the range from 0.3 to 2 W feeds the device, soldered on the board, the ambient temperature is 25°C, and by using Equations 1 and 2, the $R_{thj\text{-}amb}$ is obtained, as show in Equation 3 [3].

$$T_J = T_{amb} + P_{tot} \cdot R_{thj-amb} \qquad \text{Eq. (1)}$$

$$T_C = T_J - P_{tot} \cdot R_{thj-c} \qquad \text{Eq. (2)}$$

$$R_{thj-amb} = \frac{T_C - T_{amb}}{P_{tot}} + R_{thj-c} \qquad \text{Eq. (3)}$$

With this layout solution, the resulting $R_{thj\text{-}pcb}$ values are:

Package	Rthj-amb (°C/W)
TO-LL	42
D2PAK	32
PowerFLAT 8x8	45.7

Table 4 $R_{thj\text{-}amb}$ for adopted layout solution, with double copper layer, on TOP and BOTTOM, and thermal vias

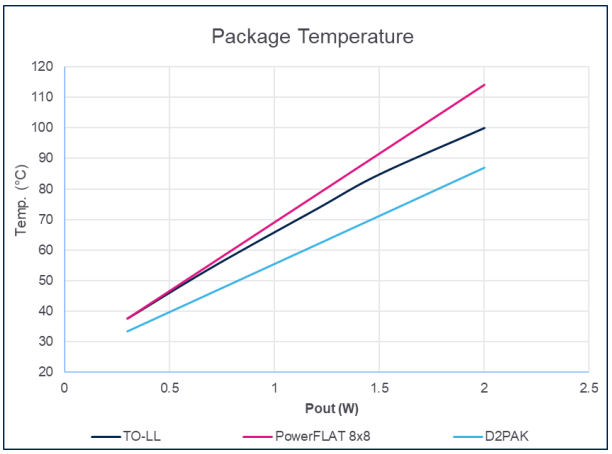

Figure 14 T_{case} during characterization test

The TO-LL packages represent a good tradeoff between PCB space, allowable die dimension and heat management.

6 Application analysis

In this section, a SMPS solution made by a continuous current mode PFC + resonant half bridge LLC, based on a TO-LL package was proposed and analyzed [6]. Moreover, a comparison in terms of power efficiency and case temperature versus a solution based on a TO-247 package was performed.
For both stages the two different packages were evaluated with the same $R_{thj\text{-}amb}$.
For PFC stage the $R_{thj\text{-}amb}$ is about 3.75 °C/W, for the LLC stage the $R_{thj\text{-}amb}$ is about 12.5 °C/W.
The measurement setup is:

- Tektronix AFG 3021, signal generator
- Tektronix DPO 7104C, oscilloscope
- Agilent AC/DC power supply 6813B
- TDK-Lambda GEN600-5.5, power supply
- Chroma 63212A-1200-480, electronic load
- Yokogawa WT310, power meter
- Tektronix TCP0030, current probe
- Tektronix P5205A, differential voltage probe
- Flir E30 Thermocamera

Figure 15 Application test JIG PFC + HB LLC

6.1 PFC stage

In the PFC stage, the major benefits associated with the adoption of the TO-LL is the kelvin pin. In fact, the total switching energy, as shown in Figure 17, is less compared with a TO-247 solution [8].
With a reduction of the switching losses, the device can work without heatsink instead the TO-247 need both fan and heatsink, as showed in figure 16.

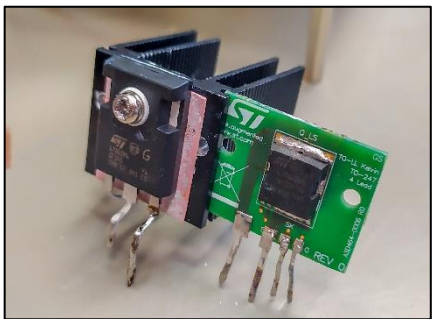

Figure 16 TO-247 with heatsink and TO-LL with daughterboard

The TO-LL device is mounted on a daughter board, figure 16, with the footprint for only one device, with the PCB layout solution regarding the thermal management showed in figure 12.

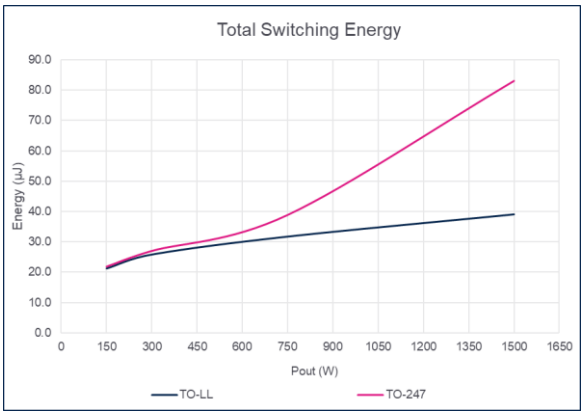

Figure 17 Total switching energy comparison between TO-LL and TO-247

The operative conditions of this stage are:

- V_{IN} 145 V_{AC}
- R_{gon} = R_{goff} = 10 Ω
- f_{SW} 80 kHz
- L_{boost} 500 µH
- SiC diode as boost diode
- V_{OUT} 400V

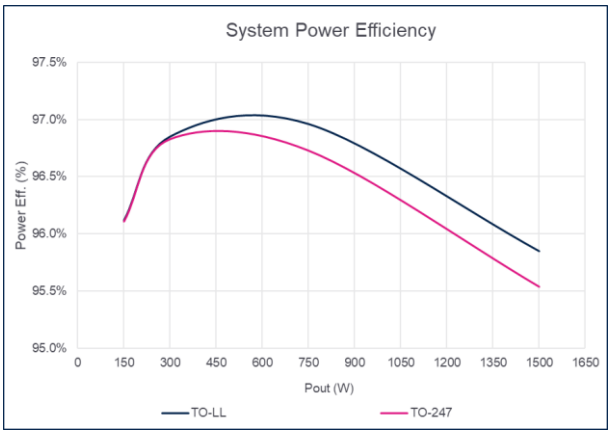

Figure 18 System power efficiency in PFC

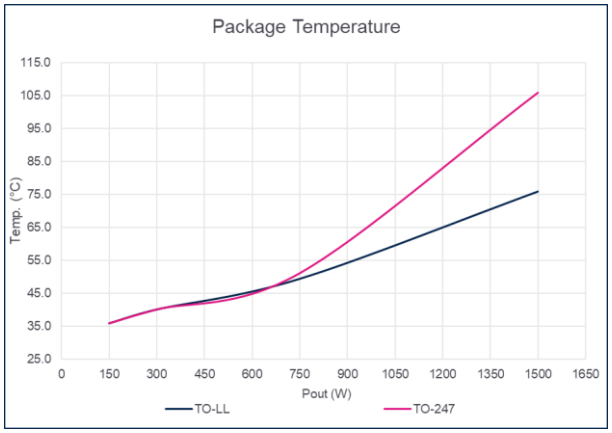

Figure 19 Temperature comparison in PFC

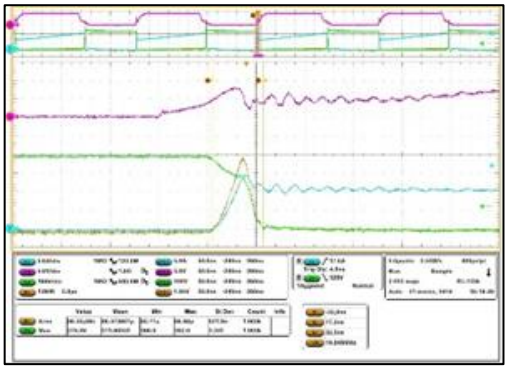

Figure 20 Turn-on waveforms in PFC for TO-247

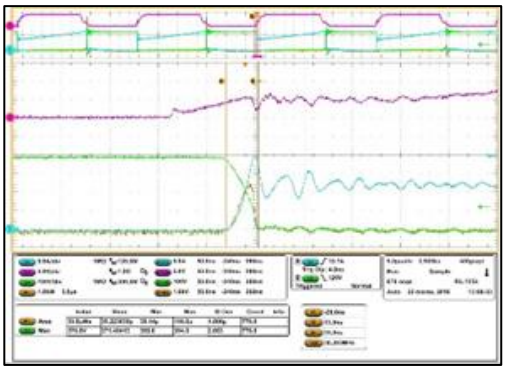

Figure 21 Turn-on waveforms in PFC for TO-LL

The switch-on losses for the TO-LL is about 77% less compared with the TO-2470. The improved switching performance is reflected on the system power efficiency.
In fact, at maximum load, the efficiency of the TO-LL is about 0.13% greater. Figure 20 shows the turn-on waveforms for the TO-247, without the kelvin pin, and in Figure 21 the turn-on for the TO-LL with the kelvin pin. Here, it is possible to see the lower turn-on area and a smaller power peak.

Figure 22 TO-LL temperature for the PFC section at 1.5kW of POUT

Figure 23 TO-247 temperature for the PFC section at 1.5kW of POUT

6.2 HB LLC stage

In this stage, the major benefits derived from the adoption of the TO-LL regards to a possible reduction in size, in the elimination of the heatsink and therefore increase the power density.
Due to the ZVS at turn-on, the switch-on losses are equal to zero; the kelvin pin does not impact the switching performance.
The operative conditions of this stage are:

- V_{IN} 400V
- R_{gon} 22 Ω
- R_{goff} 3.3 Ω
- f_{SW} from 120 to 95 kHz
- L_r 24 µH
- C_r 100nF
- L_m 81 µH
- V_{OUT} 48V

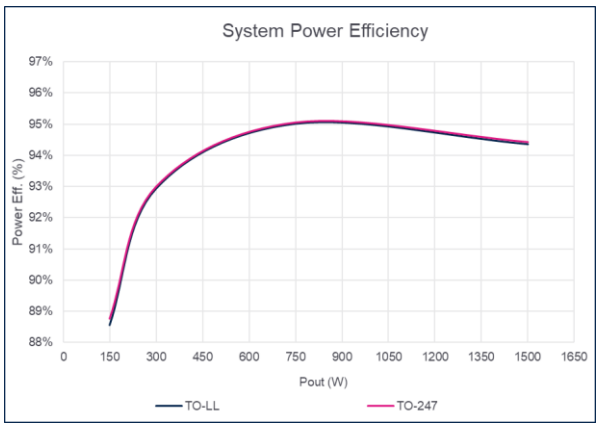

Figure 24 System power efficiency in LLC

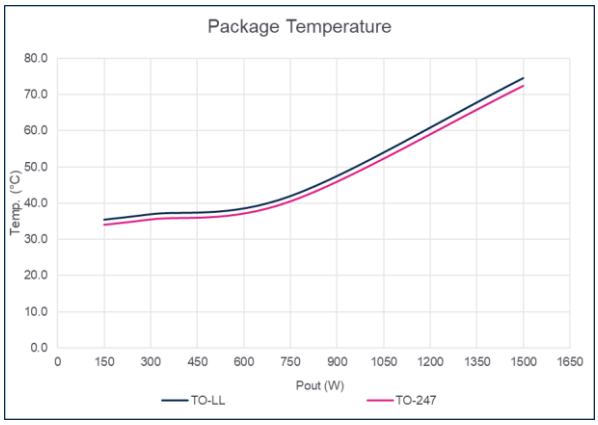

Figure 25 Temperature comparison in LLC

In LLC stage, the system power efficiency essentially is the same; the same device losses are involved.

Figure 26 TO-LL temperature for the HB LLC section at 1.5kW P_{OUT}

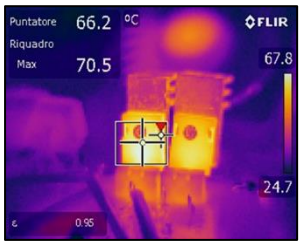

Figure 27 TO-220 temperature for the HB LLC section at 1.5kW P_{OUT}

The case temperature of the TO-LL with the fan at maximum load, is equal to 74.5 °C, for the TO-247 is 70.5 °C.
So, it is possible to consider that the system works in the same electrical and thermal

condition but with a less total weight and dimension due to the elimination of the heatsink. The dimensions of the heatsink are: 45 x 50 x 30 mm as showed in figure 28.

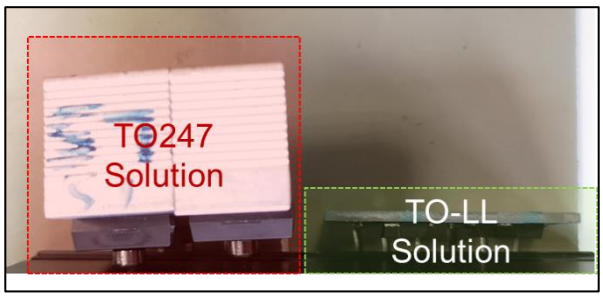

Figure 28 Comparison between TO-247 solution with heatsink and TO-LL solution with the device mounted on the same daughter board

The total volume is 67.5 cm3 and the weight, considering a specific weight of the aluminum equal to 2.7 g/cm3, is about 182 g.

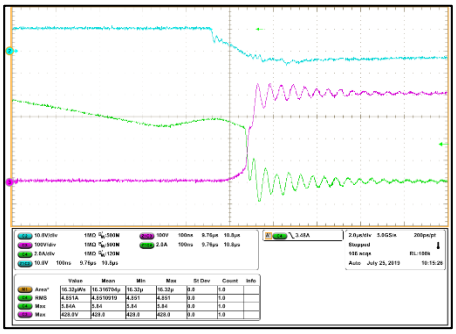

Figure 29 Switch-off waveforms in LLC for TO-247

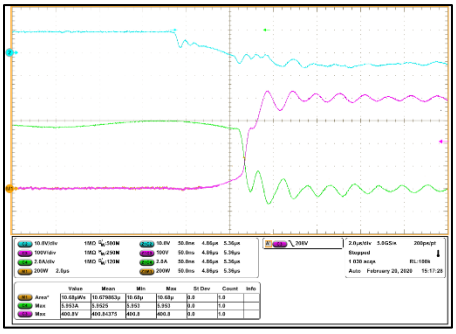

Figure 30 Switch-off waveforms in LLC for TO-LL

From Figures 29 and 30 is possible to see how the shorter distance between the high-side source and low-side drain reduce stray inductance and therefore a smaller overvoltage is present on the drain voltage (purple curves). The overvoltage is reduced by 20V [12].

7 Conclusions

In this paper ST's new TO-LL package has been evaluated in respect to other SMD packages, in order to show its features and benefits, such as the kelvin pin and the optimization between occupied space on the PCB and thermal management.
When approaching a design with an SMD package, it is important to evaluate the thickness of copper layer, vias, etc. and compare possible layouts, according to the power level of the converter, in order to improve the thermal management.
After some preliminary simulations using ANSYS, a daughter board was designed and its resultant $R_{thj\text{-}amb}$ was evaluated.
Afterwards, an application analysis in a 1.5kW SMPS, made by a CCM PFC and a half bridge LLC was performed in order to compare the electrical and thermal performance of the TO-LL packages in respect to a traditional solution based on a through-hole package, this comparison was done with the same $R_{thj\text{-}amb}$ between SMD and through-hole .
In the PFC stage, the kelvin pin helps improve the power efficiency and obtain a lower device temperature due to the smaller switch-on losses.
In the LLC stage, the TO-LL helps reduce the distance between the two MOSFETs of the bridge, so the stray inductance is also reduced.
The temperature of the SMPS at the maximum power out is around 74 °C, starting with an ambient temperature equal to 25°C.

8 References

[1] STMicroelectronics, Thermal behavior and printed circuit board assembly recommendations for STMicroelectronics PowerFLAT 8x8 HV package, AN5436.
[2] STMicroelectronics, Guidelines for using ST's MOSFET SMD packages, AN1703.
[3] STMicroelectronics, Thermal effects and junction temperature evaluation of Power MOSFETs, AN4783.
[4] STMicroelectronics, An introduction to LLC resonant half-bridge converter, AN2644.
[5] STMicroelectronics, Half bridge resonant LLC converters and primary side MOSFET selection, AN4720.

[6] D. Nardo, A. Scuto, G. Sorrentino, A. Raciti and S. A. Rizzo, "The key role of the SJ MOSFET with fast diode in high-end SMPS converters for telecom applications," 2019 AEIT International Annual Conference (AEIT), Florence, Italy, 2019, pp. 1-6.
[7] C. Parisi, M. Melito, F. Fusillo and D. Nardo, "MDmesh™ DM6: The latest Super-junction MOSFET technology with improved fast recovery diode," PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2019, pp. 1-7.
[8] C. G. Stella, M. Laudani, A. Gaito and M. Nania, "Advantage of the use of an added driver source lead in discrete Power MOSFETs," 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, Fort Worth, TX, 2014, pp. 2574-2581.
[9] R. Kibushi, T. Hatakeyama, K. Yuki, N. Unno and M. Ishizuka, "Comparison of thermal properties between Si and SiC power MOSFET using electro-thermal analysis," 2017 International Conference on Electronics Packaging (ICEP), Yamagata, 2017, pp. 188-192.
[10] A. Kempitiya and W. Chou, "Electro-thermal analysis for automotive high power MOSFETs," 2017 33rd Thermal Measurement, Modeling & Management Symposium (SEMI-THERM), San Jose, CA, 2017, pp. 302-305.
[11] A. Kulkarni and V. John, "Thermal model for paralleled surface-mount power MOSFETs," 2014 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Mumbai, 2014, pp. 1-6.
[12] R. Jagannathan, H. Hoenes and T. Duggal, "Impacts of package, layout and freewheeling diode on switching characteristics of Super Junction MOSFET in automotive DC-DC applications," 2016 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Trivandrum, 2016, pp. 1-6.