# C65SPACE

## Rad hard 65nm CMOS technology platform for space applications

**Data brief**

## Features

### Process

- STMicroelectronics C65SPACE (65nm CMOS)
- 3.3V IO gate oxide GO2 (5nm)
- 1.2V core gate oxide GO1 (1.8nm), triple VT transistors
- 7 copper metallization,5 thin and 2 thick
- Low-K inter-metallic dielectrics for thin metal layers
- High density SRAMs
- Compatible with flip-chip and wire bonding packaging

### Radiations

- SEL-free up to LET = 60Mev/mg/cm2 at 125°C Tj and Vdd max
- SEE hardened library
- Tested up to a total dose of 300 krads (Si)

### Reliability

- Library cells models with 20 years aging
- Transistor models including aging alteration
- ESD better than:
  - 2kV in HBM (Class 2 / MIL-STD-883H)
  - 150V in MM
  - 250V in CDM

### Library offer

- Comprehensive library of standard logic with PVT and aging corners models
- IO pad libraries provide interfaces at 3.3V +/- 0.30V, 2.5V+/-0.25V and 1.8V +/-0.15V
- High speed IO Pad LVDS supplied at 2.5V +/- 0.25V up to 650Mbps
- Cold sparing IOs with single/double row support
- Memories generation: single port SRAM, ROM, Dual port SRAMs, BIST library, EDAC library
- Wide-range PLLs 1.2GHz with multi-phase outputs
- 6.25Gbit/s high speed serial links (HSSL)

### Design flow

- An ST customized design flow (RTL to GDS) invoking commercial solutions (Synopsys, Cadence, Mentor…) is available for partners and certified design houses:
  - Front-End kit from RTL to gates based
  - SiPKit for IO ring generation
  - FFKit for place and route
  - SignOffKit for final verification before tape-out
- For customer owned tools (COT) flow, ST provides the C65SPACE design platform along with the DRM and sign-off kit.

## Description

The C65SPACE is fabricated on a proprietary 65nm, 7 metal layers CMOS process intended for use with a core voltage of 1.2V ±0.10V.
The ST standard-cells, memories and PLL have been designed and characterized to be compatible with each other.

# 1 Model conditions

The different model conditions are defined as described in *Table 1*.

**Table 1. Model conditions**

| Process | Voltage | Tj | Aging |
|---|---|---|---|
| Nominal | 1.2V | 25°C | Fresh |
| Slow | 1.1V | 125°C | Fresh |
| | | -40°C | Fresh |
| | | 125°C | 20 years |
| Fast | 1.3V | 125°C | Fresh |
| | | -40°C | Fresh |
| | | -40°C | 20 years |

# 2 Revision history

**Table 2. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 02-Feb-2015 | 1 | Initial release. |

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