STEVAL-LDO001V1

Quad high performance LDO evaluation board based on LDBL20, LDLN025, LD39130S and STLQ020

Features
- Multi LDO evaluation board based on four high performance low dropout linear voltage regulators in miniature packages
- Key features:
  - Low operating input voltage (from 1.4 V to 5.5 V)
  - Current capability from 200 mA to 300 mA
  - Low dropout (down to 160 mV typ.)
  - Ultra-low quiescent current (down to 500 nA typ.)
  - Low noise (down to 6.5 μVRMS typ.)
  - High PSSR (up to 80 dB)
  - Logic controlled electronic shutdown (enable)
  - Tiny packages (DFN-6L, Flip-chip, ST STAMP™)
- RoHS compliant

Applications
- Wearable devices
- IoT
- Battery operated devices
- Smart phones
- Smart watches
- Fit bands
- Smart textile
- Wireless sensor networks

Description
The STEVAL-LDO001V1 board features the following high performance low dropout linear voltage regulators in miniature packages:
- LDBL20 200 mA high PSSR low quiescent current in ST STAMP™ bumpless chip-scale package
- LDLN025 250 mA low noise, low quiescent current in Flip-Chip4
- LD39130S 300 mA ultra-low quiescent current in DFN6L
- STLQ020 200 mA very-low quiescent current in DFN6L

Using the quad LDO board with state-of-the-art very low dropout voltage regulators, you can easily evaluate performance levels in a single set-up to choose the best design solution.

The four miniaturized LDOs are designed for extend battery life in portable smart devices.
# Key parameters

Summary table with key parameters:

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Vout version</th>
<th>Vout</th>
<th>Iout</th>
<th>Package</th>
<th>Key features</th>
</tr>
</thead>
<tbody>
<tr>
<td>LDBL20D-25R</td>
<td>Fixed</td>
<td>2.5</td>
<td>200</td>
<td>STSTAMP™ 0.47 x 0.47 mm²</td>
<td>Tiny Package; High PSRR (80 dB @ 1 kHz, 50 db @ 100 kHz typ)</td>
</tr>
<tr>
<td>LDLN025J33R</td>
<td>Fixed</td>
<td>3.3</td>
<td>250</td>
<td>Flip-Chip4</td>
<td>Low Noise 6.5 μVRMS typ High PSRR 80 db @ 1 kHz typ</td>
</tr>
<tr>
<td>LD39130SPUR</td>
<td>Adjustable</td>
<td>3.3</td>
<td>300</td>
<td>DFN6L 1.2 x 1.3 mm</td>
<td>Very low quiescent current: 1 μA in automatic green mode; Output voltage</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>tolerance: ± 1.0 % at 25 °C</td>
</tr>
<tr>
<td>STLQ020PUR</td>
<td>Adjustable</td>
<td>3.3</td>
<td>200</td>
<td>DFN6L 2 x 2 mm</td>
<td>Ultra-low quiescent current: 400 nA at no load</td>
</tr>
</tbody>
</table>

Key product features:

- **LDBL20**
  - Input voltage from 1.5 to 5.5 V
  - Ultra-low dropout voltage (200 mV typ. at 200 mA load)
  - Very low quiescent current: 20 μA typ. at no-load, 0.03 μA typ. in off mode
  - Output voltage tolerance: ±1.5 % @ 25 °C
  - 200 mA guaranteed output current
  - High PSRR (80 dB @ 1 kHz, 50 db @ 100 kHz)
  - Wide range of output voltages available on request: from 0.8 V up to 5.0 V in 50 mV step
  - Logic-controlled electronic shutdown
  - Internal soft-start
  - Optional output voltage discharge feature
  - Compatible with ceramic capacitor (COUT = 0.47 μF)
  - Internal constant current and thermal protections
  - Available in STSTAMP™ (0.47 x 0.47 mm²) package
  - Operating temperature range: -40 °C to 125 °C

- **LDLN025**
  - Ultra-low output noise: 6.5 μVRms
  - Operating input voltage range: 1.5 V to 5.5 V
  - Output current up to 250 mA
  - Very low quiescent current: 12 μA at no-load
  - Controlled Iq in dropout condition
  - Very low-dropout voltage: 250 mV at 250 mA
  - Very high PSRR: 80 dB @ 100 Hz, 60 dB @ 100 kHz
  - Output voltage accuracy: 2% across line, load and temperature
  - Output voltage versions: from 1 V to 5 V, with 50 mV step
  - Logic-controlled electronic shutdown
  - Output discharge feature
  - Internal soft-start
  - Overcurrent and thermal protections
  - Temperature range: from -40 °C to +125 °C
Key parameters

- **LD39130S**
  - Input voltage from 1.4 V to 5.5 V
  - Ultra-low dropout voltage (300 mV typ. at 300 mA load)
  - Automatic green mode
  - Very low quiescent current: 1 μA in green mode, 45 μA in normal mode and 0.1 μA typ. in off mode
  - Output voltage tolerance: ±1.0 % at 25 °C
  - 300 mA guaranteed output current
  - Wide range of output voltages available on request: adjustable from 0.8 V, fixed up to 4.0 V in 100 mV step
  - Logic-controlled electronic shutdown
  - Internal soft-start
  - Compatible with ceramic capacitor (COUT = 330 nF)
  - Internal current foldback and thermal protections
  - Available in DFN6L 1.2 x 1.3 mm and Flip-chip 4 bumps 0.69 x 0.69 mm. 0.4 pitch
  - Operating temperature range: -40 °C to 125 °C

- **STLQ020 (under development)**
  - Operating input voltage range: 2 V to 5.5 V
  - Output current up to 200 mA
  - Ultra-low quiescent current: 400 nA at no load; 100 μA at 200 mA load
  - Controlled Iq in dropout condition
  - Very low dropout voltage: 160 mV at 200 mA
  - Output voltage accuracy: 2% at room temp.; 3% in full temp. range
  - Output voltage versions: from 0.8 V to 4.5 V, with 50 mV step and adjustable
  - Logic-controlled electronic shutdown
  - Output discharge feature (optional)
  - Internal overcurrent and thermal protections
  - Temperature range: from -40 °C to +125 °C
  - Packages: DFN6 - 2 x 2 mm, SOT323-5L, Flipchip4 0.8 x 0.8 mm, STSTAMP™
2 Schematic diagram

Figure 1: STEVAL-LDO001V1 circuit schematic
# Pin and connector configuration

## Table 2: Connector_1 pinout (CN1)

<table>
<thead>
<tr>
<th>U1 Pin</th>
<th>4_Vin</th>
<th>4_Vin_f</th>
<th>1_GM</th>
<th>2_GND</th>
<th>2_GND</th>
<th>3_EN</th>
<th>6_Vout</th>
<th>6_Vout</th>
</tr>
</thead>
<tbody>
<tr>
<td>CN1 upper strip</td>
<td>2_Vin_s</td>
<td>4_Vin_f</td>
<td>6_GM</td>
<td>8_GND</td>
<td>10_GND</td>
<td>12_EN</td>
<td>14_Vout_f</td>
<td>16_Vout_s</td>
</tr>
<tr>
<td>CN1 down strip</td>
<td>1_Vin_s</td>
<td>3_Vin_f</td>
<td>5_GM</td>
<td>7_GND</td>
<td>9_GND</td>
<td>11_EN</td>
<td>13_Vout_f</td>
<td>15_Vout_s</td>
</tr>
</tbody>
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## Table 3: Connector_2 pinout (CN2)

<table>
<thead>
<tr>
<th>U2 Pin</th>
<th>6_Vin</th>
<th>6_Vin</th>
<th>3_GND</th>
<th>3_GND</th>
<th>4_EN</th>
<th>1_Vout</th>
<th>1_Vout</th>
</tr>
</thead>
<tbody>
<tr>
<td>CN2 upper strip</td>
<td>2_Vin_s</td>
<td>4_Vin_f</td>
<td>6_NC</td>
<td>8_GND</td>
<td>10_GND</td>
<td>12_EN</td>
<td>14_Vout_f</td>
</tr>
<tr>
<td>CN2 down strip</td>
<td>1_Vin_s</td>
<td>3_Vin_f</td>
<td>5_NC</td>
<td>7_GND</td>
<td>9_GND</td>
<td>11_EN</td>
<td>13_Vout_f</td>
</tr>
</tbody>
</table>

## Table 4: Connector_3 pinout (CN3)

<table>
<thead>
<tr>
<th>U3 Pin</th>
<th>2_Vin</th>
<th>2_Vin</th>
<th>4_GND</th>
<th>4_GND</th>
<th>1_EN</th>
<th>3_Vout</th>
<th>3_Vout</th>
</tr>
</thead>
<tbody>
<tr>
<td>CN3 upper strip</td>
<td>2_Vin_s</td>
<td>4_Vin_f</td>
<td>6_NC</td>
<td>8_GND</td>
<td>10_GND</td>
<td>12_EN</td>
<td>14_Vout_f</td>
</tr>
<tr>
<td>CN3 down strip</td>
<td>1_Vin_s</td>
<td>3_Vin_f</td>
<td>5_NC</td>
<td>7_GND</td>
<td>9_GND</td>
<td>11_EN</td>
<td>13_Vout_f</td>
</tr>
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## Table 5: Connector_4 pinout (CN4)

<table>
<thead>
<tr>
<th></th>
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<th></th>
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</thead>
<tbody>
<tr>
<td>CN4 upper strip</td>
<td>2_Vin_s</td>
<td>4_Vin_f</td>
<td>6_NC</td>
<td>8_GND</td>
<td>10_GND</td>
<td>12_EN</td>
<td>14_Vout_f</td>
</tr>
<tr>
<td>CN4 down strip</td>
<td>1_Vin_s</td>
<td>3_Vin_f</td>
<td>5_NC</td>
<td>7_GND</td>
<td>9_GND</td>
<td>11_EN</td>
<td>13_Vout_f</td>
</tr>
</tbody>
</table>
4 Revision history

Table 6: Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
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<tbody>
<tr>
<td>01-Mar-2017</td>
<td>1</td>
<td>Initial release.</td>
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