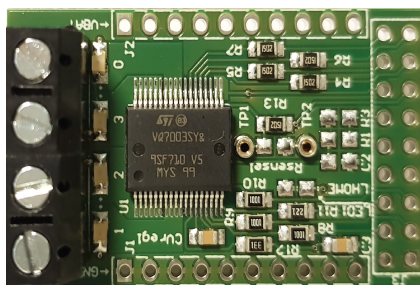


VNQ7003SY Evaluation Board



Features

Channel	V _{CC}	R _{ON} (typ)	I _{LIMH} (typ)
0-1	4 to 28 V	25 mΩ	35 A
2-3		7 mΩ	80 A

- Simple single IC application board dedicated to VNQ7003SY
- Provides electrical connectivity and thermal heat-sinking for easy prototyping
- General device features
 - 16-bit ST-SPI for full diagnostic with 8 bits Short Frame option
 - Programmable Bulb/LED mode for ch. 0-1
 - Advanced limp home functions for robust fail-safe system
 - Very low standby current
 - Optimized electromagnetic emissions
 - Very low electromagnetic susceptibility
 - Control through direct inputs and / or SPI
 - Compliant with European directive 2002/95/EC
- Diagnostic functions
 - Multiplex proportional load current sense
 - Synchronous diagnostic of over load and short to GND, output shorted to VCC and OFF-state open-load
 - Programmable case overtemperature warning
- Protections
 - Two levels load current limitation
 - Self limiting of fast thermal transients
 - Undervoltage shutdown
 - Overvoltage clamp
 - Latch-off or programmable time limited auto restart (power limitation and overtemperature shutdown)
 - Load dump protected
 - Protection against loss of ground

Product status link

[EV-VNQ7003SY](#)

Applications

Typical applications are all types of automotive resistive, inductive and capacitive loads.

Description

This board provides you an easy way to connect ST VIPower M0-7SPI technology into your existing system.

1 Overview

It comes pre-assembled with VNQ7003SY high-side driver. On board minimum set of electrical components (as for device datasheet recommendation) is enabling the user to directly connect the load, the power supply and the microcontroller without any additional effort in external component design and connection.

The VNQ7003SY is a device made using STMicroelectronics® VIPower® technology. It is intended for driving resistive or inductive loads directly connected to ground. The device is protected against voltage transient on VCC pin. An 8 bit short frame access to output control registers is provided allowing PWM control through SPI with high granularity. An analog current feedback for each channel is connected to the CURRENT-SENSE pin via a multiplexer. The device detects open-load in OFF-state conditions.

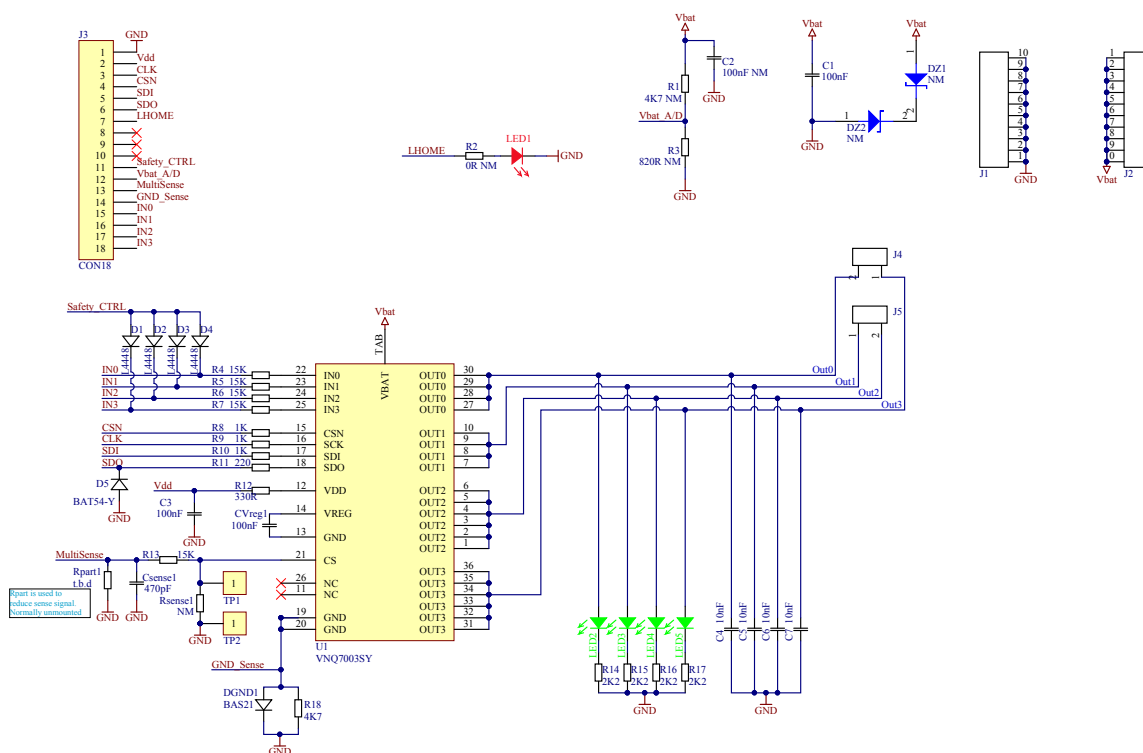
Real time diagnostic is available through the SPI bus (open-load, output short to VCC, overtemperature, communication error, power limitation or latch off).

Output current limitation protects the device in an over load condition. The device can limit the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown can be configured as latched off or programmable time limited auto restart.

The device enters a limp home mode in case of loss of digital supply (VDD), reset of digital memory or watchdog monitoring time-out event. In this mode states of channel 0, 1, 2 or 3 are respectively controlled by four dedicated pins IN0, IN1, IN2 and IN3.

Channel 0 and 1 can be programmed via SPI for load type (BULB/ LED mode).

Figure 1. EV-VNQ7003SY schematic



2 Board connections

Figure 2. Evaluation board connections shows the placement of the connectors to be used for supplying the evaluation board, connecting the load and controlling the functionality and diagnostic of the device.

Figure 2. Evaluation board connections

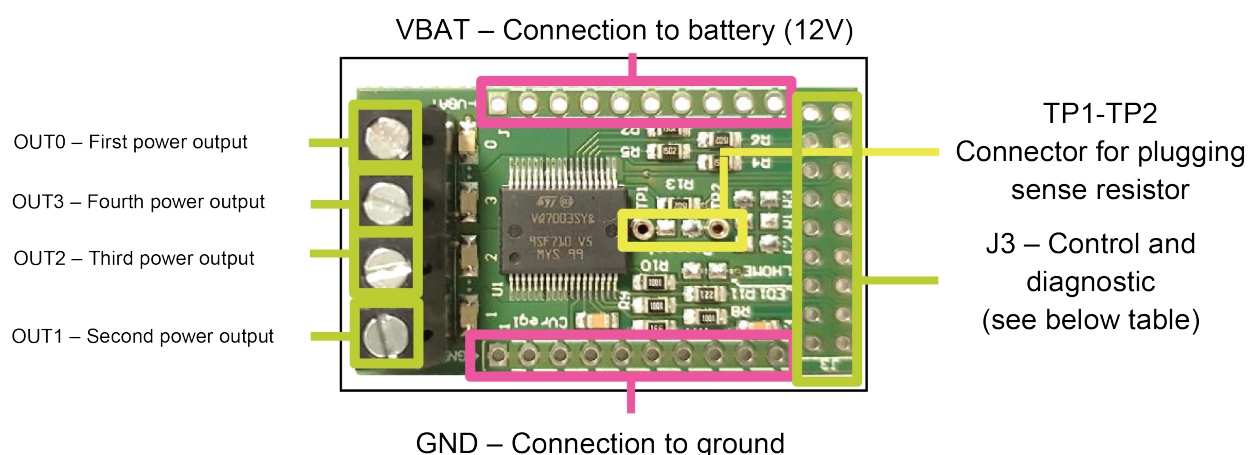


Table 1. J3 connector: pin functions

Connector	Pin number	Pin name	Pin function
J3	1	GND	Ground connection. This pin serves as the ground connection for the logic part of the device.
J3	2	Vcc	Battery connection. This is the backside TAB and is the direct connection to drain Power MOSFET switches.
J3	3	SCK	Serial clock. It is a CMOS compatible input.
J3	4	CSN	Chip select not (active low). It is the selection pin of the device. It is a CMOS compatible input.
J3	5	SDI	Serial data input. Transfers data to be written serially into the device on SCK rising edge.
J3	6	SDO	Serial data output. Transfers data serially out of the device on SCK falling edge.
J3	7	LHOME	Turn on the LED indicator in order to point out Limp Home Mode.
J3	8...10	N/A	
J3	11	Safety_CTRL	In case of a safety condition, sets direct inputs to a defined condition.
J3	12	Vbat_A/D	Monitor Vbat value.
J3	13	CurrentSense	Analog CurrentSense generator proportional to output current. CurrentSense can be programmed as bulb/LED mode for each channel. The pin can deliver the CurrentSense of OUTPUT 0, 1, 2 or 3. The value of resistance that is connected between the CurrentSense pin and device ground determines the reading level for the microcontroller.

Connector	Pin number	Pin name	Pin function
J3	14	GND_Sense	Ground connection. This is a Kelvin ground connection for the logic part of the device and is used to connect an external EMC capacitor to the VREG pin. It must not be connected to application ground.
J3	15...18	IN _{0,1,2,3}	Direct Input pin for channel 0,1,2,3. Control the OUTPUT _{0,1,2,3} state in limp home mode, and is ORed to SPI control register in normal operating mode when corresponding bit is set in DIENCR (Direct Input ENable) control register.

In case the user wishes to utilize the Current Sense / MultiSense function of the device, it is necessary to plug a sense resistor in Rsense.

The package includes a through-hole resistor, to be mounted on TP1-TP2 - see [Figure 4. Mounting through-hole sense resistor](#).

Different Rsense values can be adopted based on user preference.

Another option is soldering an SMD resistor on the dedicated PCB pad, as shown in [Figure 5. Pads for soldering SMD resistor](#).

Figure 3. No sense resistor



Figure 4. Mounting through-hole sense resistor

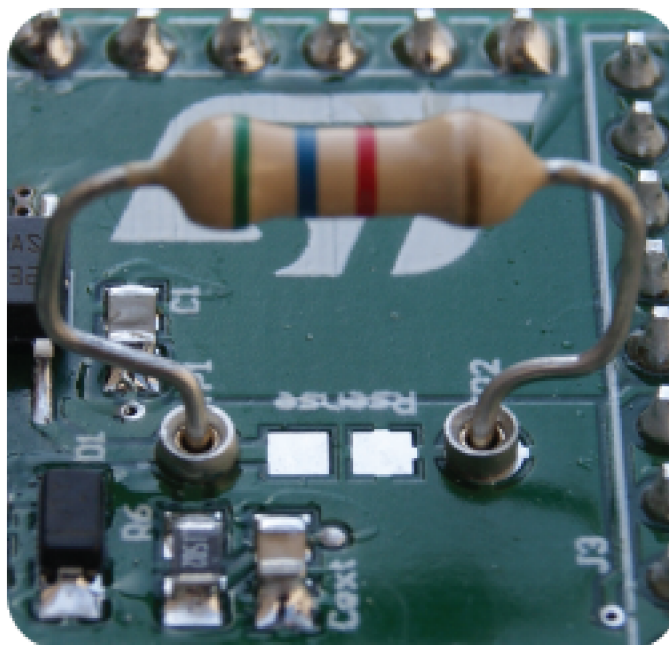
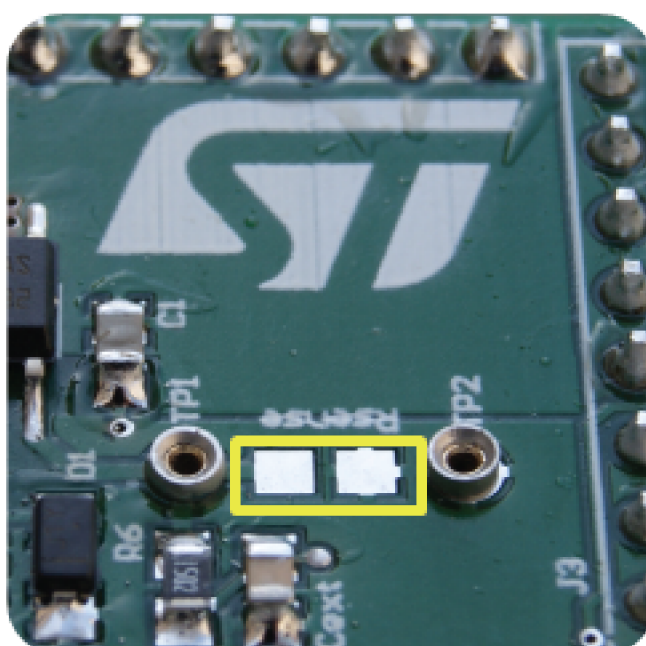


Figure 5. Pads for soldering SMD resistor



3 Thermal data

Table 2. EV-VNQ7003SY thermal data

Symbol	Parameter	Max	Unit
Rthj-amb	Thermal resistance junction-ambient (MAX)	39°	°C/W

Table 3. PCB specifications

Parameter	Value
Board dimensions	25 mm x 41.5 mm
Number of Cu layer	2
Layer Cu thickness	35 µm
Board finish thickness	1.6 mm +/- 10%
Board Material	FR4
Thermal vias diameter	0.3 mm

Revision history

Table 4. Document revision history

Date	Revision	Changes
01-Dec-2017	1	Initial release.
26-Jul-2018	2	Updated features in cover page.

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