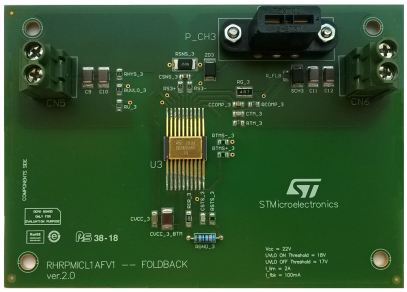
EVAL-RHRICL1AFV1

Data brief

EVAL-RHRICL1AFV1 evaluation board - foldback



Features

- V_{CC} = 22 V
- UVLO on threshold = 18 V
- UVLO off threshold = 17 V
- I_lim = 2 A
- I_fbk = 100 mA

Description

The EVAL-RHRICL1AFV1 evaluation board has been developed for the RHRPMICL1A rad-hard integrated current limiter IC, which is able to work with an external P-channel power MOSFET. Further information can be found in the datasheet available on the web.

The RHRPMICL1A features 3 user-configurable operating modes (re-triggerable, latch, foldback), with different behaviors in case of overload/short-circuit events. Each evaluation tool comes with all external components needed for a complete electrical evaluation of the device functionality in the selected configuration.

The EVAL-RHRICL1AFV1 evaluation board is intended for evaluation purposes only.

Product status link
EVAL-RHRICL1AFV1

Product summary	
Type	Evaluation tool
Order code	EVAL-RHRICL1AFV1
Configuration	Foldback
Marking	RHRPMICL1AFV1-foldback

1 Bill of material of the EVAL-RHRICL1AFV1 board

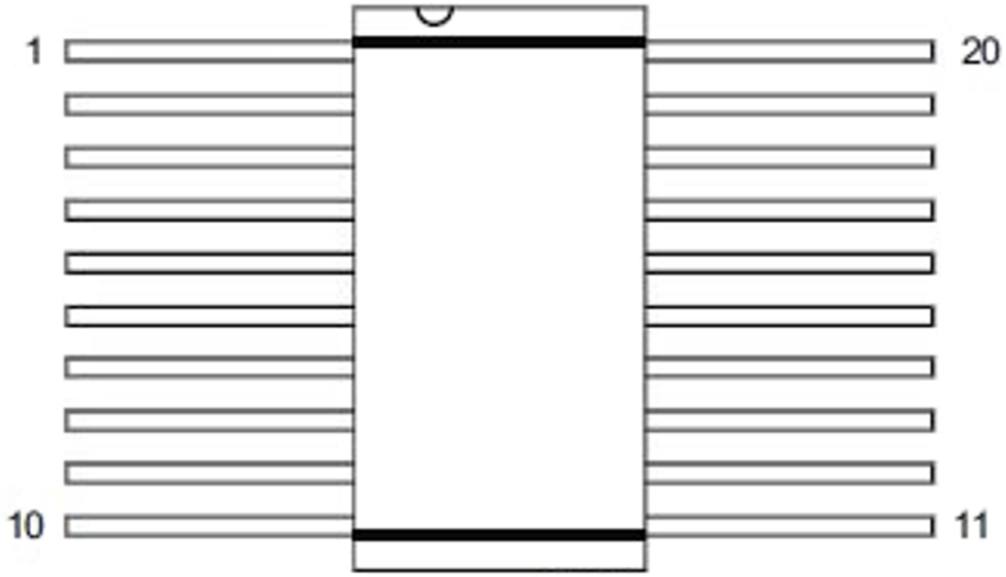
Table 1. Bill of material

Item	Qty	Reference	Part /value	Voltage current	Package	Manufacturer	Manufacturer code	More info	Footprint
1	2	CN5, CN6	2PIN screw connector	Pitch-6.35 mm	TH	Phoenix contact	1714955	Input (CN1) and ouput (CN2) connectors	
2	4	C9,C10,C11, C12	4.7 µF capacitor	100 V	1812	TDK	C4532X7S2A475M	X7S	1812
3	1	CVcc_3_btm	4.7 µF capacitor	100 V	1812	TDK	C4532X7S2A475M	X7S	1812
4	1	CVcc_3	100 nF	100 V	1206	MULTICOMP	MCCA000490	X7R	1206
5	1	Csns_3	1 µF	10 V	0805	KEMET	C0805C105K8NACTU	X8L	0805
6	1	Ccomp_3	2.2 nF	50 V	0805	AVX	08055C222JAT2A	X7R	0805
7	2	C_TM_3 C_STS_3	47 pF	50 V	0805	KEMET	C0805C470J5GACTU	NPO	0805
8	1	Rv_3	220 kΩ	100 V, 0.1%, 25 ppm/°C	0.125 W	Panasonic	ERA6AEB224V		0805
9	2	Rtms+_3, Rtms-_3	5 kΩ	150 V, 0.1%, 5 ppm/°C	0.200 W	Vishay thin film	PNM0805E5001BST5		0805
10	1	Rtm_3	100 kΩ	100 V, 0.1%, 25 ppm/°C	0.125 W	Panasonic	ERA6AEB104V	I=20 µA	0805
11	1	Rsts_3	50 kΩ	100 V, 0.1%, 25 ppm/°C	0.200 W	Vishay	PNM0805E5002BST5	I=100 µA	0805
12	1	RGND_3 (R_floating)	1.2 kΩ	1%	0.6 W	Vishay	MBB02070C1201FCT00	I=2 mA	TH
13	1	Rg_3	4.7Ω	200 V, 1%	1 W	Panasonic	ERJB1BF4R7U		1020
14	1	R_flb	107 kΩ	0.1 W, 0.1% ± 25 ppm/°C	100 mW	Multicomp	MCTC0525B1073T5E		0805
15	1	Rsns_3	50 mΩ	1W, 1% ± 75 ppm/°C	1 W	Vishay DALE	WSL2512R0500FEA		2512
16	2	RS3+ RS3-	470 Ω	100 V, 0.1%, 25 ppm/°C	125 mW	Panasonic	ERA6AEB471V		0805
17	1	Rhys_3	2.61 kΩ	100 V, 0.1%, 25 ppm/°C	0.100 W	TE CONNECTIVITY	RN73C2A2K61BTDF		0805
18	1	Ruvlo_3	35.7 kΩ	100 V, 0.1%, 25 ppm/°C	0.100 W	TE CONNECTIVITY	RN73C2A35K7BTDF		0805
19	1	Rcomp_3	1 kΩ	0.1%, 25 ppm/°C	125 mW	Panasonic	ERA6AEB102V		0805
20	1	Rir_3	100 kΩ	100 V, 0.1%, 25 ppm/°C	0.250 W	Panasonic	ERA8AEB104V	I=10 µA	1206
21	1	ZD3	ZENER	15 V, 3 W		ON SEMICONDUCTORS	1SMB5929BT3G	Zener	SMB-CASE403A

Item	Qty	Reference	Part /value	Voltage current	Package	Manufacturer	Manufacturer code	More info	Footprint
22	1	SCH3	STPS3150	3 A, 150 V		ST	STPS3150U	Diode100 V-5 A	SMB
23	1	P_ch3 SOCKET	P-ch TO254 AA socket (for the STRH40P10)	34 A, 100 V		3M TOUCH SYSTEMS	203-2737-55-1 102	P-channel, B_{Vdss} 100 V, Id 48 A, $R_{DS(on)}$ 60 mΩ, Qg 162 nC	TO-254 AA
24	1	U1	ICL001		FLAT20	ST			FLAT20

2 Device pin configuration

Figure 1. **RHRPMICL1A pin connections**



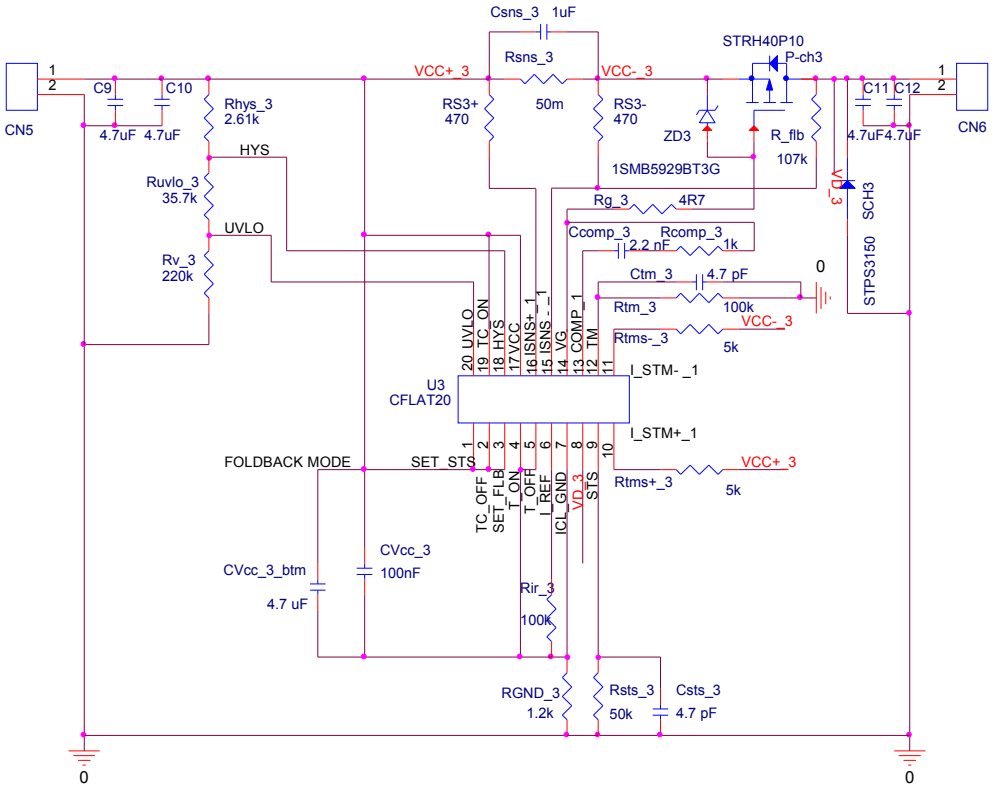
Note: Metallic lid is connected to ground

Table 2. Pin connections

#Pin	Name	Type	Description
1	SET_STS	Digital input	Configuration pin. If shorted-to -ND, the current limiter at power-up is OFF. If connected to VCC, the current limiter at power-up is normally ON
2	TC_OFF	Digital input	Telecommand interface input for OFF pulsed signal
3	SET_FLB	Digital input	Configuration pin. If connected to VCC, the foldback mode is enabled
4	TON	Analog output	Used to set the trip-off time TON. A capacitor CON is connected between this pin and GND
5	TOFF	Analog output	Used to set the recovery time TOFF. This pin has a double function. If the COFF capacitor is connected between this pin and GND, it sets the TOFF value in re-triggerable mode. If the pin is shorted-to-GND, the device is configured in latched mode
6	I_REF	Analog input/ output	Used to set the current reference. An external high-precision resistor is connected between this pin and GND in order to set the current reference
7	GND	Power supply	Ground. Return of the bias current and zero-voltage reference for all internal voltages. Connected to the main bus ground through a decoupling resistor to operate in floating ground configuration
8	VD	Analog input	Sense pin of the external MOSFET drain voltage used to detect current limitation. A small series resistor can be useful to reduce power dissipation
9	STS	Digital output	Telemetry digital status. A resistor has to be connected between the pin and the main bus ground
10	TMS+	Analog input	Non-inverting input of the telemetry circuit. An accurate external resistor is connected between ISNS+ and this pin in order to guarantee the requested accuracy on the output source current for the analog telemetry
11	TMS-	Analog input	Inverting input of the telemetry circuit. An accurate external resistor is connected between ISNS- and this pin in order to guarantee the requested accuracy on the output source current for the analog telemetry
12	TM	Analog output	Output source current for the analog telemetry. A resistor has to be connected between this pin and the main bus ground.
13	COMP	Analog output	Output pin for current limitation loop compensation
14	Vg	Analog output	MOSFET gate driver output
15	ISNS-	Analog input	Inverting input of the op-amp current limitation loop. The pin is tied directly to the hot (negative) end of the external current sense resistor
16	ISNS+	Analog input	Non-inverting input of the op-amp current limitation loop. The pin is tied directly to the hot (positive) end of the external current sense resistor
17	VCC	Power supply	Supply input voltage
18	HYS	Analog output	External setting of the UVLO hysteresis. A resistor has to be connected between the main bus and this pin
19	TC_ON	Digital input	Telecommand interface input for ON pulsed signal
20	UVLO	Analog input	External setting of the UVLO turn-on threshold. The pin has to be tied to the midpoint of a resistor divider that senses the supply voltage vs. main bus ground

3 Schematic of the EVAL-RHRICL1AFV1 board

Figure 2. EVAL-RHRICL1AFV1 schematic



4 Layout of the EVAL-RHRICL1ALV1 board

Figure 3. **EVAL-RHRICL1ALV1 top layout**

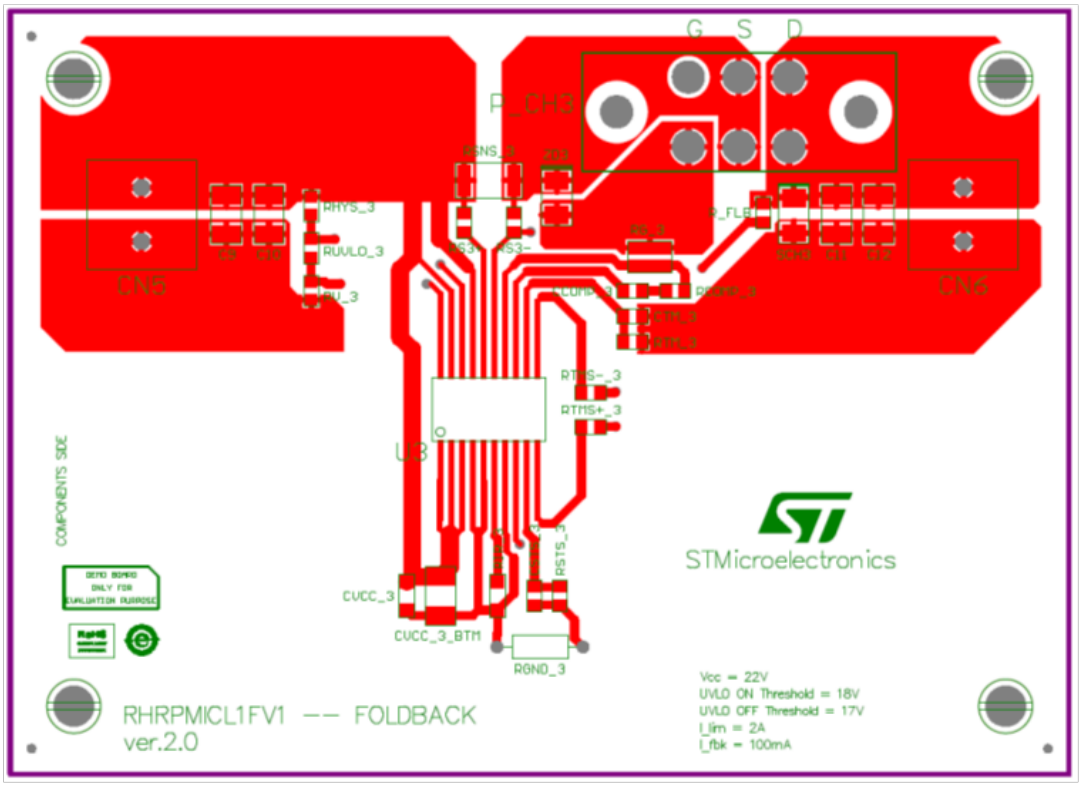
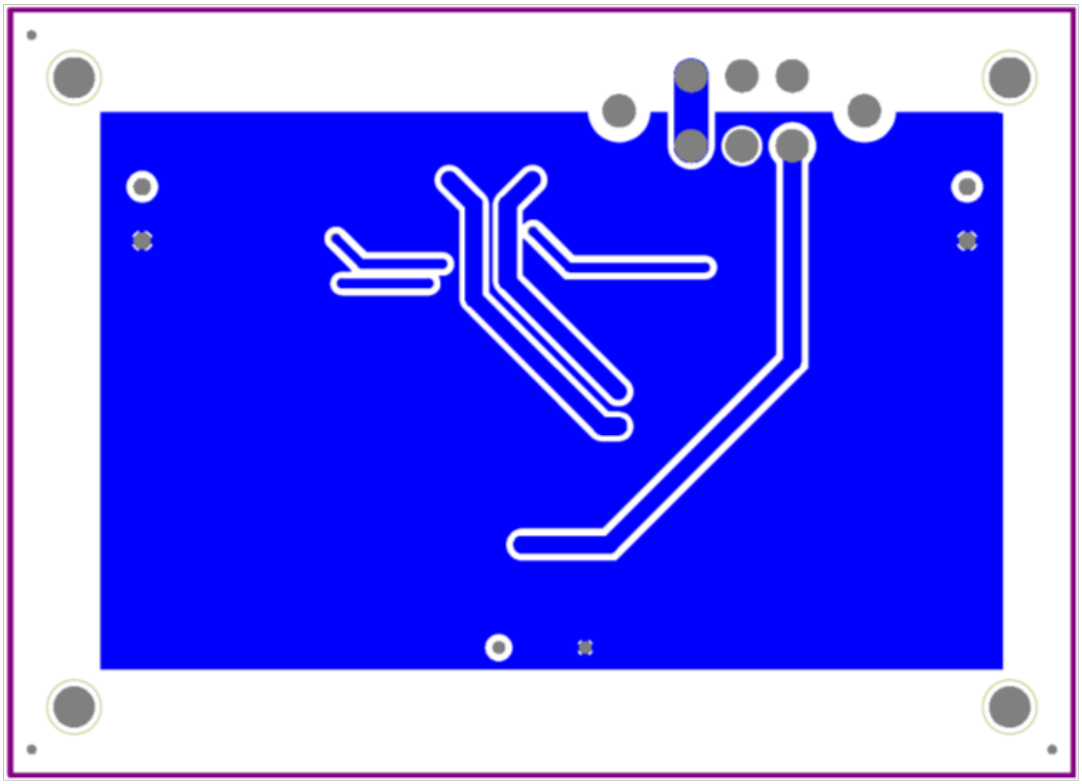


Figure 4. **EVAL-RHRICL1ALV1 bottom layout**



Revision history

Table 3. **Document revision history**

Date	Version	Changes
18-Jul-2019	1	Initial release.

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