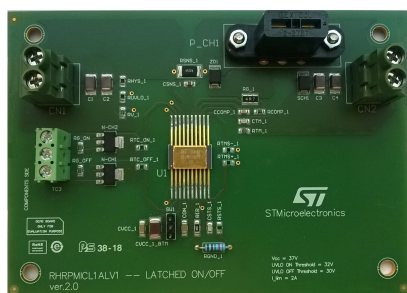


## EVAL-RHRICL1ALV1 evaluation board - latched



### Features

- $V_{CC} = 37\text{ V}$
- UVLO on threshold = 32 V
- UVLO off threshold = 30 V
- $I_{lim} = 2\text{ A}$

### Description

The **EVAL-RHRICL1ALV1** evaluation board has been developed for the RHRPMICL1A rad-hard integrated current limiter IC, which is able to work with an external P-channel power MOSFET. Further information can be found in the datasheet available on the web.

The RHRPMICL1A features 3 user-configurable operating modes (re-triggerable, latch, foldback), with different behaviors in case of overload/short-circuit events. Each evaluation tool comes with all external components needed for a complete electrical evaluation of the device functionality in the selected configuration.

The **EVAL-RHRICL1ALV1** evaluation board is intended for evaluation purposes only.

#### Product status link

[EVAL-RHRICL1ALV1](#)

#### Product summary

Type	Evaluation tools
Order code	EVAL-RHRICL1ALV1
Configuration	Latched
Marking	RHRPMICL1ALV1 - latched on/off

## 1 Bill of material of the EVAL-RHRICL1ALV1 board

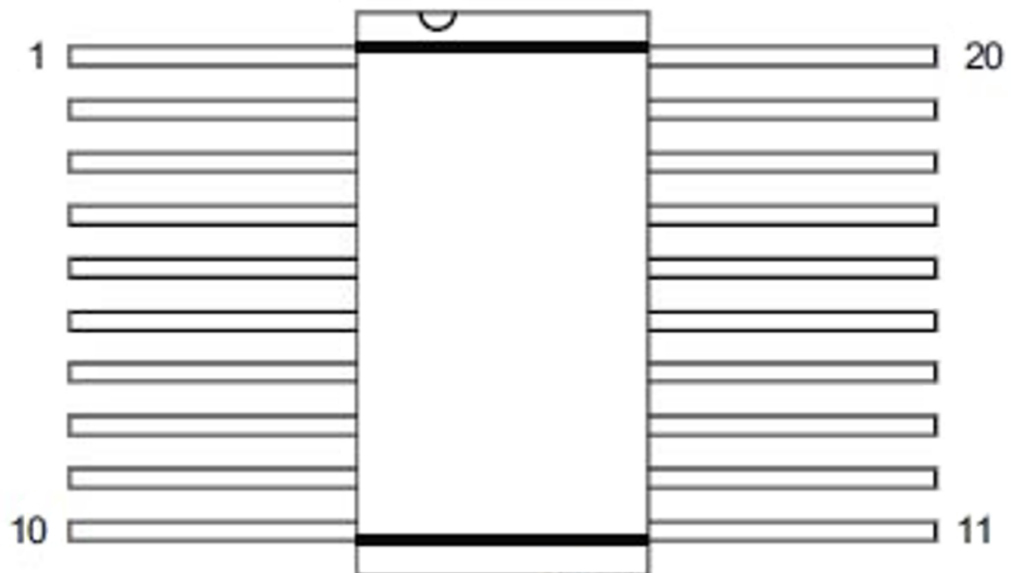
**Table 1. Bill of material of the EVAL-RHRICL1ALV1 board**

Item	Qty	Reference	Part/ value	Voltage current	Package	Manufacturer	Manufacturer code	More info	Footprint
1	2	CN1, CN2	2 PIN screw connector	Pitch-6.35 mm	TH	Phoenix contact	1714955	INPUT (CN1) and OUTPUT (CN2) connectors	
2	4	C1,C2,C3,C 4	4.7 $\mu$ F capacitor	100 V	1812	TDK	C4532X7S2A4 75M	X7S	1812
3	1	CVcc_1_bt m	4.7 $\mu$ F capacitor	100 V	1812	TDK	C4532X7S2A4 75M	X7S	1812
4	1	CVcc_1	100 nF	100 V	1206	MULTICOMP	MCCA000490	X7R	1206
5	1	Csns_1	1 $\mu$ F	10 V	0805	KEMET	C0805C105K8 NACTU	X8L	0805
6	1	Ccomp_1	2.2 nF	50 V	0805	AVX	08055C222JAT 2A	X7R	0805
7	2	C_TM_1 C_STS_1	47 pF	50 V	0805	KEMET	C0805C470J5 GACTU	NPO	0805
8	1	Con_1	100 nF	50 V	1206	AVX	12065C104KA T2A	X7R	1206
9	1	Rv_1	220 k $\Omega$	100 V, 0.1%, 25 ppm/ $^{\circ}$ C		Panasonic	ERA6AEB224V	0.125 W	0805
10	2	Rtms+_1, Rtms-_1	5 k $\Omega$	100 V, 0.1%, 25 ppm/ $^{\circ}$ C		Vishay thin film	PNM0805E500 1BST5	0.200 W	0805
11	1	Rtm_1	100 k $\Omega$	100 V, 0.1%, 25 ppm/ $^{\circ}$ C		Panasonic	ERA6AEB104V	I=20 $\mu$ A, 0.125 W	0805
12	1	Rsts_1	50 k $\Omega$	100 V, 0.1%, 25 ppm/ $^{\circ}$ C		Vishay	PNM0805E500 2BST5	I=100 $\mu$ A, 0.200 W	0805
13	1	RGND_1 (R_floating)	8.25 k $\Omega$	1%		Vishay	MBB02070C82 51FCT00	I=2 mA, 0.6 W	TH
14	1	Rg_1	4.7 $\Omega$	200 V, 1%		Panasonic	ERJB1BF4R7U	1 W	1020
15	1	Rsns_1	50 m $\Omega$	1 W, 1% $\pm$ 75 ppm/ $^{\circ}$ C		Vishay DALE	WSL2512R050 0FEA	1 W	2512
16	1	Rhys_1	1.58 k $\Omega$	100 V, 0.1%, 25 ppm/ $^{\circ}$ C		Panasonic	ERA6AEB1581 V	0.125 W	0805
17	1	Ruvlo_1	18.7 k $\Omega$	100 V, 0.1%, 25 ppm/ $^{\circ}$ C		Panasonic	ERA6AEB1872 V	0.125 W	0805
18	1	Rcomp_1	1 k $\Omega$	0.1%, 25 ppm/ $^{\circ}$ C		Panasonic	ERA6AEB102V	125 mW	0805
19	1	Rir_1	100 k $\Omega$	150 V, 0.1%, 25 ppm/ $^{\circ}$ C		Panasonic	ERA8AEB104V	I=10 $\mu$ A, 0.250 W	1206
20	1	SW1	3 way switch						jumper 3vie
21	1	ZD1	ZENER	15 V, 3 W	SMB	ON SEMICONDC TORS	1SMB5929BT3 G	Zener	SMBCASE 403A
22	1	SCH1	STPS3150	3 A, 150 V	SMB	ST	STPS3150U	Diode 100V-5 A	SMB

Item	Qty	Reference	Part/ value	Voltage current	Package	Manufacturer	Manufacturer code	More info	Footprint
23	1	P_ch1 SOCKET	P-ch TO254AA socket (for STRH40P10)	34 A, 100 V		3M TOUCH SYSTEMS	203-2737-55-1 102	P-channel, B <sub>Vdss</sub> 100 V, Id 48 A, R <sub>DS(on)</sub> 60 mΩ, Qg 162 nC	
24	1	U1	ICL001		FLAT20	ST			FLAT20
25	2	N-CH1, N- CH2	STN1NF101A, 100 V	Vgsth = 3 V		ST	STN1NF10	N-ch o NPN from 60 V - 100 V	SOT-223
26	2	Rg_on_1, Rg_off_1	1 kΩ	150 V, 1%		Vishay	CRCW08051K 00FKEA	125 mW	0805
27	2	Rtcon_1, Rtcoff_1	50 kΩ	100 V, 0.1%, 25 ppm/°C	200 mW	VISHAY thin film	PNM0805E500 2BST5	To pull down	0805
28	1	TC3 CONN	3 way screw contact			PHOENIX contact	1935174	Telecomm and external connector	TH

## 2 Device pin configuration

Figure 1. RHRPMICL1A pin connections



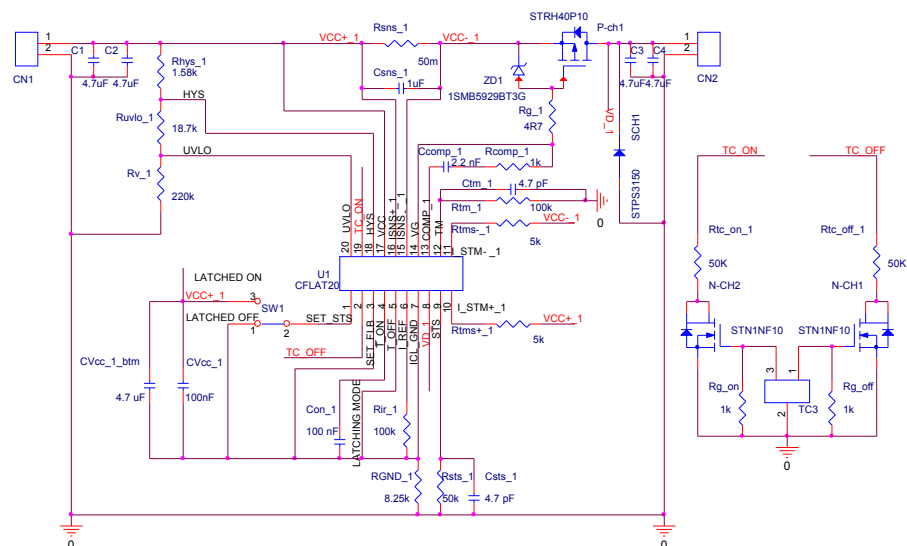
*Note:*      *Metallic lid is connected to ground*

**Table 2. Pin connections**

#Pin	Name	Type	Description
1	SET_STS	Digital input	Configuration pin. If shorted-to -ND, the current limiter at power-up is OFF. If connected to VCC, the current limiter at power-up is normally ON
2	TC_OFF	Digital input	Telecommand interface input for OFF pulsed signal
3	SET_FLB	Digital input	Configuration pin. If connected to VCC, the foldback mode is enabled
4	TON	Analog output	Used to set the trip-off time TON. A capacitor CON is connected between this pin and GND
5	TOFF	Analog output	Used to set the recovery time TOFF. This pin has a double function. If the COFF capacitor is connected between this pin and GND, it sets the TOFF value in re-triggerable mode. If the pin is shorted-to-GND, the device is configured in latched mode
6	I_REF	Analog input/output	Used to set the current reference. An external high-precision resistor is connected between this pin and GND in order to set the current reference
7	GND	Power supply	Ground. Return of the bias current and zero-voltage reference for all internal voltages. Connected to the main bus ground through a decoupling resistor to operate in floating ground configuration
8	VD	Analog input	Sense pin of the external MOSFET drain voltage used to detect current limitation. A small series resistor can be useful to reduce power dissipation
9	STS	Digital output	Telemetry digital status. A resistor has to be connected between the pin and the main bus ground
10	TMS+	Analog input	Non-inverting input of the telemetry circuit. An accurate external resistor is connected between ISNS+ and this pin in order to guarantee the requested accuracy on the output source current for the analog telemetry
11	TMS-	Analog input	Inverting input of the telemetry circuit. An accurate external resistor is connected between ISNS- and this pin in order to guarantee the requested accuracy on the output source current for the analog telemetry
12	TM	Analog output	Output source current for the analog telemetry. A resistor has to be connected between this pin and the main bus ground.
13	COMP	Analog output	Output pin for current limitation loop compensation
14	Vg	Analog output	MOSFET gate driver output
15	ISNS-	Analog input	Inverting input of the op-amp current limitation loop. The pin is tied directly to the hot (negative) end of the external current sense resistor
16	ISNS+	Analog input	Non-inverting input of the op-amp current limitation loop. The pin is tied directly to the hot (positive) end of the external current sense resistor
17	VCC	Power supply	Supply input voltage
18	HYS	Analog output	External setting of the UVLO hysteresis. A resistor has to be connected between the main bus and this pin
19	TC_ON	Digital input	Telecommand interface input for ON pulsed signal
20	UVLO	Analog input	External setting of the UVLO turn-on threshold. The pin has to be tied to the midpoint of a resistor divider that senses the supply voltage vs. main bus ground

### 3 Schematic of the EVAL-RHRICL1ALV1 board

**Figure 2.** EVAL-RHRICL1ALV1 schematic



## 4 Layout of the EVAL-RHRICL1ALV1 board

Figure 3. EVAL-RHRICL1ALV1 top layout

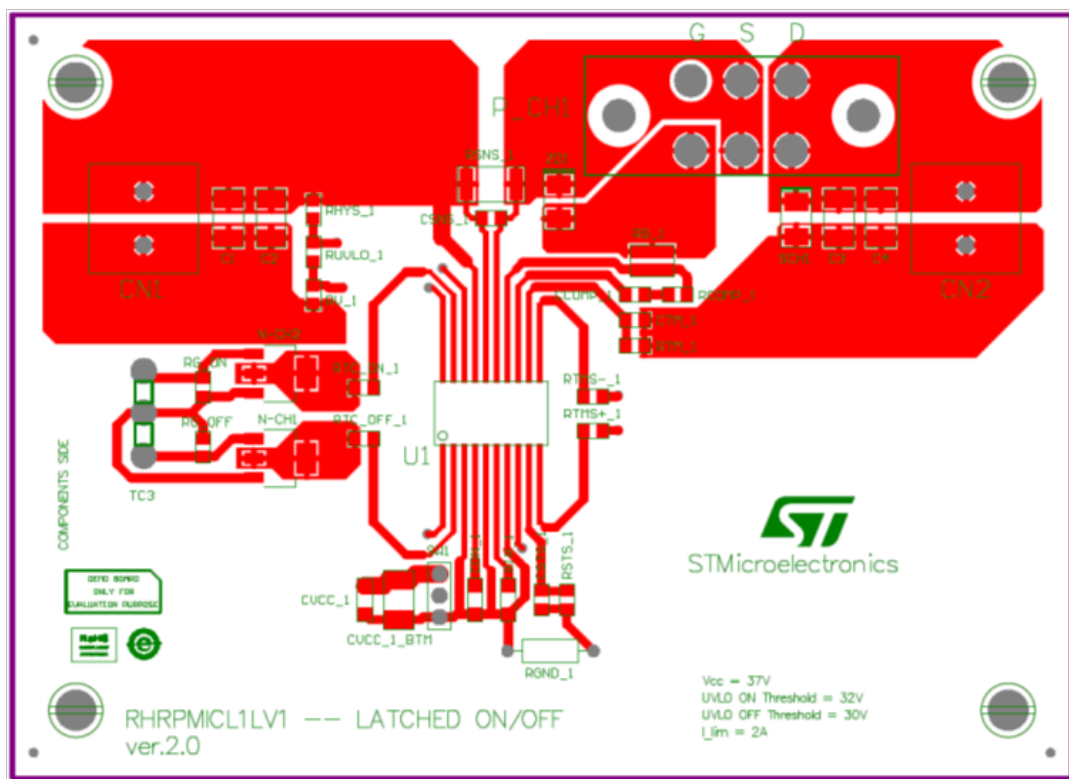
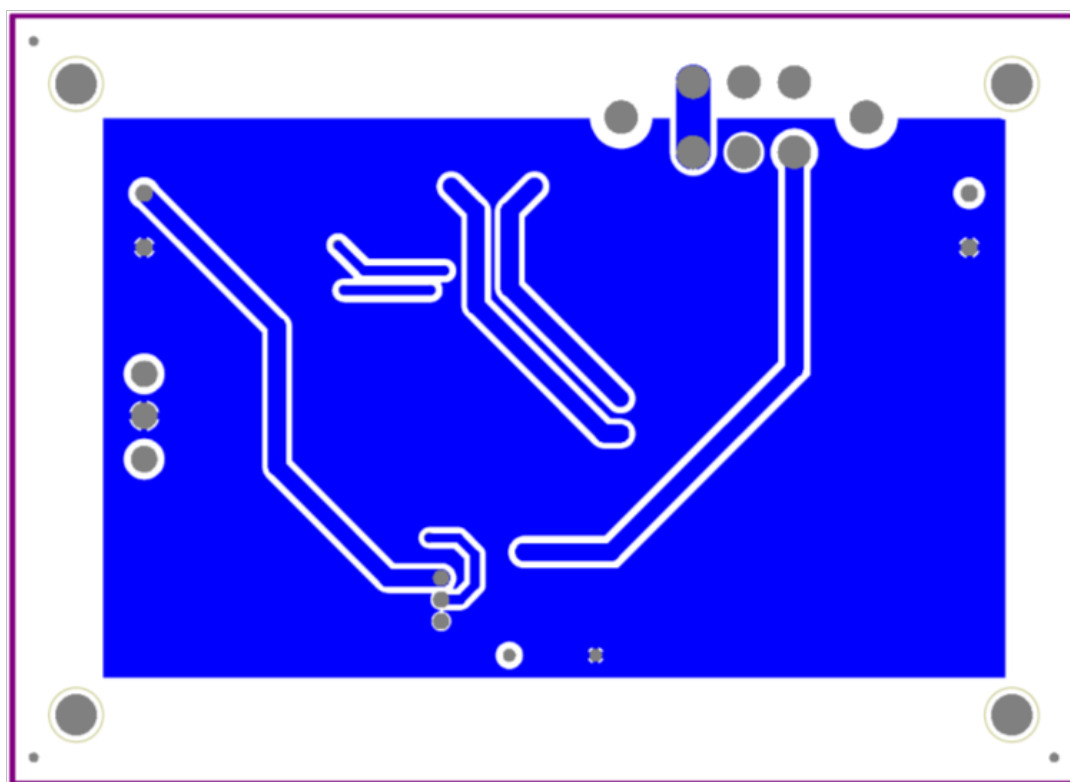


Figure 4. EVAL-RHRICL1ALV1 bottom layout





## Revision history

**Table 3. Document revision history**

Date	Version	Changes
18-Jul-2019	1	Initial release.

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