

Four channel valve driver

Data Brief

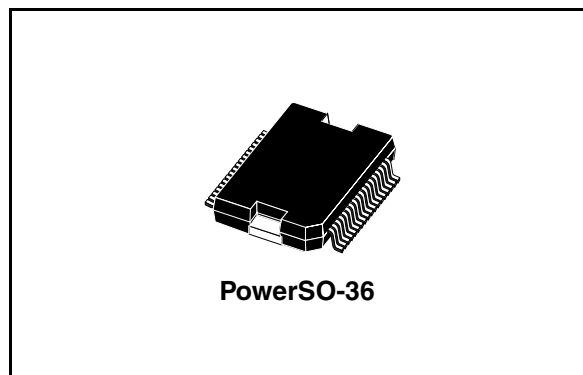
Features

- Four low-side output driver with protection diagnostics.
 - 2 channels designed as conventional switch ($r_{ON} = 0.2 \Omega$ typ.) with integrated 60 V Zener diodes clamp.
 - 2 current controlled channels ($r_{ON} = 0.2 \Omega$ typ.) with current range from 0 mA to 2.25 A typ. with integrated recirculation diodes.
- Output slope control
- Short circuit protection
- Selective overtemperature shutdown
- Open load and over load current detection
- Ground and supply loss detection
- External clock control
- Recirculation path control
- Regulator drift detection
- Regulator error control
- Electrostatic discharge (ESD) protection

Description

The L9352B is designed to drive inductive loads in low side configurations like hydraulic valves used in ABS/ESC systems.

Integrated active Zener diodes clamp (for channel1 and 2) or free wheeling diodes (for channel 3 and 4) allow the recirculation of the inductive loads.



All four channels are monitored with a status output. All wiring to the loads and supply pins of the device are controlled. The device is self-protected against short circuit at the outputs and overtemperature. For each channel, one independent push-pull status output is used for a parallel diagnostic function.

Channel 3 and 4 work as current controlled channels. The target value of the current is given by the duty cycle (DC) of the 2 kHz PWM input signal.

The output current is controlled through the output PWM of the power stage. The regulator limits of 10% or 90% are detected and monitored with the status signal. The current is measured during the recirculation phase of the load. Using an external clock frequency of 250 kHz, the PWM output frequency is 3.9 kHz.

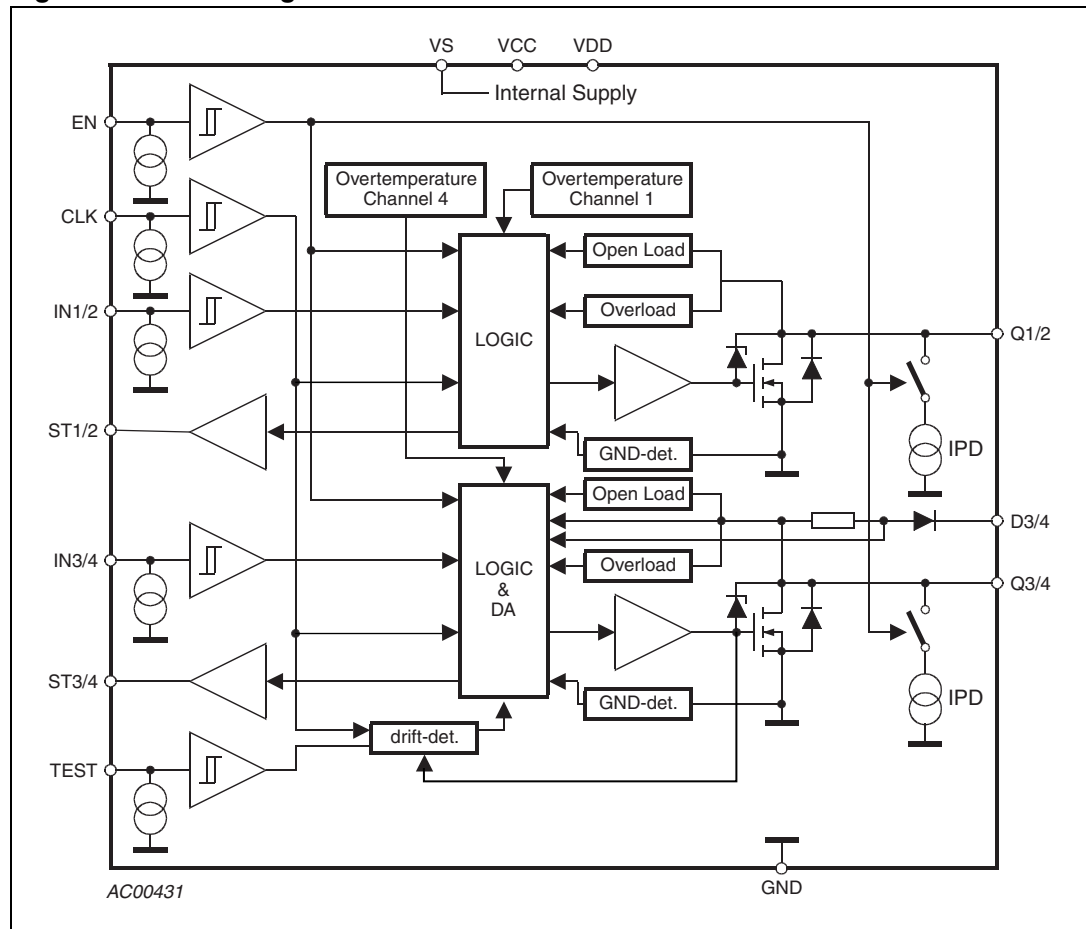
A digital PI (proportional and integrating) regulator is performed in order to internally control the target current basing on the load current measurements.

Table 1. Device summary

Order code	Package	Packing
L9352B-LF	PowerSO-36	Tray
L9352B-TR-LF	PowerSO-36	Tape and reel

1 Block diagram

Figure 1. Block diagram



2 Pins description

Figure 2. Pins connection (top view)

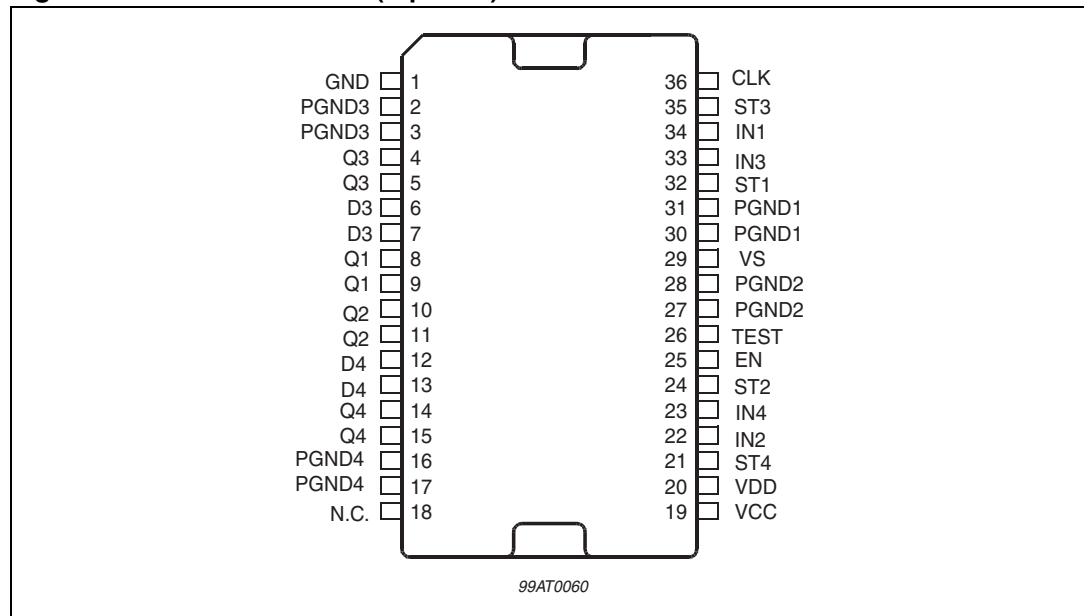


Table 2. Pins description

N°	Pin	Description
1	GND	Logic ground
2, 3	PGND3	Power ground - Channel 3
4, 5	Q3	Power output - Channel 3
6, 7	D3	Free-wheeling diode - Channel 3
8, 9	Q1	Power output - Channel 1
10, 11	Q2	Power output - Channel 2
12, 13	D4	Free-wheeling diode - Channel 4
14, 15	Q4	Power output - Channel 4
16, 17	PGND4	Power ground - Channel 4
18	NC	Not Connected
19	VCC	5 V supply
20	VDD	5 V supply
21	ST4	Status output - Channel 4
22	IN2	Control input - Channel 2
23	IN4	Control input - Channel 4
24	ST2	Status output - Channel 2
25	EN	Enable input for all four channels

Table 2. Pins description (continued)

N°	Pin	Description
26	TEST	Enable input for drift detection
27, 28	PGND2	Power ground - Channel 2
29	VS	Supply voltage
30, 31	PGND1	Power ground - Channel 1
32	ST1	Status output - Channel 1
33	IN3	Control input - Channel 3
34	IN1	Control input - Channel 1
35	ST3	Status output - Channel 3
36	CLK	Clock input

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_S	Supply voltage		-0.3		40	V
V_{CC}, V_{DD}	Supply voltage		-0.3		6	V
V_Q	Output voltage static				40	V
V_Q	Output voltage during clamping	$t < 1 \text{ ms}$			60	V
V_{IN}, V_{EN}	Input voltage IN1 to IN4, EN	$I_I < 110 \text{ mA}$	-1.5		6	V
V_{CLK}	Input voltage CLK		-1.5		6	V
V_{ST}	Output voltage status		-0.3		6	V
V_D	Recirculation circuits D3, D4				40	V
V_{DRmax}	Max. reverse breakdown voltage of free wheeling diodes D3, D4				55	V
$I_{Q1/2}$	Output current for Q1 and Q2		>5		internal limited	A
$I_{Q3/4}$	Output current for Q3 and Q4		>3		internal limited	A
$I_{Q1/2}, I_{PGND1/2}$	Output current at reversal supply for Q1 and Q2		-4			A
$I_{Q3/4}, I_{PGND3/4}$	Output current at reversal supply for Q3 and Q4		-2			A
I_{ST}	Output current status pin		-5		5	mA
E_Q	Switch off energy for inductive loads				50	mJ

3.2 ESD susceptibility

Table 4. Human body model

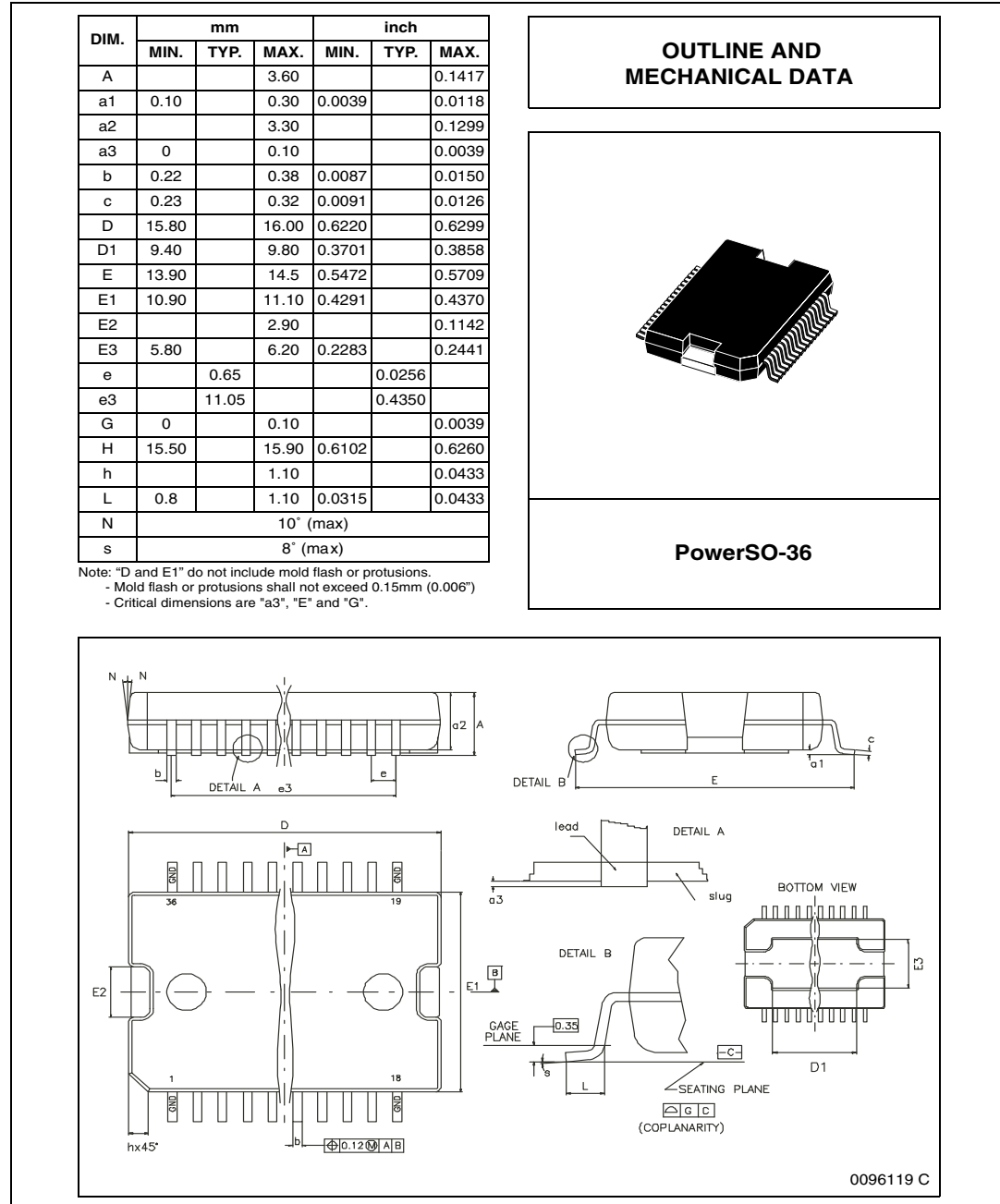
Pin	Conditions	Min	Typ	Max	Unit
All pins		± 2			kV
Output pins (Qx, Dx)	vs. common GND (PGND1-4 + GND)	± 4			kV

4 Package information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 3. PowerSO-36 mechanical data and package dimensions



5 Revision history

Table 5. Document revision history

Date	Revision	Changes
17-Jun-2008	1	Initial release.
17-Sep-2013	2	Updated Disclaimer.

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