Automotive 16 channels chip for advanced airbag applications

TQFP128 exposed pad down
(14x14x1.0 mm)

Product status link
L9691

Product summary		
Order code	**Package**	**Packing**
L9691 -TR	TQFP128EP 14x14x1.0 mm	Tape and reel

Features

- AEC-Q100 qualified
- Single chip and master/slave configurations
- Boost regulator for energy reserve
  - 2 MHz operation
  - Output voltage 24 V/33 V ±6%, user-selectable, peak inductor current regulation
  - Capacitor value and ESR diagnostics
- Boost regulator for low voltage system operation
  - 2 MHz operation
  - Output voltage, 10 V ±8%, 870 mA max
- Buck regulator for remote sensor
  - 2 MHz operation
  - Output voltage, 6.5 V/8 V ±4%, 700 mA max
- Buck regulator for micro controller unit
  - 2 MHz operation
  - Output voltage, 3.3 V ±3%, 450 mA max
- Remote sensor interface and SYNC pulse supply voltage inputs and monitorings
- Linear regulator with external power PNP transistor, 5 V ±5%, 135 mA max
- Integrated energy reserve crossover switch with switch active output indicator, configured as input for slave mode operation
- Battery voltage monitor and shutdown with wake-up control
- System voltage diagnostics with integrated ADCs
- Squib/LEA deployment drivers
  - 16 channel HSD/LSD for squib load
  - 2 over 16 channels supporting LEA load
  - 2 channel couples supporting common-return connection
  - 18 V deployment voltage
  - Low, high and automatic dynamic deployment current profiles
  - R measure, STB, STG and leakage diagnostics
  - High and low side driver FET tests
  - LEA presence diagnostics
- Two isolated high side safing FET regulators and diagnostics
- Eight channel PSI-5 v2.3 remote sensor interface
- Three channel general purpose low side drivers with 0-100% PWM control
- Twelve channel hall-effect, resistive or switch sensor interface
- User-programmable safing logic and rolling average algorithm
- E2E arming procedure through Global SPI
- Temporal watchdog timer
- End-of-life disposal interface
- Temperature sensor
- 32 bit Global SPI bus interface
- 32 bit Remote Sensor SPI bus interface, SafeSPI v1.0 compatible

- LIN v2.2A interface with OCS message decoding capability
- 5.4 V min operating voltage at VIN battery input for start-up
- Full ISO 26262 compliant, ASIL-D systems ready
- Packaging 128 pin

Description

The L9691 is an advanced airbag system chip solution targeted for the global airbag market.

High frequency power supply design optimizes system cost by using smaller and less expensive external components. All switching regulators operate at 2 MHz and all buck converters have integrated synchronous rectifiers.

The reserve capacitor is electrically isolated from the boost regulator by integrated switches and external resistors, controlling in-rush current. A capacitor discharge switch is integrated to discharge the capacitor at shutdown.

Low quiescent current permits the device to be directly connected to battery. In this mode, device start-up and shutdown are controlled through the wake-up input pin (actually, shutdown needs also dedicated SPI command too). The power supply and crossover function are controlled automatically through the internal state machine.

For systems with high feature content, two L9691 devices can be used in a master/slave configuration.

The L9691 provides two fully isolated deployment voltage regulators, using the external safing FETs as power elements in the regulator loop. Deployment voltage is set to a nominal 18V value to further optimize system cost.

Integrated safing logic uses a rolling average algorithm and decodes all sensor information within the system remote sensor SPI bus. Number of samples and thresholds are user-programmable. An alternative safing function permits arming from an external source through the Global SPI bus (E2E communication).

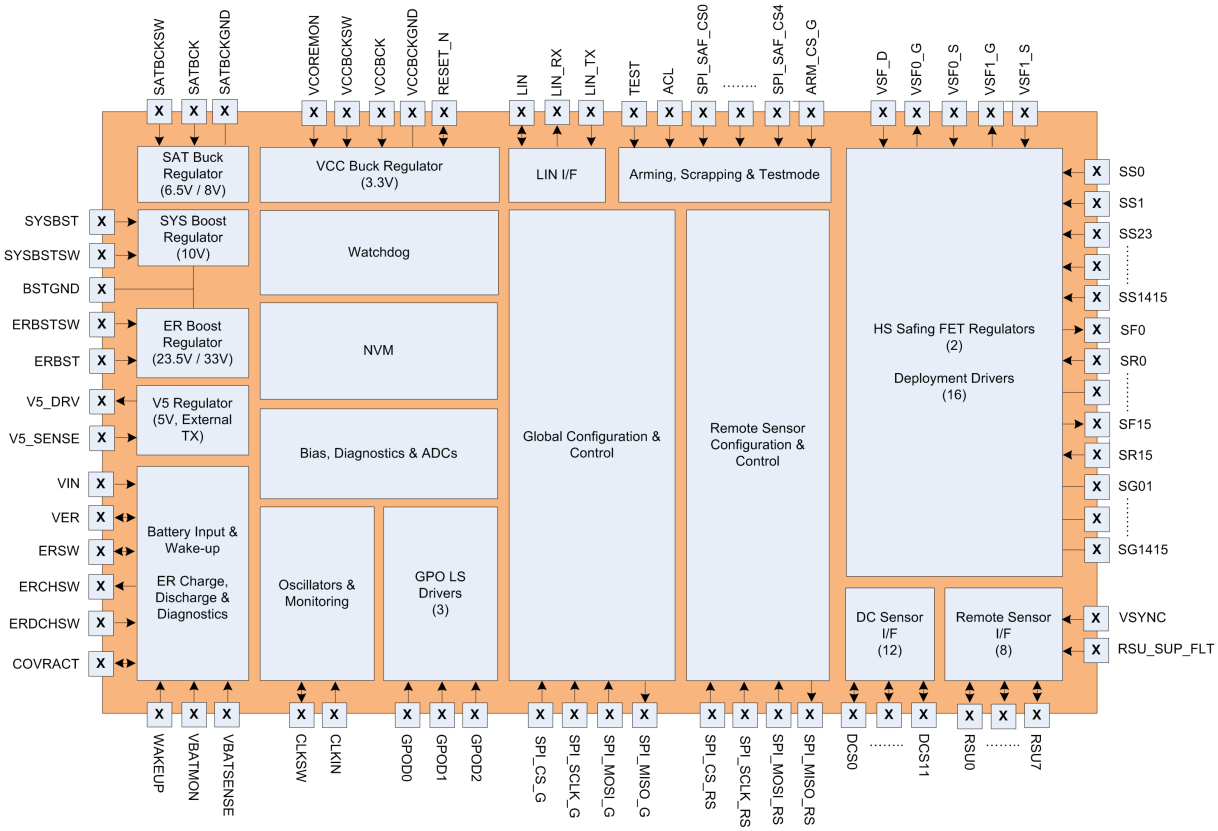
Dual SPI interfaces separate device global functions and remote sensors. LIN interface is available, providing OCS message decoding for passenger loop inhibition.

1 Block diagram and pin description

1.1 Block diagram

The L9691 IC is an application specific standard component for airbag system chip. Its main functions include power management, deployment drivers (supporting both squib and low-energy actuator loads), deployment voltage regulators, remote sensor interfaces (supporting PSI-5 satellite sensors), diagnostics, deployment arming, hall-effect/switch sensor interfaces, general purpose output low-side drivers, watchdog, LIN interface. A simplified block diagram for this IC is shown in the Figure 1.

Figure 1. Block diagram



1.2 Pin description

Figure 2. **Device pinout**

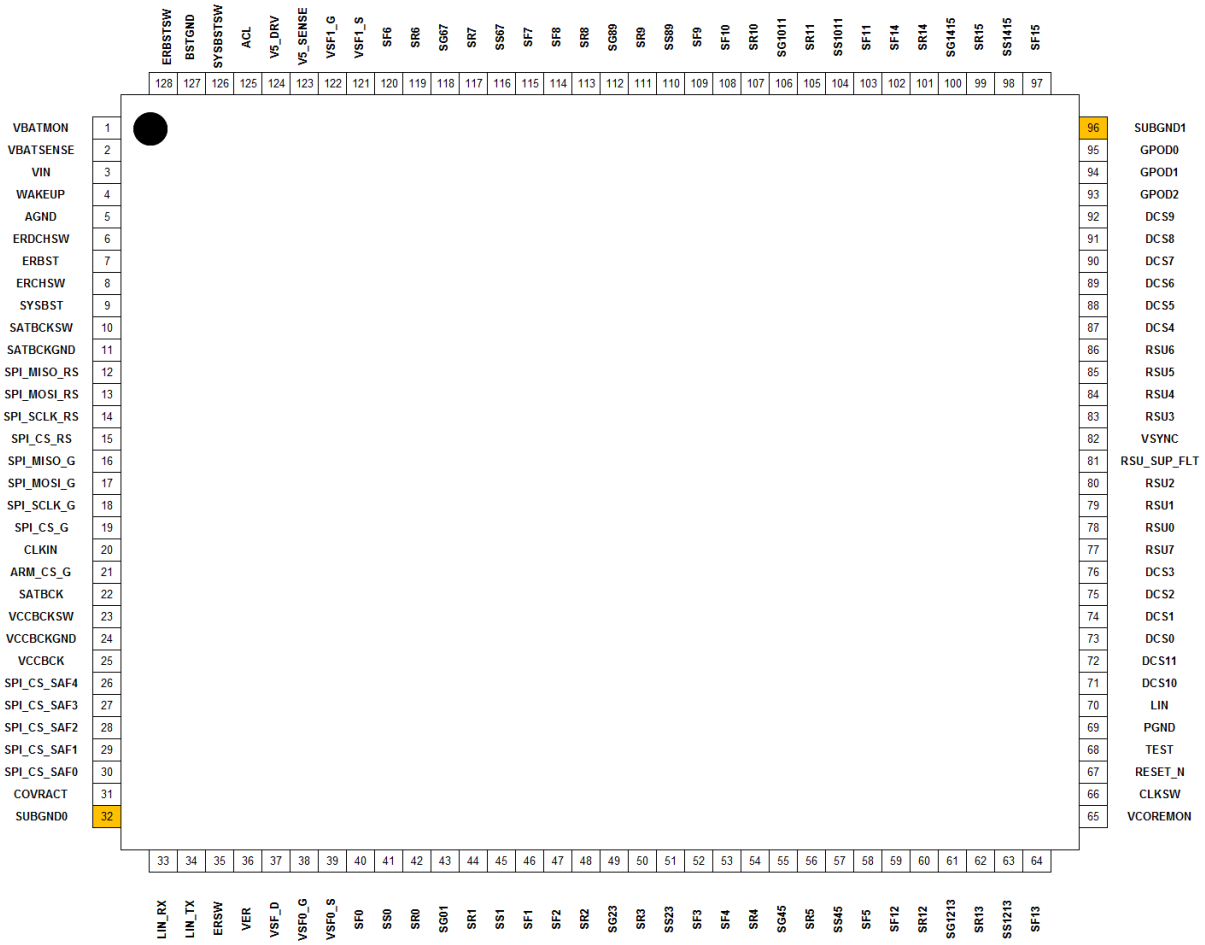


Table 1. **Pin function**

Pin #	Pin name	Description	I/O type	Class
1	VBATMON	Battery monitor for wake up	I	Global
2	VBATSENSE	Battery sense input	I	Global
3	VIN	Battery input voltage	S	Global
4	WAKEUP	Wake-up control input	I	Global
5	AGND	Analog ground	S	Local
6	ERDCHSW	Energy reserve discharge path	O	Local
7	ERBST	Energy reserve boost output voltage	S	Local
8	ERCHSW	Energy reserve charge path	O	Local
9	SYSBST	System boost output voltage	S	Local
10	SATBCKSW	Satellite buck switching output	O	Local
11	SATBCKGND	Satellite buck ground	S	Local
12	SPI_MISO_RS	Remote sensor SPI data out/snooping input	I/O	Local
13	SPI_MOSI_RS	Remote sensor SPI data in	I	Local

Pin #	Pin name	Description	I/O type	Class
14	SPI_SCLK_RS	Remote sensor SPI clock	I	Local
15	SPI_CS_RS	Remote sensor SPI chip select	I	Local
16	CLKIN	External clock input	I	Local
17	SPI_MOSI_G	Global SPI data in	I	Local
18	SPI_SCLK_G	Global SPI clock	I	Local
19	SPI_CS_G	Global SPI chip select	I	Local
20	SPI_MISO_G	Global SPI data out/snooping input	I/O	Local
21	ARM_CS_G	Arm status capture input (on global SPI)	I	Local
22	SATBCK	Satellite buck output voltage	S	Local
23	VCCBCKSW	VCC buck switching output	O	Local
24	VCCBCKGND	VCC buck ground	S	Local
25	VCCBCK	VCC buck output voltage	S	Local
26	SPI_CS_SAF4	SPI safing sensor chip select 4	I	Local
27	SPI_CS_SAF3	SPI safing sensor chip select 3	I	Local
28	SPI_CS_SAF2	SPI safing sensor chip select 2	I	Local
29	SPI_CS_SAF1	SPI safing sensor chip select 1	I	Local
30	SPI_CS_SAF0	SPI safing sensor chip select 0	I	Local
31	COVRACT	Crossover switch control input/output	I/O	Local
32	SUBGND0	Substrate ground 0 (fused with lead frame)	S	Local
33	LIN_RX	LIN bus receive data out	I/O	Local
34	LIN_TX	LIN bus transmit data in	I	Local
35	VER	Energy reserve voltage	I	Local
36	ERSW	Energy reserve switch input/output	I/O	Local
37	VSF_D	Safing FET drain sense/force	O	Local
38	VSF0_G	Safing FET regulator 0 gate output	O	Local
39	VSF0_S	Safing FET regulator 0 source input	I	Local
40	SF0	Squib high-side channel 0	O	Global
41	SS0	Squib high-side supply channel 0	S	Local
42	SR0	Squib low-side channel 0	O	Global
43	SG01	Squib low-side ground channel 0 and 1	S	Local
44	SR1	Squib low-side channel 1	O	Global
45	SS1	Squib high-side supply channel 1	S	Local
46	SF1	Squib high-side channel 1	O	Global
47	SF2	Squib high-side channel 2	O	Global
48	SR2	Squib low-side channel 2	O	Global
49	SG23	Squib low-side ground channel 2 and 3	S	Local
50	SR3	Squib low-side channel 3	O	Global
51	SS23	Squib high-side supply channel 2 and 3	S	Local
52	SF3	Squib high-side channel 3	O	Global
53	SF4	Squib high-side channel 4	O	Global
54	SR4	Squib low-side channel 4	O	Global

Pin #	Pin name	Description	I/O type	Class
55	SG45	Squib low-side ground channel 4 and 5	S	Local
56	SR5	Squib low-side channel 5	O	Global
57	SS45	Squib high-side supply channel 4 and 5	S	Local
58	SF5	Squib high-side channel 5	O	Global
59	SF12	Squib high-side channel 12	O	Global
60	SR12	Squib low-side channel 12	O	Global
61	SG1213	Squib low-side ground channel 12 and 13	S	Local
62	SR13	Squib low-side channel 13	O	Global
63	SS1213	Squib high-side supply channel 12 and 13	S	Local
64	SF13	Squib high-side channel 13	O	Global
65	VCOREMON	MCU core voltage monitoring input	I	Local
66	CLKSW	Switching regulator sync input/output	I/O	Local
67	RESET_N	Reset input/output	I/O	Local
68	TEST	Test-mode, watchdog disable input and ISRC check	I/O	Local
69	PGND	Power ground for LIN, GPOs and RSU	S	Local
70	LIN	LIN bus	I/O	Global
71	DCS10	DC sensor interface channel 10	O	Global
72	DCS11	DC sensor interface channel 11	O	Global
73	DCS0	DC sensor interface channel 0	O	Global
74	DCS1	DC sensor interface channel 1	O	Global
75	DCS2	DC sensor interface channel 2	O	Global
76	DCS3	DC sensor interface channel 3	O	Global
77	RSU7	Remote sensor interface channel 7	O	Global
78	RSU0	Remote sensor interface channel 0	O	Global
79	RSU1	Remote sensor interface channel 1	O	Global
80	RSU2	Remote sensor interface channel 2	O	Global
81	RSU_SUP_FLT	RSU filtered supply input	S	Local
82	VSYNC	RSU SYNC pulse supply input	S	Local
83	RSU3	Remote sensor interface channel 3	O	Global
84	RSU4	Remote sensor interface channel 4	O	Global
85	RSU5	Remote sensor interface channel 5	O	Global
86	RSU6	Remote sensor interface channel 6	O	Global
87	DCS4	DC sensor interface channel 4	O	Global
88	DCS5	DC sensor interface channel 5	O	Global
89	DCS6	DC sensor interface channel 6	O	Global
90	DCS7	DC sensor interface channel 7	O	Global
91	DCS8	DC sensor interface channel 8	O	Global
92	DCS9	DC sensor interface channel 9	O	Global
93	GPOD2	General purpose drain output channel 2	O	Global
94	GPOD1	General purpose drain output channel 1	O	Global
95	GPOD0	General purpose drain output channel 0	O	Global

Pin #	Pin name	Description	I/O type	Class
96	SUBGND1	Substrate ground 1 (fused with lead frame)	S	Local
97	SF15	Squib high-side channel 15	O	Global
98	SS1415	Squib high-side supply channel 14 and 15	S	Local
99	SR15	Squib low-side channel 15	O	Global
100	SG1415	Squib low-side ground channel 14 and 15	S	Local
101	SR14	Squib low-side channel 14	O	Global
102	SF14	Squib high-side channel 14	O	Global
103	SF11	Squib high-side channel 11	O	Global
104	SS1011	Squib high-side supply channel 10 and 11	S	Local
105	SR11	Squib low-side channel 11	O	Global
106	SG1011	Squib low-side ground channel 10 and 11	S	Local
107	SR10	Squib low-side channel 10	O	Global
108	SF10	Squib high-side channel 10	O	Global
109	SF9	Squib high-side channel 9	O	Global
110	SS89	Squib high-side supply channel 8 and 9	S	Local
111	SR9	Squib low-side channel 9	O	Global
112	SG89	Squib low-side ground channel 8 and 9	S	Local
113	SR8	Squib low-side channel 8	O	Global
114	SF8	Squib high-side channel 8	O	Global
115	SF7	Squib/LEA high-side channel 7	O	Global
116	SS67	Squib/LEA high-side supply channel 6 and 7	S	Local
117	SR7	Squib/LEA low-side channel 7	O	Global
118	SG67	Squib/LEA low-side ground channel 6 and 7	S	Local
119	SR6	Squib/LEA low-side channel 6	O	Global
120	SF6	Squib/LEA high-side channel 6	O	Global
121	VSF1_S	Safing FET regulator 1 source input	I	Local
122	VSF1_G	Safing FET regulator 1 gate output	O	Local
123	V5_SENSE	V5 regulator sense input	I	Local
124	V5_DRV	V5 regulator drive output	O	Local
125	ACL	End-of-life disposal control input	I	Global
126	SYSBSTSW	System boost switching output	O	Local
127	BSTGND	Boost regulator ground	S	Local
128	ERBSTSW	Energy reserve boost switching output	O	Local
-	Ex Pad Down	Substrate ground (backside)	S	Local

Legend: I = Input, O = Output, I/O = Input/Output, S = Supply or ground

2 Maximum ratings

2.1 Absolute maximum ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

All voltages are related to the potential at substrate ground (SUBGND0 and SUBGND1).

Table 2. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
VBATMON	Battery monitor for wake up	-18(1)	-	40	V
VBATSENSE	Battery sense input	-18(1)	-	40	V
VIN	Battery input voltage	-1(2)	-	40	V
WAKEUP	Wake-up control input	-1	-	40	V
ERDCHSW	Energy reserve discharge path	-0.3	-	40	V
ERCHSW	Energy reserve charge path	-0.3	-	40	V
ERBST	Energy reserve boost output voltage	-0.3	-	40	V
AGND	Analog ground	-0.3	-	0.3	V
SYSBST	System boost output voltage	-0.3	-	40	V
SATBCKSW	Satellite buck switching output	-0.3	-	40	V
SATBCKGND	Satellite buck ground	-0.3	-	0.3	V
SPI_MISO_RS	Remote sensor SPI data out/snooping input	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_MOSI_RS	Remote sensor SPI data in	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_SCLK_RS	Remote sensor SPI clock	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_CS_RS	Remote sensor SPI chip select	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_MISO_G	Global SPI data out/snooping input	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_MOSI_G	Global SPI data in	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_SCLK_G	Global SPI clock	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_CS_G	Global SPI chip select	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
CLKIN	External clock input	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
ARM_CS_G	Arm status capture input (on global SPI)	-0.3	-	20(3)	V
SATBCK	Satellite buck output voltage	-0.3	-	20	V
VCCBCKSW	VCC buck switching output	-0.3	-	20	V
VCCBCKGND	VCC buck ground	-0.3	-	0.3	V
VCCBCK	VCC buck output voltage	-0.3	-	4.6	V
SPI_CS_SAF4	SPI safing sensor chip select 4	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_CS_SAF3	SPI safing sensor chip select 3	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_CS_SAF2	SPI safing sensor chip select 2	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_CS_SAF1	SPI safing sensor chip select 1	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_CS_SAF0	SPI safing sensor chip select 0	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
COVRACT	Crossover switch control input/ouput	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SUBGND0	Substrate ground 0 (fused with lead frame)	-0.3	-	0.3	V
LIN_RX	LIN bus receive data out	-0.3	-	min (VCCBCK + 0.3, 4.6)	V

Symbol	Parameter	Min	Typ	Max	Unit
LIN_TX	LIN bus transmit data in	-0.3	-	40	V
ERSW	Crossover switch output	-0.3	-	40	V
VER	Energy reserve voltage	-0.3	-	40	V
VSF_D	Safing FET drain sense/force	-0.3	-	40	V
VSF0_G	Safing FET regulator 0 gate output	-0.3	-	40	V
VSF0_S	Safing FET regulator 0 source input	-0.3	-	40	V
SF0	Squib high-side channel 0	-1(4)	-	40	V
SS0	Squib high-side supply channel 0	-0.3	-	40	V
SR0	Squib low-side channel 0	-0.3	-	35	V
SG01	Squib low-side ground channel 0 and 1	-0.3	-	0.3	V
SR1	Squib low-side channel 1	-0.3	-	35	V
SS1	Squib high-side supply channel 1	-0.3	-	40	V
SF1	Squib high-side channel 1	-1(4)	-	40	V
SF2	Squib high-side channel 2	-1(4)	-	40	V
SR2	Squib low-side channel 2	-0.3	-	35	V
SG23	Squib low-side ground channel 2 and 3	-0.3	-	0.3	V
SR3	Squib low-side channel 3	-0.3	-	35	V
SS23	Squib high-side supply channel 2 and 3	-0.3	-	40	V
SF3	Squib high-side channel 3	-1(4)	-	40	V
SF4	Squib high-side channel 4	-1(4)	-	40	V
SR4	Squib low-side channel 4	-0.3	-	35	V
SG45	Squib low-side ground channel 4 and 5	-0.3	-	0.3	V
SR5	Squib low-side channel 5	-0.3	-	35	V
SS45	Squib high-side supply channel 4 and 5	-0.3	-	40	V
SF5	Squib high-side channel 5	-1(4)	-	40	V
SF6	Squib/LEA high-side channel 6	-1(4)	-	40	V
SR6	Squib/LEA low-side channel 6	-0.3	-	35	V
SG67	Squib/LEA low-side ground channel 6 and 7	-0.3	-	0.3	V
SR7	Squib/LEA low-side channel 7	-0.3	-	35	V
SS67	Squib/LEA high-side supply channel 6 and 7	-0.3	-	40	V
SF7	Squib/LEA high-side channel 7	-1(4)	-	40	V
VCOREMON	MCU core voltage monitoring input	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
CLKSW	Switching regulator sync input/output	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
RESET_N	Reset input/output	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
TEST	Test-mode, watchdog disable input and ISRC check	-0.3	-	40	V
PGND	Power ground for LIN, GPOs and RSU	-0.3	-	0.3	V
LIN	LIN bus	-27(5)	-	40	V
DCS0	DC sensor interface channel 0	-2	-	40	V
DCS1	DC sensor interface channel 1	-2	-	40	V
DCS2	DC sensor interface channel 2	-2	-	40	V
DCS3	DC sensor interface channel 3	-2	-	40	V

Symbol	Parameter	Min	Typ	Max	Unit
DCS4	DC sensor interface channel 4	-2	-	40	V
DCS5	DC sensor interface channel 5	-2	-	40	V
RSU0	Remote sensor interface channel 0	-1	-	40	V
RSU1	Remote sensor interface channel 1	-1	-	40	V
RSU2	Remote sensor interface channel 2	-1	-	40	V
RSU3	Remote sensor interface channel 3	-1	-	40	V
RSU_SUP_FLT	RSU filtered supply input	-0.3	-	40	V
VSYNC	RSU SYNC pulse supply input	-0.3	-	40	V
RSU4	Remote sensor interface channel 4	-1	-	40	V
RSU5	Remote sensor interface channel 5	-1	-	40	V
RSU6	Remote sensor interface channel 6	-1	-	40	V
RSU7	Remote sensor interface channel 7	-1	-	40	V
DCS6	DC sensor interface channel 6	-2	-	40	V
DCS7	DC sensor interface channel 7	-2	-	40	V
DCS8	DC sensor interface channel 8	-2	-	40	V
DCS9	DC sensor interface channel 9	-2	-	40	V
DCS10	DC sensor interface channel 10	-2	-	40	V
DCS11	DC sensor interface channel 11	-2	-	40	V
GPOD2	General purpose drain output channel 2	-1	-	40	V
GPOD1	General purpose drain output channel 1	-1	-	40	V
GPOD0	General purpose drain output channel 0	-1	-	40	V
SUBGND1	Substrate ground 1 (fused with lead frame)	-0.3	-	0.3	V
SF15	Squib high-side channel 15	-1[(4)]	-	40	V
SS1415	Squib high-side supply channel 14 and 15	-0.3	-	40	V
SR15	Squib low-side channel 15	-0.3	-	35	V
SG1415	Squib low-side ground channel 14 and 15	-0.3	-	0.3	V
SR14	Squib low-side channel 14	-0.3	-	35	V
SF14	Squib high-side channel 14	-1[(4)]	-	40	V
SF13	Squib high-side channel 13	-1[(4)]	-	40	V
SS1213	Squib high-side supply channel 12 and 13	-0.3	-	40	V
SR13	Squib low-side channel 13	-0.3	-	35	V
SG1213	Squib low-side ground channel 12 and 13	-0.3	-	0.3	V
SR12	Squib low-side channel 12	-0.3	-	35	V
SF12	Squib high-side channel 12	-1[(4)]	-	40	V
SF11	Squib high-side channel 11	-1[(4)]	-	40	V
SS1011	Squib high-side supply channel 10 and 11	-0.3	-	40	V
SR11	Squib low-side channel 11	-0.3	-	35	V
SG1011	Squib low-side ground channel 10 and 11	-0.3	-	0.3	V
SR10	Squib low-side channel 10	-0.3	-	35	V
SF10	Squib high-side channel 10	-1[(4)]	-	40	V
SF9	Squib high-side channel 9	-1[(4)]	-	40	V

Symbol	Parameter	Min	Typ	Max	Unit
SS89	Squib high-side supply channel 8 and 9	-0.3	-	40	V
SR9	Squib low-side channel 9	-0.3	-	35	V
SG89	Squib low-side ground channel 8 and 9	-0.3	-	0.3	V
SR8	Squib low-side channel 8	-0.3	-	35	V
SF8	Squib high-side channel 8	-1(4)	-	40	V
VSF1_S	Safing FET regulator 1 source input	-0.3	-	40	V
VSF1_G	Safing FET regulator 1 gate output	-0.3	-	40	V
V5_SENSE	V5 regulator sense input	-0.3	-	40	V
V5_DRV	V5 regulator drive output	-0.3	-	40	V
ACL	End-of-life disposal control input	-0.3	-	40(6)	V
SYSBSTSW	System boost switching output	-0.3	-	40	V
BSTGND	Boost regulator ground	-0.3	-	0.3	V
ERBSTSW	Energy reserve boost switching output	-0.3	-	40	V
Ex Pad Down	Substrate ground (backside)	-0.3	-	0.3	V

1. *Or 20 mA for 10 ms during transient.*
2. *Valid in transient conditions only.*
3. *Set at 20 V for pin FMEA constraints.*
4. *In the case of deployment turn off the transient voltages on SS and SF pins can move away from each other until a maximum voltage of SS-SF < 45 V for a limited transient time (6.5 µs maximum) with no damage on device. Additionally in this time transient, in worst case load condition (maximum load inductance 56 µH) the peak energy that can be handled by the ESD protection on SF pin is 128 µJ within a maximum time of 6.5 µs.*
5. *Valid for T_J > 27 deg, otherwise -18 V.*
6. *Set at 40 V for pin FMEA constraints.*

Table 3. ESD protection

Symbol	Parameter	Min	Typ	Max	Unit
All pins	HBM	-2	-	2	kV
All pins	CDM (values for corner pins in brackets)	-500/(-750)	-	500/(750)	V
Global pins (except LIN)	HBM	-4	-	4	kV
LIN pin	HBM	-6	-	6	kV

2.2 Temperature ranges and thermal data

Table 4. Temperature ranges and thermal data

Symbol	Parameter	Min	Max	Unit
T_{AMB}	Operating temperature (ECU environment)	-40	105	°C
T_J	Operating junction temperature	-40	175	°C
T_{STG}	Storage temperature	-55	150	°C
$R_{TH\_J\_CASE}$	Thermal resistance junction to case	-	2	°C/W

3 Device overview

3.1 Main features

- Capability to operate in dual-chip mode in master/slave configuration, user-selectable via NVM programming
- Internal 16 MHz oscillator for timing generation
- Internal 10 MHz oscillator for monitoring
- Dedicated CLKIN pin to provide an external 4 MHz clock, 1% accurate, to improve timing accuracy (by FLL circuitry)
- Dedicated CLKSW pin to optimize switching regulator operation phases between master and slave devices (output when master, input when slave)
- Phase configuration for switching regulators time base, user-programmable via Global SPI
- Integrated temporal watchdog control
- RESET_N reset input/output pin (output with pull-up and pull-down capability when master, input with pull-down capability when slave)
- Internal NVM, used for trimming and device configuration, user-programmable via Global SPI

3.2 SPI interface

- One dedicated 32-bit SPI bus for global configuration and control
- One dedicated 32-bit SPI bus for remote sensor configuration and control, SafeSPI v1.0 compatible

3.3 Power supply and energy reserve management

- Integrated 2 MHz SYS boost regulator, 10 V ±8% nominal output
- Integrated 2 MHz energy reserve boost regulator, 33 V ±6% or 23.5 V ±6% nominal output, user-selectable via Global SPI
- Integrated energy reserve capacitor charge current-limited switch
- Integrated energy reserve capacitor discharge overcurrent-protected switch
- Integrated energy reserve crossover current-limited switch
- Crossover switch “active” signal (output when master, input when slave)
- Integrated 2 MHz synchronous SAT buck regulator, 8 V ±4% or 6.5 V ±4% nominal output, user-selectable via NVM programming
- Integrated 2 MHz synchronous VCC buck regulator, 3.3 V ±3% nominal output; 50% fixed duty-cycle mode (FDM), selectable via NVM programming
- External microcontroller core supply voltage monitoring (VCOREMON), user-selectable via NVM programming
- V5 linear regulator with external power PNP transistor, 5 V ±5% nominal output; possibility to disable via NVM programming
- Switching frequency selection via Global SPI
- Over and undervoltage status monitorings
- Open feedback diagnostic on VCC buck and V5 linear regulators
- Switching regulator ground loss detection and shutdown
- Boost external diode loss detection and voltage clamping
- Overtemperature detection and shutdown on all switching regulators, ER crossover switch and ER charge switch
- Energy reserve diagnostics, capacitor value and ESR

3.4 Safing FET regulator and diagnostics

- Dual integrated 18 V linear regulators for high-side safing FET source voltage, enabled via arming logic
- Safing FET connection integrity diagnostics
- Battery and energy reserve diode integrity diagnostics

3.5 Deployment drivers and diagnostics

- 16 high-side deployment drivers, 16 low side deployment drivers
- Low-energy actuator (LEA) support available on 2 channels (6 and 7)
- Common-return (CSRx) connection support available on 2 channel couples (2-3 and 4-5)
- Independently controlled high-side and low-side FETs
- User-programmable deployment options
  - Low current: 1.21 A minimum
  - High current: 1.76 A minimum
  - Programmable dwell time in 16 µs increments
  - Automatic dynamic deployment current profile
- Configurable deployment current monitor feature
- Deployment interruption in case of high-side short to ground and/or supply overvoltage
- Squib/LEA resistance measurement
- High and low-side FET tests
- Open and shorts diagnostics, including between loop drivers
- LEA diode presence/integrity diagnostics

3.6 Remote sensor interfaces

- 8 channel receiver, PSI-5 v2.3 compatible with SYNC pulse
- Dedicated supply input pins for both satellite and SYNC pulse operation
- Current limit with short circuit protection diagnostics
- Auto-adjusting current trip points for each channel
- Satellite data with parity and CRC, 10 bit, 16 bit and 20 bit messages, 125 k or 189 kbps
- Satellite message error detection

3.7 DC sensor interfaces

- 12 integrated interfaces with current sense capability
- Compatible with Hall-effect, resistive and switch sensors
- Capability to perform 2 simultaneous measurements on two different channels (0-1-2-3-10-11 and 4-5-6-7-8-9 grouping)
- Current limit protected output
- Capability to inhibit passenger airbag loops via monitoring of 2 DC sensor channels (0 and 1)

3.8 General purpose low-side outputs

- 3 low-side drivers
- ON-OFF mode and PWM 0-100% fine control
- Diagnostics for short circuit protection and open load detection
- Current limit protected

3.9 Arming/Passenger inhibit logic

- User-configurable safing algorithms with 22 safing records
- 5 independent chip-select inputs for external sensor interface SPI snooping
- Independent chip-select input for master/slave device arming status SPI snooping (in master/slave configuration)
- Independent user-programmable thresholds
- Independent user-programmable latch timers
- 8 discrete and independent internal arming signals
- 8 discrete and independent arming result outputs
- Passenger loop inhibition via internal monitoring of DC sensors and LIN OCS communication
- Capability to snoop master/slave device passenger inhibit status on global SPI (in master/slave configuration)
- Capability to snoop alternative microcontroller passenger inhibit status on global SPI
- Capability to receive arming request from global SPI communication using E2E protocol
- End-of-Life interface

3.10 LIN interface and decoder

- LIN specification v2.2A compliance and K-LINE ISO9141 compatibility
- Configurable integrated communication decoder for OCS message monitoring and passenger airbag loop inhibition

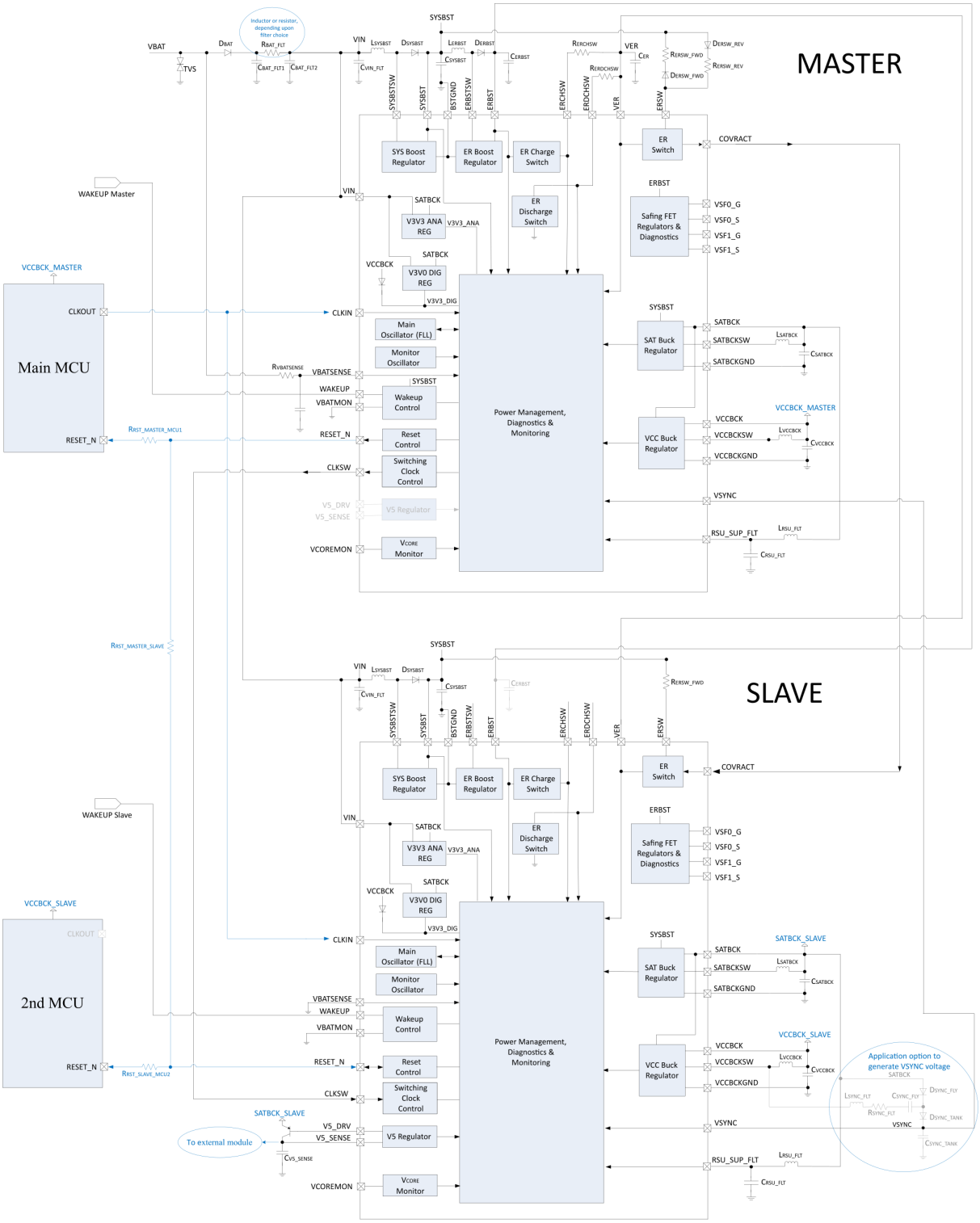
3.11 A/D converters

- One A/D converter dedicated to power-supply voltage and die average temperature monitoring, providing a 10 bit conversion via Global SPI and with the capability to handle a queue of 4 conversion requests
- 2 A/D converters used to perform ER capacitor value (14 bit conversion, Global SPI) and ESR (13 bit conversion, Global SPI) measurement diagnostic
- One A/D converter dedicated to deployment and safing FET regulator circuitry voltage monitoring, providing a 10 bit conversion via Global SPI and with the capability to handle one conversion request per time
- One A/D converter dedicated to deployment leakage current diagnostic, providing a 10 bit conversion of the measured leakage current via Global SPI; this current A/D converter is shared among all 16 deployment channels
- 8 A/D converters dedicated to remote sensor interfaces, providing a 10 bit conversion of the sensor current value and used for sensor communication decoding; each RSU channel have a dedicated current A/D converter
- 2 A/D converters dedicated to DC sensor interfaces, one providing the voltage value (10 bit conversion) and the other one providing the current value (10 bit conversion); the 2 A/D converters are shared among all 12 DC sensor channels. Conversions are provided via Global SPI, with the capability to handle a queue of 4 conversion requests; channel 0 and 1 voltage/current conversions can also be used internally by the passenger airbag inhibit feature

4 Applicative circuit

An example of a dual chip/master-slave application scenario is shown in Figure 3, in which two microcontrollers are present, one connected to the master (primary micro) and one to the slave (secondary).

Figure 3. Example of dual chip/master-slave scenario



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 TQFP128 (14X14X1.0 mm, 8.0x8.0 mm exp. pad down) package information

Figure 4. TQFP128 (14X14X1.0 mm, 8.0x8.0 mm exp. pad down) package outline

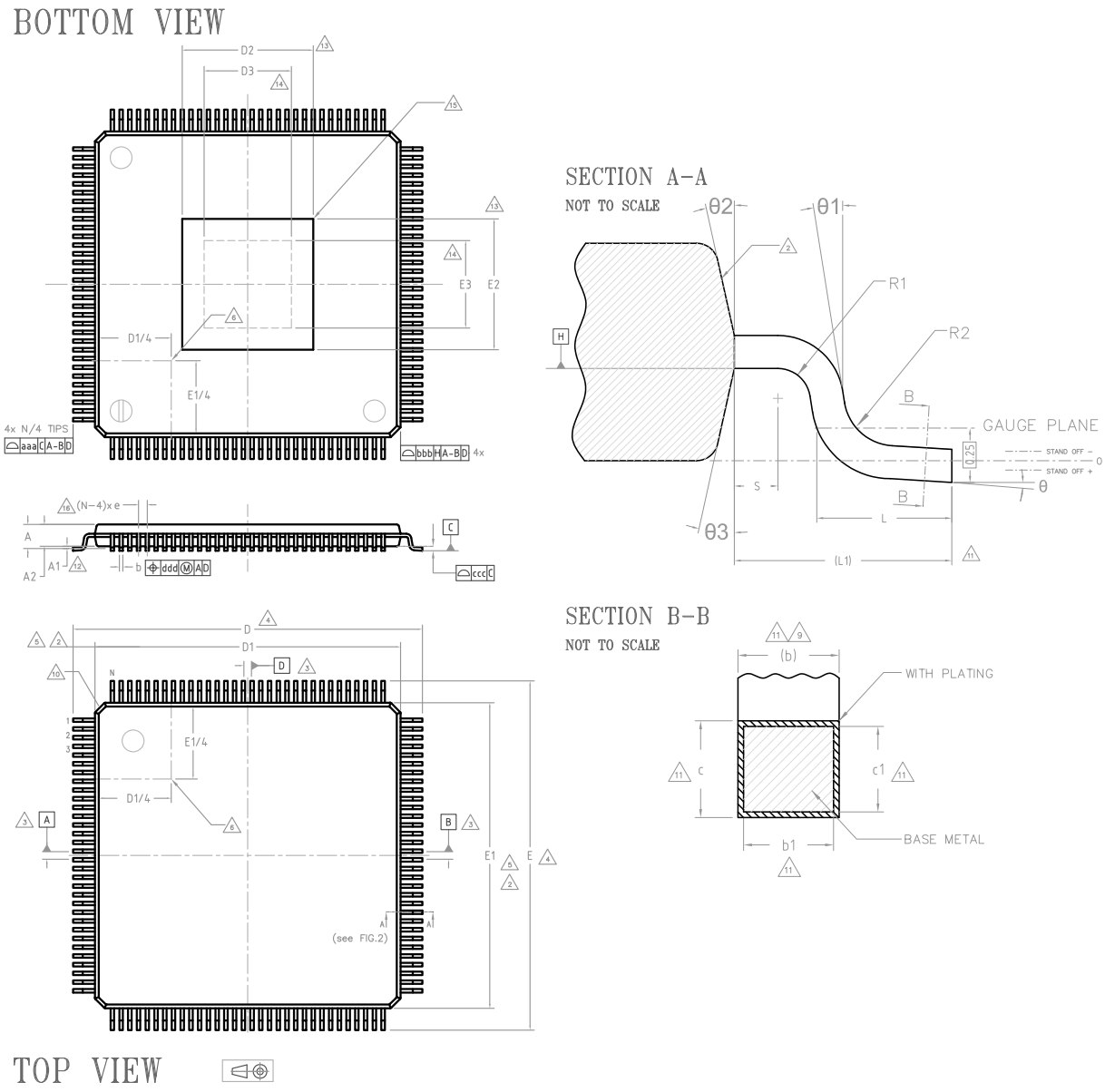


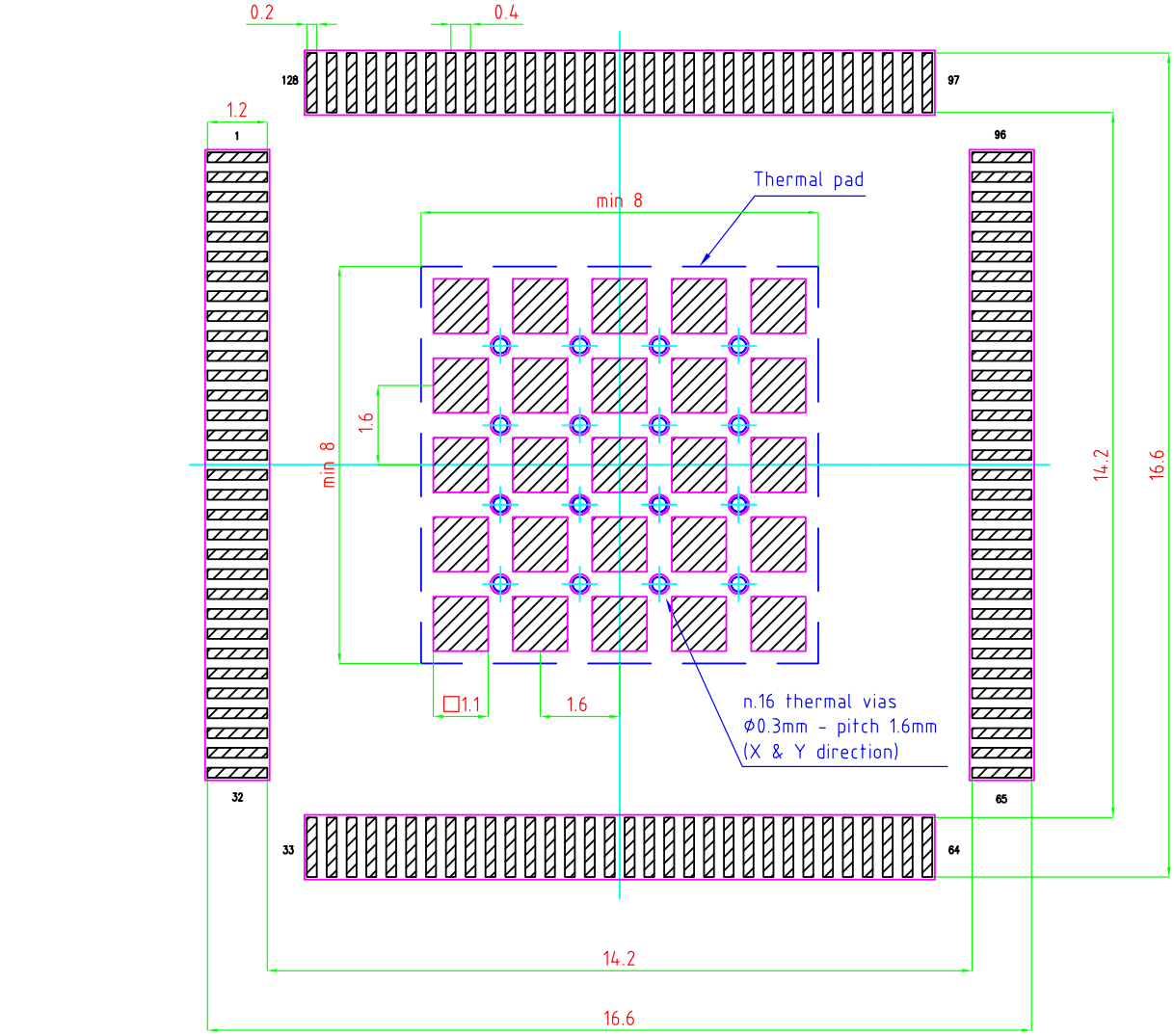
Table 5. TQFP128 (14X14X1.0 mm, 8.0x8.0 mm exp. pad down) package mechanical data

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
Θ	0°	3.5°	7°
Θ1	0°	-	-

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
Θ2	11°	12°	13°
Θ3	11°	12°	13°
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
c	0.09	-	0.20
c1	0.09	-	0.16
D	16.00 BSC		
D1	14.00 BSC		
D2(1)	-	-	8.18
D3(2)	6.80	-	-
e	0.40 BSC		
E	16.00 BSC		
E1	14.00 BSC		
E2(1)	-	-	8.18
E3(2)	6.80	-	-
L	0.45	0.60	0.75
L1	1.00 REF		
N	128		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
Tolerance of form and position			
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.07		

1. *Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. End user should verify D2 and E2 dimensions according to specific device application.*
2. *Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.*

Figure 5. TQFP128 (14X14X1.0 mm, 8.0x8.0 mm exp. pad down) PCB footprint



NOTE:
This is a draft proposal only and it might be not in line with customer or pcb supplier design rules.

Revision history

Table 6. **Document revision history**

Date	Version	Changes
09-Aug-2022	1	Initial release.
06-Sep-2022	2	Updated title in cover page.

Contents

List of tables

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