

Automotive 8-channel LS driver



TFQFN24 4x4x0.9

Product status link L9800

| Product summary | | | | |
|-----------------|-----------------|--|--|--|
| Order code | L9800 | | | |
| Package | TFQFN24 4x4x0.9 | | | |
| Packing | Tray | | | |
| Order code | L9800-TR | | | |
| Package | TFQFN24 4x4x0.9 | | | |
| Packing | Tape and reel | | | |

Features

| Symbol | Parameter | Values |
|----------------------|---|----------------------------------|
| V _{BATT} | Supply voltage | 3 V to 28 V |
| V _{DDIO} | Supply and SO buffer voltage | 3 V to 5.5 V |
| R _{DS(ON)} | Maximum on-state resistance at T _J = 150 °C | 1.7 Ω |
| I _{L(NOM)} | Nominal load current (T _A = 85 °C, all channels) | 330 mA |
| E _{AR} | Maximum energy dissipation - repetitive | 10 mJ at I _L = 220 mA |
| V _{DS(CL)} | Minimum drain-source clamping voltage | 42 V |
| I _{L(OVL0)} | Maximum overload switch OFF threshold | 3 A |
| f _{SCLK} | Maximum SPI clock frequency | 8 MHz |

- AEC-Q100 qualified
- Full ISO26262 compliant, ASIL-B systems ready
- General
 - Eight LS drivers
 - 16-bit SPI interface for outputs control and for diagnosis data communication
 - Daisy chain compatible and available even with 8-bit SPI
 - 2 parallel input pins with input mapping functionality
 - Cranking capability down to V_{BATT} = 3 V
 - Digital supply voltage range compatible with 3.3 V and 5 V MCU
 - LFD mode
 - Bulb inrush mode (BIM) with two channels in parallel mode and enhanced capacitive loads driving capability to drive 2 W lamps, 5 W lamps and electronic loads
 - Two independent internal PWM generators for MCU offloads and to drive LEDs
 - Very low quiescent current (with usage of IDLE pin)
 - Limp-home mode (with usage of IDLE and IN pins)
 - Safety features
 - Temperature sensor and monitoring
 - Serial communications using address feedback, 1 parity bit, frame counter and short frame detection
 - Fail-safe activation via input pins
 - Safe operation at low battery voltage (cranking)
- · Protective functions
 - Overcurrent latch OFF
 - Lower supply voltage range for extended operation
 - Electrostatic discharge (ESD) protection
 - Reverse battery protection on VBATT without external components
 - Short circuit battery protection
 - Thermal shutdown latch OFF



- · Diagnostic features
 - Latched diagnostic information via SPI register
 - Overcurrent and overtemperature detection at ON state
 - OFF state diagnosis, able to detect and distinguish open load and short to GND conditions

Applications

- Low-side switches for 12 V in automotive or industrial applications such as lighting, heating, motor driving, energy and power distribution
- Especially designed for driving relays, LEDs and motors

Description

The L9800 is an 8-channel LS driver designed for automotive applications (LEDs and relays) and compatible with resistive, inductive and capacitive loads. The device offers advanced diagnostic and protection functionalities such as open load, overcurrent and overtemperature detections, short to GND. The eight output channels can be driven by SPI or by dedicated parallel inputs. Limp-home functionality is present. Daisy chain available (no constraint on SPI number of bits of devices in chain). The device is able to guarantee cranking scenario down to $V_{\rm BATT} = 3 \, V$ and ensures very low-quiescent current under RESET.

The device is an 8-channel low-side power switch in a TFQFN24 4x4x0.9 package providing embedded protective functions. It is specially designed to control relays and LEDs in automotive and industrial applications.

A serial peripheral interface (SPI) is used for control and diagnosis of the loads as well as of the device. For direct control and PWM there are two input pins (IN0 and IN1) available, connected to two outputs by default (OUT2 and OUT3). Additional or different outputs can be controlled by the same input pins if programmed by SPI.

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Block diagram and pin description

L9800 OUT0D Power supply VBATT OUT1D VDDIO OUT2D GND OUT3D OUT4D OUT5D NCS OUT6D CLK OUT7D SI SO Ch_0 Ch_1 Ch_2 Ch_3 Ch_4 IDLE Ch_5 IN0 Ch_6 Logic IN1 Ch_7 **NRES** OUT07S DIS OUT56S OUT34S OUT12S

Figure 1. Block diagram

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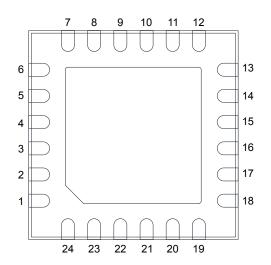


Figure 2. Pin configuration (bottom view)

Table 1. Pin description

| Pin# | Pin name | Description | I/O type |
|------|----------|--------------------------|----------|
| 1 | OUT7D | Drain 7 | 0 |
| 2 | OUT6D | Drain 6 | 0 |
| 3 | OUT56S | Source 5–6 | 0 |
| 4 | OUT5D | Drain 5 | 0 |
| 5 | NRES | NRES function | 1 |
| 6 | IN1 | Parallel command input 1 | I |
| 7 | IN0 | Parallel command input 2 | I |
| 8 | GND | Ground pin | |
| 9 | IDLE | Idle function | I |
| 10 | VDDIO | IO supply | |
| 11 | SO | SPI output stream | 0 |
| 12 | CLK | SPI clock | I |
| 13 | NCS | SPI chip select | I |
| 14 | SI | SPI input stream | I |
| 15 | OUT4D | Drain 4 | 0 |
| 16 | OUT34S | Source 4 | 0 |
| 17 | OUT3D | Drain 3 | 0 |
| 18 | DIS | Channel disable | I |
| 19 | OUT2D | Drain 2 | 0 |
| 20 | OUT12S | Source 1–2 | 0 |
| 21 | OUT1D | Drain 1 | 0 |
| 22 | VBATT | Battery voltage | |
| 23 | OUT07S | Source 0–7 | 0 |
| 24 | OUT0D | Drain 0 | 0 |

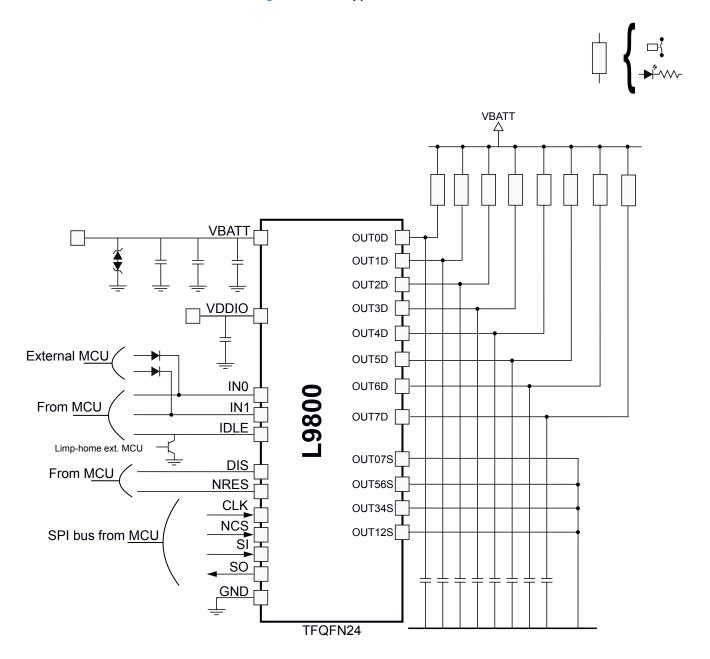
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2 Application circuit

Here below a general application circuit with the TFQFN24 package.

Figure 3. L9800 application circuit



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Table 2. External components list

| Pin | External components | | | | | Requirement ⁽¹⁾ | Comment | | | | | | |
|---------------|---------------------|------|------|------|------|----------------------------|--|--|--|----|--|----|---|
| PIII | Туре | Min. | Тур. | Max. | Unit | Requirement | Comment | | | | | | |
| | Capacitor | | 120 | | nF | 2., 3. | Tolerance ±20% 50 V | | | | | | |
| | Capacitor | | 100 | | μF | 2. | 50 V, Transient and load dump protection | | | | | | |
| VBATT | TVS | -15 | | 38 | V | 4. | Transient voltage suppressor | | | | | | |
| | Capacitor | | 10 | | μF | 2., 3. | Tolerance ±20% | | | | | | |
| | | | 10 | | | | 50 V, Transient and load dump protection | | | | | | |
| VDDIO | Capacitor | | 100 | | nF | 2. | Tolerance ±10% 50 V | | | | | | |
| OUT2D-OUT7D | Capacitor | | | | | | | | | 12 | | 3. | Maximum total capacitance value at output load (channel configured as low side) |
| OUT0D-OUT7D | | 47 | | | nF | nF | 4. | Minimum capacitance value at load supply (channel configured as high side, DRAIN0 and DRAIN1 if available) | | | | | |
| OUT07S-OUT12S | Capacitor | | | 12 | nF | 3. | Maximum total capacitance value as output load (channel configured as high side) | | | | | | |

^{1.} Refer to the following Items.

In the list of external components, the different parts are marked following the items reported below:

- 1. Mandatory components for L9800 functionality.
- 2. Recommended components for EMC robustness.
- 3. Recommended components for ESD trials.
- 4. Recommended system component.

Note:

Recommended components may depend on the requirements at system level and shall be confirmed by specific tests on the final applications.

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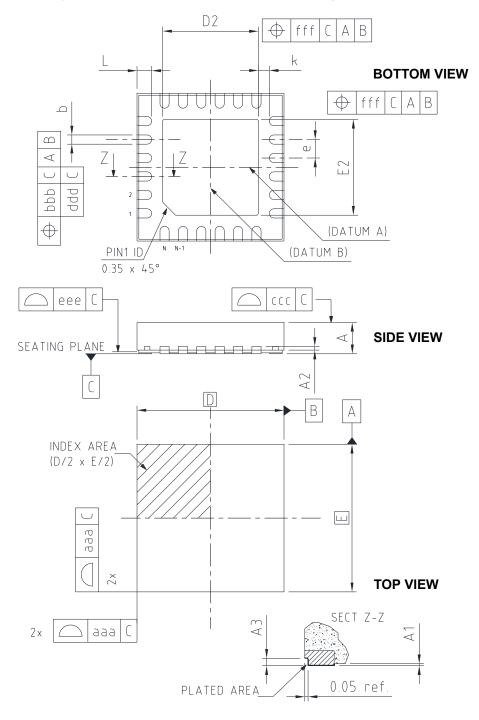


3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 TFQFN24 4x4x0.9 wettable flanks package information

Figure 4. TFQFN24 4x4x0.9 wettable flanks package dimension



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Table 3. TFQFN24 4x4x0.9 wettable flanks mechanical data

| Symbol | | Dimensions | | | | |
|--------|----------|-------------------------|------|----------|--|--|
| | Min. | Тур. | Max. | Note | | |
| А | 0.80 | 0.90 | 1.00 | (1) | | |
| A1 | 0.00 | 0.02 | 0.05 | (2) | | |
| A2 | | 0.20 REF | | | | |
| A3 | 0.1 | | | | | |
| b | 0.20 | 0.25 | 0.30 | (1), (3) | | |
| D | | 4.00 | | | | |
| D2 | 2.75 | 2.80 | 2.85 | | | |
| е | | 0.50 | | | | |
| E | | 4.00 | | | | |
| E2 | 2.75 | 2.80 | 2.85 | | | |
| L | 0.35 | 0.40 | 0.45 | (1) | | |
| k | 0.25 | | | | | |
| N | | 24 | | | | |
| | Tolerand | ce of form and position | | | | |
| aaa | | 0.15 | | | | |
| bbb | | 0.10 | | | | |
| ccc | | 0.08 | | | | |
| ddd | | 0.05 | | | | |
| eee | | 0.10 | | | | |

- 1. To be determined at setting datum plane C.
- 2. A1 is defined as the distance from the seating plane to the lowest point on the package body.
- 3. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
- 4. "N" is the maximum number of terminal positions for the specified body size.
- 5. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.

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Revision history

Table 4. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 04-May-2022 | 1 | Initial release. |
| | | Removed "ST Restricted" watermark. |
| 09-Nov-2023 | 2 | Updated Device summary, Features and Description on cover page. |
| | | Updated Section 2 Application circuit. |

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