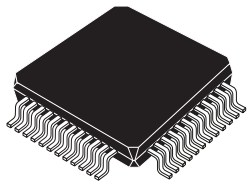
L9908

Data brief

Automotive 3-Phase motor gate driver unit



TQFP48 (exposed pad down)

Product status link
L9908

Product summary		
Order code	Package	Packing
L9908	TQFP48 (exp. pad down)	Tray
L9908-TR		Tape&Reel

Features

- AEC-Q100 qualified
- Full ISO26262 compliant, ASIL-D systems ready
- VDH motor supply voltage range from 4.5 V to 75 V for working in single (12 V systems), double (24 V systems) and 48 V battery applications
- 3.3 V internal supply voltage generated from 5 V on VDD pin
- Digital I/O compatible to 3.3 V/5 V logics
- 6 separate N-channel FET pre-drivers:
  - dedicated source connection to each FET
  - the device can withstand -14 V to 95 V on motor connection pins
  - 0% to 100% duty cycle operation support
  - dedicated PWM input pin for each gate driver
- 3 differential high accuracy current monitors for ground referred current measurements:
  - ADC/DAC architecture
  - SPI adjustable Gain Factor and Output Offset
  - built-in error calibration
  - the device can withstand -14 V to 6 V on input sensing pins
  - SPI readable current measurement
  - 0 to 4.6 V DAC output dynamic range
- 3 real time phase voltage monitor channels:
  - SPI programmable phase voltage feedback;
  - SPI readable phase duty cycle measurement;
- 32-bits - 10 MHz SPI interface with 5-bit CRC and 1bit frame counter for internal setting, self-test and full diagnostics
- Protection and diagnostic:
  - SPI programmable VDS diagnostic and protection in on state
  - SPI programmable Dead Time protection
  - SPI programmable Shoot-trough diagnostic and protection
  - Open load, short to GND and short to battery diagnostic in off state
  - Over-temperature diagnostic and protection with SPI programmable warning flag
  - SPI readable Tj measurement
  - Ground loss diagnostic
  - System clock monitoring
  - Power supply pins VDD, VDH, VBP over-voltage and under-voltage diagnostic
  - FET driver supply VPRE and VCP under-voltage and over-voltage diagnostic
  - SPI Window Watchdog
  - Fault status flag output

Application

- EPS – Electronic Power Steering
- HVAC Blowers – Heating, ventilation, and air conditioning
- Engine Cooling Fans
- Electronic Brake Booster
- EWP, EFP, EOP

Description

L9908 is a gate driver unit (GDU) for controlling 6 N-channel FETs for brushless motors in automotive applications.

Each one of the 3 half bridge drivers channels (HS/LS couples) can be independently configured allowing different load driving and is able to withstand -14 V to 95 V excursion on motor`s pins.

Through 6 dedicated parallel input the pre-driver stages can be controlled independently supporting duty cycle operations from 0% to 100% and allowing to implement all kinds of electric motor control strategy. A dedicated combination of regulators, charge pumps and bootstrap circuits allows L9908 to be suitable to operate in passenger, commercial or hybrid vehicles.

Safe operation of half bridges is ensured by shoot-trough diagnosis, dead-time, short to battery, short to ground and open load detection plus a real time phase voltage monitoring.

L9908 is equipped with 3 independent high accuracy current monitor channels with SPI-configurable input differential voltage ranges for ground referenced current measurements, with 5 V/3.3 V output dynamic range compatibility.

L9908 implements diagnostics on external and internal supply, ground level, internal temperature.

A 32-bit out of frame SPI-slave interface is implemented for communication up to 10 MHz between L9908 and uC. SPI communication is safe-guarded by 5-bit CRC, 1bit frame counter, frame length check and an SPI-configurable Window Watchdog.

1 Block diagram and pin description

Figure 1. **Block diagram**

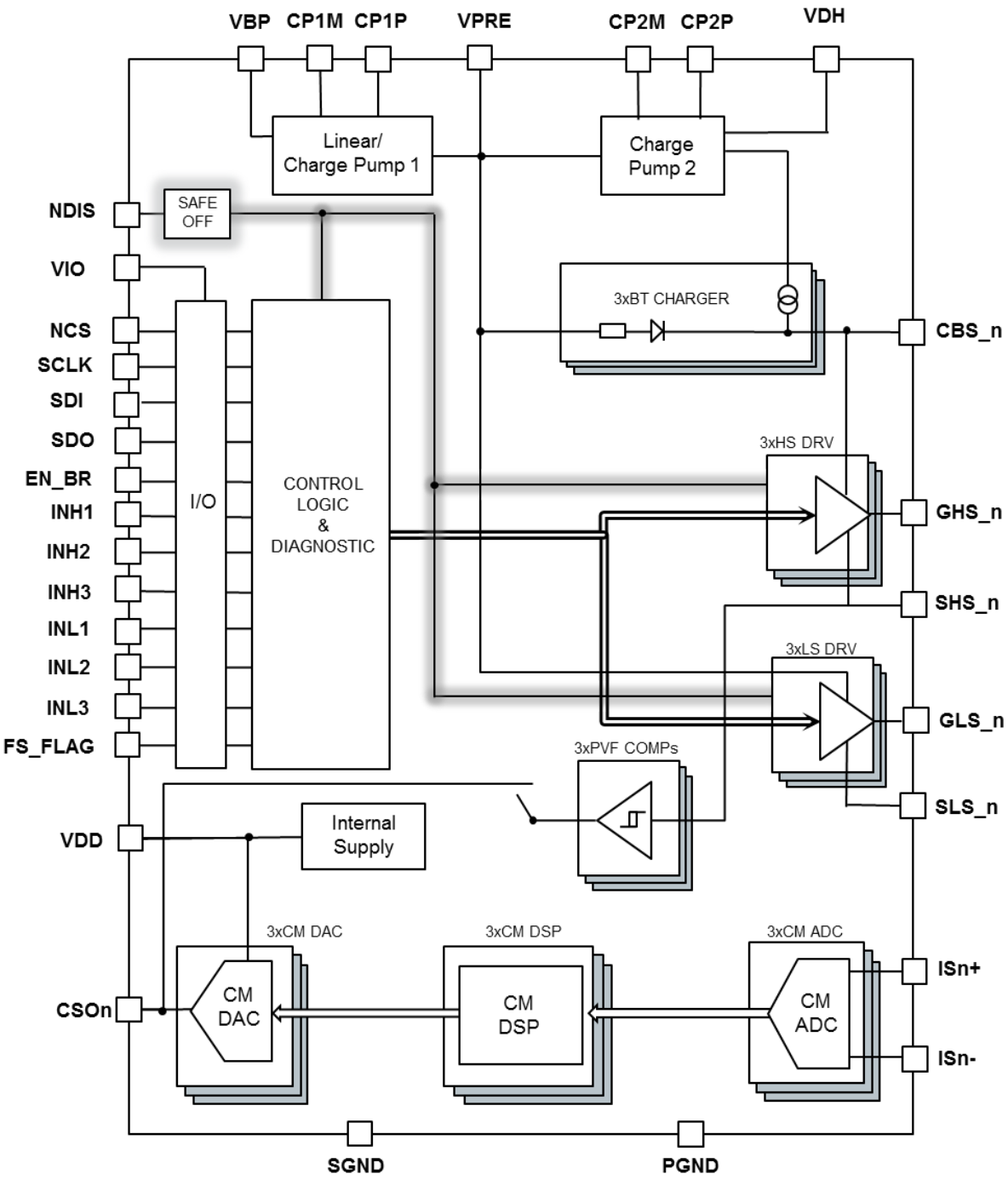
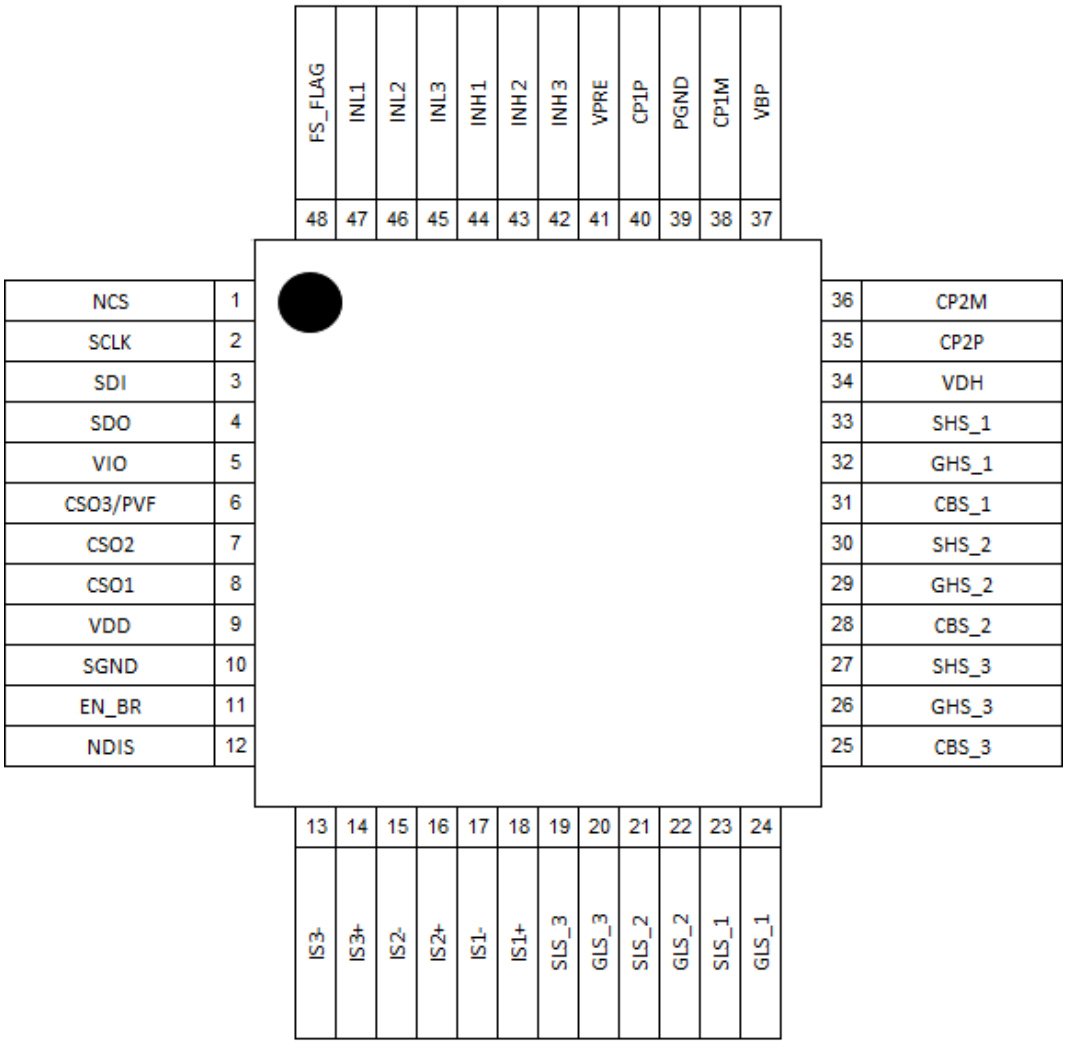


Figure 2. **Pin connection diagram (top view)**



Legenda: I = Input, O = Output, P = Power Supply, G = Ground, I/O = Input/Output

Table 1. **Pin list description**

Pin #	Pin name	Description	Pin type	Class
1	NCS	SPI Chip Select Input (Active LOW)	I	Local
2	SCLK	SPI Serial Clock Input	I	Local
3	SDI	SPI Serial Data Input	I	Local
4	SDO	SPI Serial Data Output	O	Local
5	VIO	Power supply for digital output	P	Local
6	CSO3/PVM	Current monitor 3 analog output. Phase voltage feedback output	O	Local
7	CSO2	Current monitor 2 analog output	O	Local
8	CSO1	Current monitor 1 analog output	O	Local
9	VDD	Power supply input for internal circuitry and current monitors analog output (CSOn)	P	Local
10	SGND	Signal Ground (Analog, Digital, Reference)	G	Local

Pin #	Pin name	Description	Pin type	Class
11	EN_BR	Bridge Enable Input (Active HIGH)	I	Local
12	NDIS	Safe switch-off activation Input (Active LOW)	I	Local
13	IS3-	Current monitor 3 negative input	I	Local
14	IS3+	Current monitor 3 positive input	I	Local
15	IS2-	Current monitor 2 negative input	I	Local
16	IS2+	Current monitor 2 positive input	I	Local
17	IS1-	Current monitor 1 negative input	I	Local
18	IS1+	Current monitor 1 positive input	I	Local
19	SLS_3	Source connection of LS FET, phase 3	I/O	Local
20	GLS_3	Gate connection of LS FET, phase 3	I/O	Local
21	SLS_2	Source connection of LS FET, phase 2	I/O	Local
22	GLS_2	Gate connection of LS FET, phase 2	I/O	Local
23	SLS_1	Source connection of LS FET, phase 1	I/O	Local
24	GLS_1	Gate connection of LS FET, phase 1	I/O	Local
25	CBS_3	Bootstrap capacitor of HS, phase 3	I/O	Local
26	GHS_3	Gate connection of HS FET, phase 3	I/O	Local
27	SHS_3	Source connection of HS FET, phase 3	I/O	Global
28	CBS_2	Bootstrap capacitor of HS, phase 2	I/O	Local
29	GHS_2	Gate connection of HS FET, phase 2	I/O	Local
30	SHS_2	Source connection of HS FET, phase 2	I/O	Global
31	CBS_1	Bootstrap capacitor of HS, phase 1	I/O	Local
32	GHS_1	Gate connection of HS FET, phase 1	I/O	Local
33	SHS_1	Source connection of HS FET, phase 1	I/O	Global
34	VDH	Drain connection of HS FETs	P	Global
35	CP2P	Charge Pump 2 positive input of fly capacitance	I/O	Local
36	CP2M	Charge Pump 2 negative input of fly capacitance	I/O	Local
37	VBP	Pre-regulation stage power supply	P	Global
38	CP1M	Charge Pump 1 negative input of fly capacitance	I/O	Local
39	PGND	Power Ground (Charge Pump 1 and 2)	G	Local
40	CP1P	Charge Pump 1 positive input of fly capacitance	I/O	Local
41	VPRE	Pre-regulated voltage for HS/LS Vgs driving	I/O	Local
42	INH3	PWM command for HS, phase 3 (Active HIGH)	I	Local
43	INH2	PWM command for HS, phase 2 (Active HIGH)	I	Local
44	INH1	PWM command for HS, phase 1 (Active HIGH)	I	Local
45	INL3	PWM command for LS, phase 3 (Active HIGH)	I	Local
46	INL2	PWM command for LS, phase 2 (Active HIGH)	I	Local
47	INL1	PWM command for LS, phase 1 (Active HIGH)	I	Local
48	FS_FLAG	Fault status flag output (Active LOW)	O	Local
	Exp. PAD	Cooling slug to be connected to GND plane		

2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 TQFP48 (7x7x1 mm exp. pad down) package information

Figure 3. TQFP48 (7x7x1 mm exp. pad down) package outline

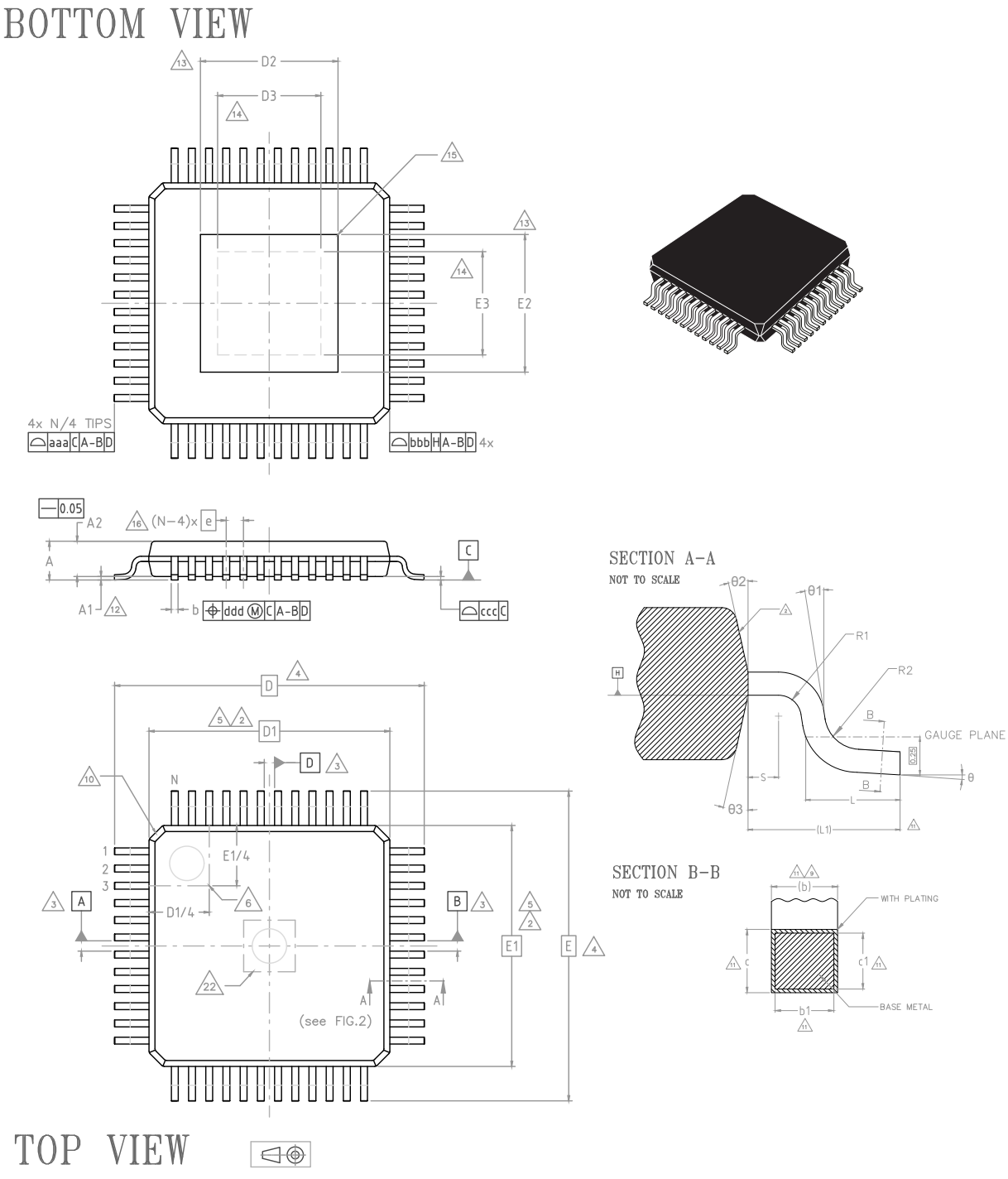


Table 2. **LQFP64 (10x10x1.4 mm exp. pad up) package mechanical data**

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
A	-	-	1.2
A1	0.04	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	-	0.20
D		9.00	
D1		7.00	
D2	-	-	4.15
D3	3.89	-	-
e	-	0.50	-
E		9.00	
E1		7.00	
E2	-	-	4.15
E3	3.89	-	-
L	0.45	0.60	0.75
L1		1.00	
N		48	
R1	0.08	-	-
R2	0.08	-	0.2
S	0.2	-	-
Tolerance of form and position			
aaa	-	0.2	-
bbb	-	0.2	-
ccc	-	0.08	-
ddd	-	0.08	-

Revision history

Table 3. **Document revision history**

Date	Version	Changes
03-Nov-2020	1	Initial release.

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