

## Automotive door actuator driver with embedded LIN

**Data brief** 



### **Features**



- 1 half bridge for 7.5 A load (R<sub>ON</sub> = 100 mΩ)
- 1 half bridge for 7.5 A load (R<sub>ON</sub> = 150 mΩ)
- 2 half bridges for 3 A load (R<sub>ON</sub> = 300 mΩ)
- 1 configurable high-side driver for up to 1.5 A (R<sub>ON</sub> = 500 mΩ) or 0.35 A (R<sub>ON</sub> = 1600 mΩ) load
- 1 configurable high-side driver for 0.8 A ( $R_{ON}$  = 800 m $\Omega$ ) or 0.35 A ( $R_{ON}$  = 1600 m $\Omega$ ) load
- 3 configurable high-side drivers for 0.15 A/0.35 A (R<sub>ON</sub> =2 Ω)
- 1 configurable high-side driver for 0.25 A/0.5 A (R<sub>ON</sub> = 2 Ω)
- 4 configurable high-side drivers for 0.15 A/0.25 A (R<sub>ON</sub> = 5 Ω)
- Internal 10bit PWM timer for each stand-alone high-side driver
- Buffered supply for voltage regulators and 2 high-side drivers (OUT15 & OUT\_HS / both P-channel) to supply e.g. external contacts
- Programmable soft-start function to drive loads with higher inrush currents as current limitation value (for OUT1-6, OUT7, OUT8 and OUT\_HS) with thermal expiration feature
- All the embedded outputs come with protection and supervision features:
  - Current Monitor (high-side only)
  - Open-load
  - Overcurrent
  - Thermal warning
  - Thermal shutdown

- Fully protected driver for external MOSFETs in H-bridge configuration
- Two 5 V voltage regulators for microcontroller and peripheral supply
- Programmable reset generator for power-on and undervoltage
- · Configurable window watchdog
- LIN 2.2a compliant (SAEJ2602 compatible) transceiver
- Separated (Isolated) fail-safe block with 2 LS (R<sub>ON</sub> = 1 Ω) to pull down the gates of the external HS MOSFETs
- Thermal clusters
- A/D conversion of supply voltages and internal temperature sensors
- Embedded and programmable VS duty cycle adjustment for LED driver outputs

## **Description**

The L99DZ120 is a door zone systems IC providing electronic control modules with enhanced power management power supply functionality, including various standby modes, as well as LIN physical communication layers.

The two low-drop voltage regulators of the devices supply the system microcontroller and external peripheral loads such as sensors and provide enhanced system standby functionality with programmable local and remote wake-up capability. In addition 8 high-side drivers to supply LEDs, 2 high-side drivers to supply bulbs increase the system integration level.

Up to 3 DC motors and 4 external MOS transistors in H-bridge configuration can be driven. All outputs are SC protected and implement an open-load diagnosis.

The ST standard SPI interface (4.0) allows control and diagnosis of the device and enables generic software development.

## 1 Block diagram and pin descriptions

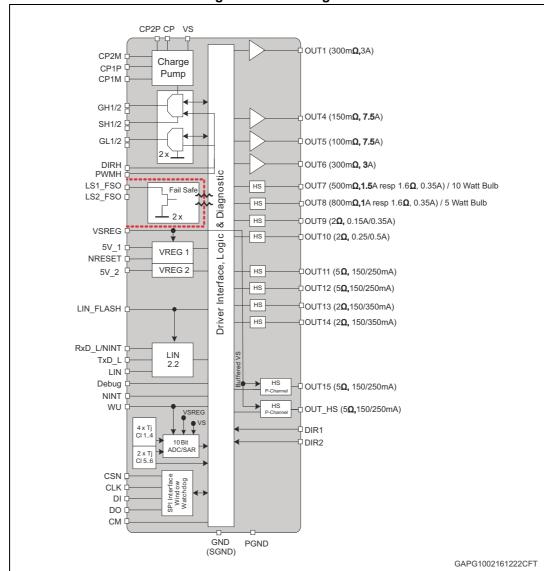


Figure 1. Block diagram

Table 1. Pin definitions and functions

Pin	Symbol	Function		
1	WU	Wake-up Input: Input pin for static or cyclic monitoring of external contacts		
2	CP2M	Charge pump pin for capacitor 2, negative side		
3	CP2P	Charge pump pin for capacitor 2, positive side		
4	СР	Charge pump output		
5	CP1P	Charge pump pin for capacitor 1, positive side		
6	CP1M	Charge pump pin for capacitor 1, negative side		



2/8 DocID029974 Rev 1

Table 1. Pin definitions and functions (continued)

Pin	Symbol	Function			
	-				
7	NC	Not connected			
8	NC	Not connected			
9	OUT14	High-side-driver output to drive LEDs			
10	OUT13	High-side-driver output to drive LEDs			
11	OUT12	High-side-driver output to drive LEDs			
12	OUT9	High-side-driver output to drive LEDs			
13	OUT10	High-side-driver-output			
14	OUT11	High-side-driver output to drive LEDs			
15	LS1_FSO	Fail Safe low-side switch (Active low)			
16	LS2_FSO	Fail Safe low-side switch (Active low)			
17	VS	Power supply voltage for power stage outputs (external reverse battery protection required), for this input a ceramic capacitor as close as possible to GND is recommended. Important: For the capability of driving, the full current at the outputs all pins of VS must be connected externally!			
18	VS; 2nd pin	Current capability (pin description see above)			
19	OUT7	High-side-driver output to drive LEDs or a 10 Watt bulb (programmable R <sub>dson</sub> )			
20	OUT6	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output)			
21	OUT1	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output)			
22	NC	Not connected			
23	OUT5	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to V <sub>S</sub> , low-side driver from GND to output)			
24	OUT5; 2nd pin	Current capability (pin description see above)			
25	$V_{SREG}$	Power supply voltage to supply the internal voltage regulators, OUT15 and the OUT_HS (external reverse battery protection required / Diode) for this input a ceramic capacitor as close as possible to GND and an electrolytic back up capacitor is recommended.			
26	OUT_HS	High-side-driver output to drive LEDs or to supply contacts			



Table 1. Pin definitions and functions (continued)

Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to V <sub>S</sub> , low-side driver from GND to output)  28 OUT4; 2 <sup>nd</sup> pin Current capability (pin description see above)  29 NC Not connected  30 VS; 3rd pin Current capability (for the pin description see above)  31 OUT15 High-side-driver output to drive LEDs  32 PGND Power GND  33 OUT8 High-side-driver output to drive LEDs or a 5 Watt bulb (programmable Rdson)  34 NC Not connected  35 SGND Signal Ground  Current monitor output: depending on the selected multiplexer bits CM_SEL_x (CR 7) of the; Control Register this output sources an image of the instant current; through the corresponding high-side driver with a fixed ratio  37 NC Not connected  38 CLK SPI: serial clock input  39 DO SPI: serial data output (push pull output stage)  40 DI SPI: serial data input  41 CSN SPI: chip select not input  42 TxD_L LIN Transmit data input	Pin	Symbol	Function		
which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to V <sub>S</sub> , low-side driver from GND to output)  28 OUT4; 2 <sup>nd</sup> pin Current capability (pin description see above)  29 NC Not connected  30 VS; 3rd pin Current capability (for the pin description see above)  31 OUT15 High-side-driver output to drive LEDs  32 PGND Power GND  33 OUT8 High-side-driver output to drive LEDs or a 5 Watt bulb (programmable R <sub>dson</sub> )  34 NC Not connected  35 SGND Signal Ground  36 CM CM_SEL_x (CR 7) of the; Control Register this output sources an image of the instant current; through the corresponding high-side driver with a fixed ratio  37 NC Not connected  38 CLK SPI: serial clock input  39 DO SPI: serial data output (push pull output stage)  40 DI SPI: serial data input  41 CSN SPI: chip select not input  42 TXD_L LIN Transmit data input  43 RXD_L/NINT RXD_L SIN receive data output; NINT -> indicates local/remote wake-up events (push pull output stage)  44 LIN_FLASH LIN Flash Mode enable (former TXD_C pin, to guarantee family compatibility)  45 NC Not connected  46 DIR1 Direct Drive Input 1  47 PWMH PMHH input: this input signal can be used to control the H-bridge Gate Drivers.  48 DIRH Direct Drive Input 2  NRESET With Grain Connected to the output pin and internal pull up resistance to with drain connected to the output pin and internal pull up resistance to					
Not connected  Not connected  Not connected  Not connected  Not side driver output to drive LEDs  PGND  Power GND  Not connected  Not connected  Not connected  Not connected  Not connected  Not connected  Redson  Comparison of the instant current; through the corresponding high-side driver with a fixed ratio  Robert Serial data output (push pull output stage)  Not Selt Serial data input  Not Connected  Procedure of the serial data input  Not Connected  Not Connected Connected  Not Connected Connected  Not Connected	27	OUT4	which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to V <sub>S</sub> , low-side driver		
30    VS; 3rd pin	28	OUT4; 2 <sup>nd</sup> pin	Current capability (pin description see above)		
31 OUT15	29	NC	Not connected		
PGND   Power GND	30	VS; 3rd pin	Current capability (for the pin description see above)		
OUT8	31	OUT15	High-side-driver output to drive LEDs		
NC	32	PGND	Power GND		
SGND Signal Ground  Current monitor output: depending on the selected multiplexer bits CM_SEL_x (CR 7) of the; Control Register this output sources an image of the instant current; through the corresponding high-side driver with a fixed ratio  NC Not connected  SPI: serial clock input  DO SPI: serial data output (push pull output stage)  PI: serial data input  CSN SPI: chip select not input  TxD_L LIN Transmit data input  RxD_L/NINT RXDL -> LIN receive data output; NINT -> indicates local/remote wake-up events (push pull output stage)  LIN_FLASH LIN_FLASH Compatibility)  NC Not connected  DIR1 Direct Drive Input 1  PWMH PWMH input: this input signal can be used to control the H-bridge Gate Drivers.  DIR2 Direction Input: this input controls the H-bridge Drivers for the external MOSFETs  NRESET NRESET NRESET SIGNARD.	33	OUT8			
Current monitor output: depending on the selected multiplexer bits  CM_SEL_x (CR 7) of the; Control Register this output sources an image of the instant current; through the corresponding high-side driver with a fixed ratio  NC Not connected  CLK SPI: serial clock input  DO SPI: serial data output (push pull output stage)  PI: serial data input  CSN SPI: chip select not input  LIN_Transmit data input  RXD_L/NINT  RXDL -> LIN receive data output; NINT -> indicates local/remote wake-up events (push pull output stage)  LIN_FLASH  LIN_FLASH  LIN_FLASH  LIN_FLASH  CN Not connected  PWMH  DIRCI Direct Drive Input 1  PWMH  PWMH input: this input signal can be used to control the H-bridge Gate Drivers.  Direction Input: this input controls the H-bridge Drivers for the external MOSFETs  NRESET  NRESET  NRESET  NRESET  NRESET  Current monitor output: depending on the selected multiplexer bits  CM_SLATA (CR 7) of the; Control Register this output stage of the corresponding high-side driver with a fixed ratio of the instant current; through the corresponding high-side driver with a fixed ratio of the instant current; through the corresponding high-side driver with a fixed ratio of the instant current; through the corresponding high-side driver with a fixed ratio of the instant current; through the corresponding high-side driver with a fixed ratio of the instant current; through the corresponding high-side driver with a fixed ratio of the instant current; through the corresponding high-side driver with a fixed ratio of the instant current; through the corresponding high-side driver with a fixed ratio of the instant current high quarter than a fixed ratio of the instant current high quarter than a fixed ratio of the instant current high quarter than a fixed ratio of the instant current high quarter than a fixed ratio of the instant current high quarter than a fixed ratio of the instant current high quarter than a fixed ratio of the instant current high quarter high quarter than a fixed ratio of the instant current high quart	34	NC	Not connected		
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38 CLK SPI: serial clock input 39 DO SPI: serial data output (push pull output stage) 40 DI SPI: serial data input 41 CSN SPI: chip select not input 42 TxD_L LIN Transmit data input 43 RxD_L/NINT RxDL -> LIN receive data output; NINT -> indicates local/remote wake-up events (push pull output stage) 44 LIN_FLASH LIN Flash Mode enable (former TxD_C pin, to guarantee family compatibility) 45 NC Not connected 46 DIR1 Direct Drive Input 1 47 PWMH PWMH input: this input signal can be used to control the H-bridge Gate Drivers. 48 DIRH Direct Drive Input 2 49 DIR2 Direct Drive Input 2 NRESET	36	СМ	CM_SEL_x (CR 7) of the; Control Register this output sources an image of the instant current; through the corresponding high-side driver with a		
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40 DI SPI: serial data input  41 CSN SPI: chip select not input  42 TxD_L LIN Transmit data input  43 RxD_L/NINT RxDL -> LIN receive data output; NINT -> indicates local/remote wake-up events (push pull output stage)  44 LIN_FLASH LIN Flash Mode enable (former TxD_C pin, to guarantee family compatibility)  45 NC Not connected  46 DIR1 Direct Drive Input 1  47 PWMH PWMH input: this input signal can be used to control the H-bridge Gate Drivers.  48 DIRH Direction Input: this input controls the H-bridge Drivers for the external MOSFETs  49 DIR2 Direct Drive Input 2  NRESET NRESET NRESET NRESET NICE NOT	38	CLK	SPI: serial clock input		
41 CSN SPI: chip select not input  42 TxD_L LIN Transmit data input  43 RxD_L/NINT RxDL -> LIN receive data output; NINT -> indicates local/remote wake-up events (push pull output stage)  44 LIN_FLASH LIN Flash Mode enable (former TxD_C pin, to guarantee family compatibility)  45 NC Not connected  46 DIR1 Direct Drive Input 1  47 PWMH PWMH input: this input signal can be used to control the H-bridge Gate Drivers.  48 DIRH Direction Input: this input controls the H-bridge Drivers for the external MOSFETs  49 DIR2 Direct Drive Input 2  NRESET NRESET NRESET NINE SPICE NINE SPICE	39	DO	SPI: serial data output (push pull output stage)		
42 TxD_L LIN Transmit data input  43 RxD_L/NINT RxDL -> LIN receive data output; NINT -> indicates local/remote wake-up events (push pull output stage)  44 LIN_FLASH LIN Flash Mode enable (former TxD_C pin, to guarantee family compatibility)  45 NC Not connected  46 DIR1 Direct Drive Input 1  47 PWMH PWMH input: this input signal can be used to control the H-bridge Gate Drivers.  48 DIRH Direction Input: this input controls the H-bridge Drivers for the external MOSFETs  49 DIR2 Direct Drive Input 2  NRESET NRESET NRESET NRESET NINTER STATE OF THE PROPERTY OF THE PROPE	40	DI	SPI: serial data input		
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events (push pull output stage)  LIN_FLASH  LIN_FLASH  LIN_FLASH  LIN Flash Mode enable (former TxD_C pin, to guarantee family compatibility)  NC  Not connected  DIR1  Direct Drive Input 1  PWMH  PWMH input: this input signal can be used to control the H-bridge Gate Drivers.  Direction Input: this input controls the H-bridge Drivers for the external MOSFETs  DIR2  Direct Drive Input 2  NReset output to micro controller; (reset state = LOW) (low-side switch with drain connected to the output pin and internal pull up resistance to	42	TxD_L	LIN Transmit data input		
44 LIN_FLASH compatibility)  45 NC Not connected  46 DIR1 Direct Drive Input 1  47 PWMH PWMH input: this input signal can be used to control the H-bridge Gate Drivers.  48 DIRH Direction Input: this input controls the H-bridge Drivers for the external MOSFETs  49 DIR2 Direct Drive Input 2  NReset output to micro controller; (reset state = LOW) (low-side switch with drain connected to the output pin and internal pull up resistance to	43	RxD_L/NINT	RxDL -> LIN receive data output; NINT -> indicates local/remote wake-up events (push pull output stage)		
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PWMH input: this input signal can be used to control the H-bridge Gate Drivers.  Direction Input: this input controls the H-bridge Drivers for the external MOSFETs  Direct Drive Input 2  NRESET	45	NC	Not connected		
Drivers.  Direction Input: this input controls the H-bridge Drivers for the external MOSFETs  Direct Drive Input 2  NReset output to micro controller; (reset state = LOW) (low-side switch with drain connected to the output pin and internal pull up resistance to	46	DIR1	Direct Drive Input 1		
MOSFETs  49 DIR2 Direct Drive Input 2  NReset output to micro controller; (reset state = LOW) (low-side switch with drain connected to the output pin and internal pull up resistance to	47	PWMH			
NReset output to micro controller; (reset state = LOW) (low-side switch with drain connected to the output pin and internal pull up resistance to	48	DIRH			
NRESET with drain connected to the output pin and internal pull up resistance to	49	DIR2	Direct Drive Input 2		
	50	NRESET	with drain connected to the output pin and internal pull up resistance to		
51 5V_1 Voltage regulator 1 output: 5 V supply e.g. micro controller	51	5V_1	Voltage regulator 1 output: 5 V supply e.g. micro controller		
52 NC Not connected	52	NC	Not connected		



Table 1. Pin definitions and functions (continued)

Pin	Symbol	Function		
53	NINT	Interrupt output (low active; push-pull output stage) to indicate V <sub>SREG</sub> early warning (Active mode); indicates wake-up events from V1_standby mode		
54	NC	Not connected		
55	NC	Not connected		
56	Debug	Debug input to deactivate the window watchdog (high active)		
57	LIN	LIN bus line		
58	5V_2	Voltage regulator 2 output: 5 V supply for external loads (potentiometer, sensors). V2 is protected against reverse supply		
59	GL1	Gate driver for PowerMOS low-side switch in half-bridge 1		
60	SH1	Source of high-side switch in half-bridge 1		
61	GH1	Gate driver for PowerMOS high-side switch in half-bridge 1		
62	GH2	Gate driver for PowerMOS high-side switch in half-bridge 2		
63	SH2	Source of high-side switch in half-bridge 2		
64	GL2	Gate driver for PowerMOS low-side switch in half-bridge 2		



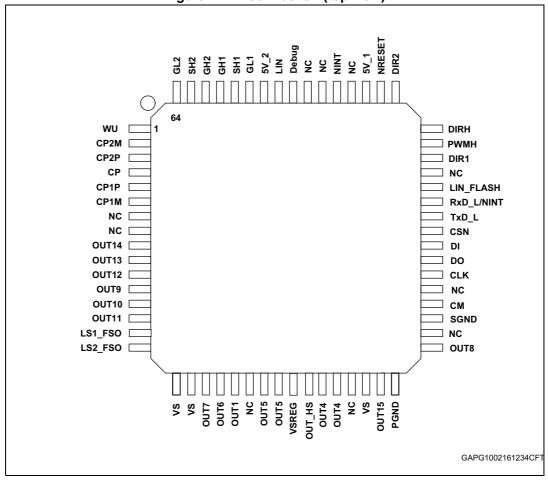


Figure 2. Pin connection (top view)



L99DZ120 Revision history

# 2 Revision history

Table 2. Document revision history

Date	Revision	Changes	
03-Nov-2016	1	Initial release.	

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