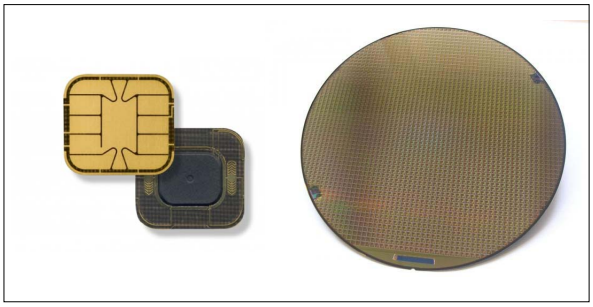
MR31Z052

ST31-K330A platform secure dual interface MCU with enhanced security and 52 Kbytes of EEPROM (MIFARE® supported)

Data brief



Features

Hardware features

- ARM® SecurCore® SC000™ 32-bit RISC core
- 245 Kbytes of User ROM
- 8 Kbytes of User RAM
- 52 Kbytes of User EEPROM
- CPU clock frequency up to 28 MHz
- Power-saving Standby state
- Contact assignment compatible with ISO/IEC 7816-3 standards
- Asynchronous receiver transmitter (IART) for high speed serial data support (ISO/IEC 7816-3 T=0/T=1 and EMV compliant)
- ESD protection greater than 5 kV (HBM)

Contactless features

- Complies with ISO/IEC 14443 Type A, B and B', and PayPass® standards
- 13.56 MHz carrier frequency
- RFUART (RF universal asynchronous receiver transmitter) up to 848 Kbps
- Very High Bit Rate (VHBR): Tx = 6.8 Mbps and Rx = 1.7 Mbps
- Simultaneous mode (Contact and Contactless)
- 4-Kbyte RF frame buffer in dedicated RFUART RAM
- MIFARE Plus® and MIFARE® DESFire® EV1 HW and SW implementation
- MIFARE® Classic available as part of MIFARE Plus®

Security features

- Three-key Triple DES accelerator
- AES accelerator
- NESCRYPT coprocessor for public key cryptography algorithm
- Protection against multiple attacks

1 Description

Designed for secure ID and banking applications, the MR31Z052 is a serial access microcontroller that incorporates the most recent generation of ARM® processors for embedded secure systems. Its SecurCore® SC000™ 32-bit RISC core is built on the Cortex®-M0 core with additional security features to help to protect against advanced forms of attacks.

Cadenced at 28 MHz, the SecurCore® SC000™ core brings great performance and excellent code density thanks to the ARM® Thumb®-2 instruction set.

MR31Z devices implement MIFARE® DESFire® EV1 or MIFARE Plus® (including MIFARE® Classic) technology. MIFARE, MIFARE Plus, MIFARE DESFire and MIFARE Classic are registered trademarks of NXP B.V. and are used under license.

An RF interface including an RF universal asynchronous receiver (RFUART) enables contactless communication up to 848 Kbps compatible with the ISO/IEC 14443 Type A and Type B standards.

Very High Bit Rates (VHBR, Tx = 6.8 Mbps and Rx = 1.7 Mbps) are possible in Type B frames.

A Simultaneous mode where contactless communication can be enabled while the device is in Contact mode is also available.

The MR31Z052 also offers a serial communication interface fully compatible with the ISO/IEC 7816-3 standard (T=0, T=1).

Two 16-bit general-purpose timers are available; one is configurable as a watchdog.

The MR31Z052 features hardware accelerators for advanced cryptographic functions. The AES accelerator provides a high-performance implementation of AES-128, AES-192, AES-256 algorithms. The 3-key Triple DES accelerator (EDES+) peripheral enables Cipher Block Chaining (CBC) mode, fast DES and triple DES computation based on three key registers and one data register, while the NESCRYPT crypto-processor efficiently supports the public key algorithm with native operations up to 4096 bits long.

The MR31Z family operates in the –25 to +85 °C temperature range, at 3 V and 5 V supply voltage ranges in Contact mode and complies with ISO/IEC 14443 specification limits. A comprehensive range of power-saving modes enables the design of efficient low-power and contactless applications.

Software development tools description

Dedicated SecurCore® SC000™ software development tools are provided by ARM® and Keil®. This includes the Instruction Set Simulator (ISS) and C compiler. The documentation is available on the ARM® and Keil® web sites.

Moreover, STMicroelectronics provides:

- A time-accurate hardware emulator controlled by the Keil® debugger tool and the ST development environment.
- A complete product simulator based on Keil® ISS simulator for the SecurCore® SC000™ CPU.

2 Revision history

Table 1. Document revision history

Date	Revision	Changes
07-Jun-2012	1	Initial release.
04-Apr-2014	2	Updated MIFARE®, PayPass® and Keil® trademarks.
19-Jun-2014	3	Updated secure MCU platform information.

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