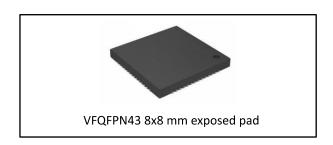


IEEE802.3bt PoE-PD interface with integrated dual-active-bridge

Data brief



Features

- System in package:
 - Dual-active-bridge with 100 V MOSFETs and 0.2 Ω total path resistance
 - 100 V, 0.1 Ω hot-swap MOSFETs
 - PoE-PD single-signature interface,
 IEEE 802.3af/at/bt (draft 2.3)-compliant
- Detection and support of high power, 4-pair applications
- Support 12 V auxiliary sources
- Identifies which kind of PSE (standard or legacy) is connected and provides successful IEEE802.3 af/at/bt classification indications as combination of T0, T1 and T2 signals (open-drain)
- Smart operational mode selection by command signals: STBY, RAUX and FAUX
- Programmable classification current with 3.3 ms delay
- Autoclass feature (optional)
- Advanced energy-saving MPS timings
- Hot-swap current protection in two steps:
 DC with 1 ms delay and short-circuit with
 10 μs delay
- Start-up phase (pre-charge of the output capacitor) due to an internally limited current source
- PGD signal (open-drain) to enable an external PWM controller
- Thermal shutdown protection
- VFQFPN package with 6 exposed pads

Applications

- High power 4-pair powered devices
- Outdoor security cameras
- High power pay systems
- WLAN access points
- IoT applications
- PoE lighting systems

Description

The PM8805 is a system in package for Power over Ethernet (PoE) and powered devices (PD) applications. It embeds: two active bridges and their driving circuitry, a charge pump to drive high-side MOSFETs, the hot-swap MOSFET and the standard single-signature interface IEEE 802.3bt-compliant, including detection, classification, UVLO and inrush current limitation. The active bridges sustain up to 1 A current and the hot-swap MOSFET is designed to safely work up to 2 A. The device performs IEEE 802.3bt physical layer classification scheme, providing the system with an indication of successful PSE-type. The device identifies a 4-pair PSE. monitoring the pairs of the Ethernet cable and providing the system with a dedicated matrix of Tx signals. The device works with power either from the Ethernet cable or from an external power source such as a wall adapter, with the likelihood of the auxiliary source being prevalent over PoE. The device is suitable to build the interface section of PoE switch mode power supplies targeting the highest conversion efficiency. It provides a PGD signal that can be used to enable a PWM controller, a DC-DC converter or a LED driver.

Table 1: Device summary

Order code	Package	Packing	
PM8805TR	VFQFPN 8X8X1.0 43L pitch 0.5	Tape and reel	

March 2017 DocID030407 Rev 1 1/12

Contents PM8805

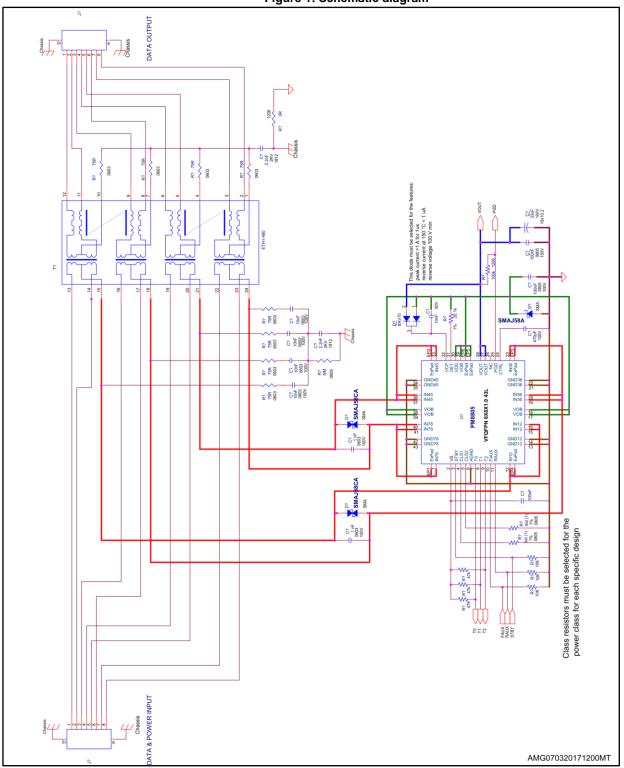
Contents

1	Schematic	
2	Block diagram	2
3	_	
4		
5	Engineering samples usage	8
6	Packing information	
	6.1 VFQFPN43 package information	(
7	Revision history	11

PM8805 Schematic

1 Schematic

Figure 1: Schematic diagram



Block diagram PM8805

2 **Block diagram**

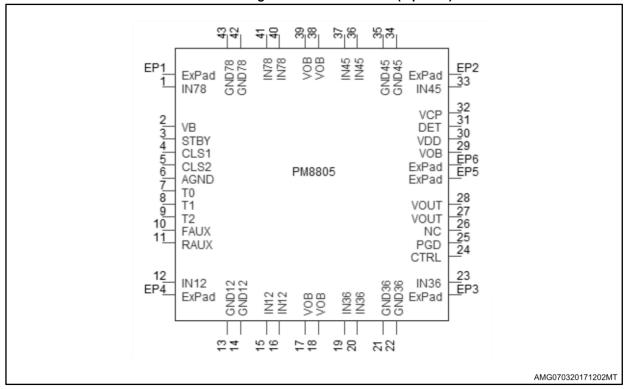
VOB=VDD CTRL V_v __VOUT _{5V} VB VΒ regulator VOUT SENSE 12V Inrush regulator 3.3V VDD-0.5V Hot Swap regulator Controller CTRL PGD -□ VDD+5V START Inrush END T2 -□ 85ms Timer Th SHDN Main control → PGD override UVLO, Th SHDN logic ➤ UVLO ➤ Inrush Charge IN12 IN78 Pump Thermal Protect MPS=10/18mA Th SHDN T=290/305ms; D=3/27% Enable MPS UVLO, Th SHDN VDD IN36 IN45 -□ $\sum_{n=0}^{\infty} 100\Omega$ □ RAUX □STBY □FAUX

Figure 2: PM8805 general internal block diagram

AMG070320171201MT

3 Pin descriptions and connection diagrams

Figure 3: Pin connections (top view)



PM8805 overview PM8805

4 PM8805 overview

The PM8805 integrates a dual bridge MOSFET and a PD-PoE single-signature interface, specifically designed to support high power 4-pair (4P) applications, as per IEEE802.3bt standard, but it can work with high efficiency 2P applications.

Typically after the data transformer, a diode bridge is used to set a defined polarity on the input voltage since this polarity on the Ethernet cable may vary.

By considering the maximum power levels defined by the IEEE802.3-2015 standard (25 W for a type2 PD), diode bridge power losses may still be acceptable, but with new power-hungry applications such as UPOE, with more than 50 W at PD end, power losses of a standard diode bridge become too high.

The same consideration is valid for standard applications needing to squeeze the maximum available power from the PSE. For example, by comparing a diode bridge with V_d = 0.8 V with a 100 m Ω R_{DS(on)} MOSFET bridge, the gain at 0.5 A, 50 V is about 0.75 W out of 25 W, i.e. about 3% overall efficiency.

Table 2: Multiple-event classification description table

PD type	1 st event (CLS1)	2 nd event (CLS1)	3 rd event (CLS2)	4 th event (CLS2)	5 th event (CLS2)	Classification	Pairs
Type 1	Class 0-3	(exit)				Class 0-3	2
Type 2	Class 4	Class 4	(exit)			Class 4	2
	Class 1-3 long pulse	(exit)				Class 1-3	2 or 4
	Class 4 long pulse	Class 4	(exit)			Class 4	2 or 4
Type 3	Class 4 long pulse	Class 4	Class 0	Class 0	(exit)	Class 5	4
	Class 4	Class 4	Class 4	Class 4	(avit)	Class C	4
	long pulse	Class 4	Class 1	Class 1	(exit)	Class 6	4
	Class 4	Class 4	Class 2	Class 2	Class 2	Class 7	4
T 4	long pulse	Class 4	Class 2 Class 2 Class 7	Class /	4		
Type 4	Class 4	Class 4	01 0	Class 2	Class 2	Class	4
	long pulse	UIASS 4	Class 3	Class 3	Class 3	Class 8	4

PM8805 overview

Table 3: Power available at the PD PI depending on assigned class

PD requested class	Number of PSE class events	Assigned class	Power available at the PD PI (W)	PM8805 outputs	
Class	Class events	Class	FD FI (VV)	T0	T1
Any	0	0	13.0	1	1
0	1	0	13.0	1	1
1	1	1	3.84	1	1
2	1	2	6.49	1	1
3 to 8	1	3 or 0	13.0	1	1
4 to 8	2 or 3	4	25.5	0	1
5	4	5	40.0	1	0
6 to 8	4	6	51.0	1	0
7	5	7	62.0	0	0
8	5	8	71.3	0	0

The PM8805 can cover all single-signature PD types and classes. As far as a type1-2 PD is concerned, the PM8805 presents a class 0–4 current within the classification range 14.5 V to 20.5 V using the CLS1 pin during the first two class events. From the 3rd class event onwards, the CLS2 pin is activated, so it is possible to set the new classes defined for type 3 and 4 PDs.

Input Voltage Detection Classification Power On V_{uvlo_rising} 1st Class 2nd Class 3rd Class nth Class Event Event **Event Event** V_{off_class} Class Range V_{on_class} Mark Range V_{rst_cls} Autoclass on \(\square CLS1 CLS2 \leftrightarrow \leftrightarrow Td_cls Tcls_Typ3 Td_cls Td_cls Td_cls AMG070320171203MT

Figure 4: Classification signals and timings

Figure 5: CLS internal circuit

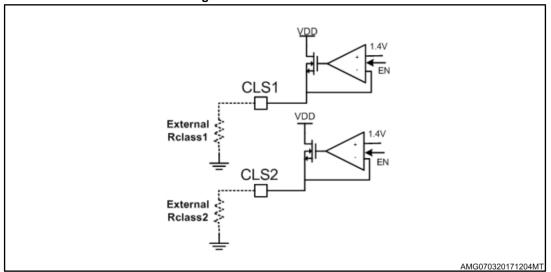


Table 4: Classification current description

PD class	CLS1 resistor (Ω)	CLS2 resistor (Ω)	Min. (mA)	Max. (mA)
Class 0	2000	2000	0	4
Class 1	150	150	9	12
Class 2	80.6	80.6	17	20
Class 3	51.1	51.1	26	30
Class 4	36.5	36.5	36	44
Class 5	36.5	2000	36/0	44/4
Class 6	36.5	150	36/9	44/12
Class 7	36.5	80.6	36/17	44/20
Class 8	36.5	51.1	36/26	44/30

5 Engineering samples usage

Parts marked as the PM8805-ESh/ESh2 are not yet qualified, therefore since they cannot be used in production any consequence coming from such usage is not under ST's responsibility. Before using these engineering samples to run qualification activity, contact ST quality department.

PM8805 Packing information

6 Packing information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

6.1 VFQFPN43 package information

Figure 6: VFQFPN43 package outline

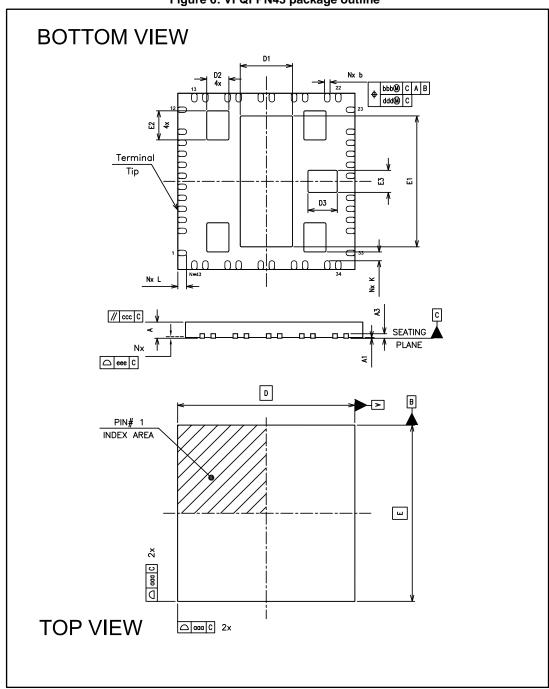
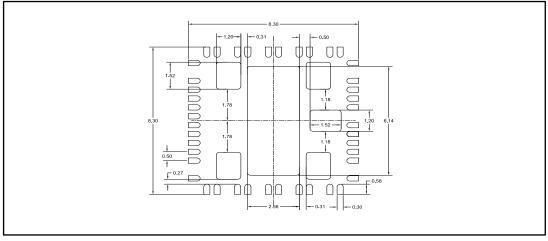


Table 5: VFQFPN43 mechanical data

Dim		mm	
Dim.	Min.	Тур.	Max.
Α	0.8	0.9	1.00
A1	0.00	0.02	0.05
A3		0.20 ref.	
b	0.23	0.28	0.33
D		8.00 BSC	
E		8.00 BSC	
D1	2.205	2.355	2.455
E1	5.790	5.940	6.040
D2	0.85	1.00	1.10
E2	1.17	1.32	1.42
D3	1.17	1.32	1.42
E3	0.85	1.00	1.10
K	0.2		
L	0.30	0.40	0.50
N		43	
NOTES		1,2	
LF P/N		443431	

Symbol	Tolerance of form and position
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.05
Note	0.08
Ref	

Figure 7: VFQFPN43 recommended footprint



PM8805 Revision history

7 Revision history

Table 6: Document revision history

Date	Revision	Changes
22-Mar-2017	1	First revision

IMPORTANT NOTICE - PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics - All rights reserved