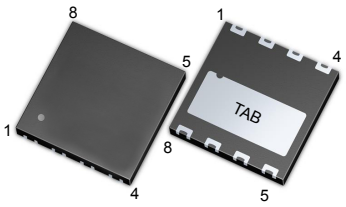
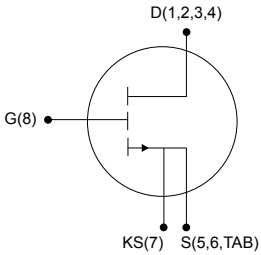
SGT080R70ILB

Data brief

700 V, 60 mΩ typ., 29 A, e-mode PowerGaN transistor



DFN 8x8



G8D1234S56TABKS7

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	Series
SGT080R70ILB	700 V	80 mΩ	29 A	G-HEMT

- Enhancement mode normally off transistor
- Very high switching speed
- High power management capability
- Extremely low capacitances
- Kelvin source pad for optimum gate driving
- Zero reverse recovery charge

Applications

- Adapters for tablets, notebook and AIO
- USB type-C PD adapters and quick chargers
- AC-DC converters
- DC-DC converters

Description

The SGT080R70ILB is a 700 V, 29 A e-mode PowerGaN transistor combined with a well established packaging technology. The resulting G-HEMT device provides extremely low conduction losses, high current capability and ultra fast switching operation to enable high power density and unbeatable efficiency performances.

Product status link
SGT080R70ILB

Product summary	
Order code	SGT080R70ILB
Marking	080R70I
Package	DFN 8x8
Packing	Tape and reel

1 Electrical ratings

T_C = 25 °C unless otherwise specified.

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	700(1)	V
	Drain-source voltage (transient, t_p < 200 µs)	800	
V_{GS}	Gate-source voltage	-6 to 7	V
I_D	Drain current (continuous)	29(2)	A
I_{DM}	Pulse drain current (t_p = 10 µs)	58	A
P_{TOT}	Total power dissipation at T_C = 25 °C	188(2)	W
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Recommended continuous maximum bus voltage during switching operations should not exceed 450 V.*
2. *Limited by design.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.52	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	33.6(1)	°C/W

1. *When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.*

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Drain-source leakage current	V_{GS} = 0 V, V_{DS} = 700 V		5	65	µA
		V_{GS} = 0 V, V_{DS} = 700 V, T_J = 150 °C		13	390(1)	
I_{GSS}	Gate-source leakage current	V_{DS} = 0 V, V_{GS} = 6 V		163		µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 30.7 mA	1.2	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 6 V, I_D = 8 A		60	80	mΩ
		V_{GS} = 6 V, I_D = 8 A, T_J = 150 °C		135		

1. *Specified by design, not tested in production.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 400 V, f = 100 kHz	-	225	-	pF
C_{oss}	Output capacitance		-	70	-	pF
C_{rss}	Reverse transfer capacitance		-	0.5	-	pF
$C_{o(er)}$(1)	Equivalent output capacitance energy related	V_{GS} = 0 V, V_{DS} = 0 to 400 V	-	105	-	pF
$C_{o(tr)}$(2)	Equivalent output capacitance time related		-	150	-	pF
R_g	Intrinsic gate resistance	f = 5 MHz, I_D = 0 A	-	3	-	Ω
V_{plat}	Gate plateau voltage	V_{DS} = 400 V, I_D = 8 A	-	2.2	-	V
Q_g	Total gate charge	V_{GS} = 0 to 6 V, V_{DS} = 400 V, I_D = 8 A	-	6.2	-	nC
Q_{gs}	Gate-source charge		-	0.5	-	nC
Q_{gd}	Gate-drain charge		-	2.2	-	nC
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V, V_{DS} = 400 V	-	0	-	nC
Q_{oss}	Output charge		-	60	-	nC

1. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to the stated value.*
2. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to the stated value.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DS} = 400 V, I_D = 16 A, V_{GS} = 6 V, $R_{G(on)}$ = 10 Ω, $R_{G(off)}$ = 2 Ω, L = 318 µH	-	3	-	ns
t_r	Rise time		-	4	-	ns
$t_{d(off)}$	Turn-off delay time		-	5	-	ns
t_f	Fall time		-	4	-	ns

Table 6. Reverse conduction

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Source-drain reverse voltage	V_{GS} = 0 V, I_{SD} = 8 A	-	2.3	-	V

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
02-Apr-2025	1	First release.

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.