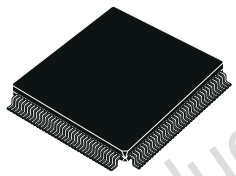
JPC563M60

32-bit PowerPC MCU with 1 MByte Flash and 48 KByte RAM memories

Data Brief

Features

- 80 MHz e200z3 PowerPC core
  - Variable length instruction encoding (VLE)
  - SIMD
  - FPU
- Memory organization
  - 1 MByte on-chip Flash memory with ECC and Read While Write (RWW)
  - 48 KByte on-chip RAM with StandBy functionality (24 KByte) and ECC
  - 12 + 2.5 KByte eTPU code and data RAM
  - 3 x 4 Crossbar
- Interrupt
  - 307 nodes interrupt controller (with NMI)
  - 32-channels DMA
- Serial channels
  - 2 x eSCI
  - 2 x DSPI with microsecond support
- 2 x FlexCAN
  - 1 x 32 messages
  - 1 x 64 messages
- 2 x A/D Converters
  - 32-channels 12-bit (multiplexed on the 2 ADC)
  - 6 command queues
  - Trigger and DMA support
  - 1µs Minimum conversion time
  - 160ns sampling time at 80MHz
- 1 x eTPU2 (second generation eTPU)
  - 12KByte Code and 2.5KByte Data RAMs
  - 32 standard channels
  - Architectural enhancements to improve code efficiency and added flexibility
- 1 x eMIOS
  - 16 unified channels
- Boot Assist Module (BAM)



LQFP144

- Nexus
  - Class 2+ for the PPC core
  - Class 1 for the eTPU
  - 3.3V or 5V pins shared with IOs
- JTAG
  - 2 pins serial JTAG
- Clock generation
  - On-chip 4-40 MHz main oscillator
  - On-chip PLL with Frequency Modulation
- Up to 105 general purpose I/O lines
  - Individually programmable as input, output or special function
  - Programmable threshold (hysteresis)
- Power reduction mode
- Single voltage supply: 5V ±10% for TQFP144 package
  - On-chip voltage regulator for regulating 5V down to 1.2V for core logic
  - On-chip voltage regulator for regulating 5V down to 3.3V for Nexus interface
- Packages
  - LQFP144
  - LBGA208
  - LBGA496 for tools (Vertical, calibration, full Nexus trace port) dual supply 5V and 3.3V.

This product is jointly developed by Freescale Semiconductors and STMicroelectronics

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1 Introduction

The JPC563M60 is the first microcontroller in the JPC563 family of devices, jointly developed by Freescale Semiconductors and STMicroelectronics based on the PowerPC[a] Book E architecture.

The JPC563 family is a completely compatible extension to the Freescale MPC5500 family, targeted towards lower end applications.

This document describes the features of the JPC563M60 and highlights important electrical and physical characteristics of the device.

The JPC563 family of devices contains all the features of the MPC5500 family and many new features coupled with high performance 90nm CMOS technology to provide substantial reduction of cost per feature and significant performance improvement.

The host processor core of the JPC563M60 complies with the PowerPC Book E architecture. It is 100% user mode compatible (with floating point library) with the classic PowerPC instruction set. The Book E architecture has enhancements that improve the PowerPC architecture's fit in embedded applications. In addition to the classic PowerPC instruction set, this core also has additional instruction support for digital signal processing (DSP).

The JPC563M60 has a single level of memory hierarchy consisting of 48-kbyte on-chip SRAM. 1M bytes of internal flash memory. The JPC563M60 also has an external bus interface for 'calibration', that is only accessible when using the Freescale Vertical Calibration System. This external bus interface has been designed to support most of the standard memories used with the MPC5xx family.

On-chip modules include:

- Single issue, 32-bit PowerPC Book E compliant e200z3 CPU core complex
  - Includes Freescale Variable Length Encoding (VLE) enhancements for code size reduction
- 32-channel enhanced direct memory access controller (eDMA)
- Interrupt controller (INTC) capable of handling 307 selectable-priority interrupt sources
- Frequency modulated phase-locked loop (PLL)
- Calibration external bus interface (EBI) (Only in Vertical Calibration System - not on production package)
- System integration unit (SIU), Boot assist module (BAM)
- 1 MByte on-chip flash with flash control unit (FCU)
  - Fetch Accelerator - for single cycle flash access @80MHz
- 48 KByte on-chip static RAM (including 24 KByte standby RAM)
- Boot assist module (BAM)
- 32-channel second generation enhanced time processor unit (eTPU2)
  - 32 standard ETPU channels
  - Architectural enhancements to improve code efficiency and added flexibility
- 16-channels enhanced modular Input Output System (eMIOS)

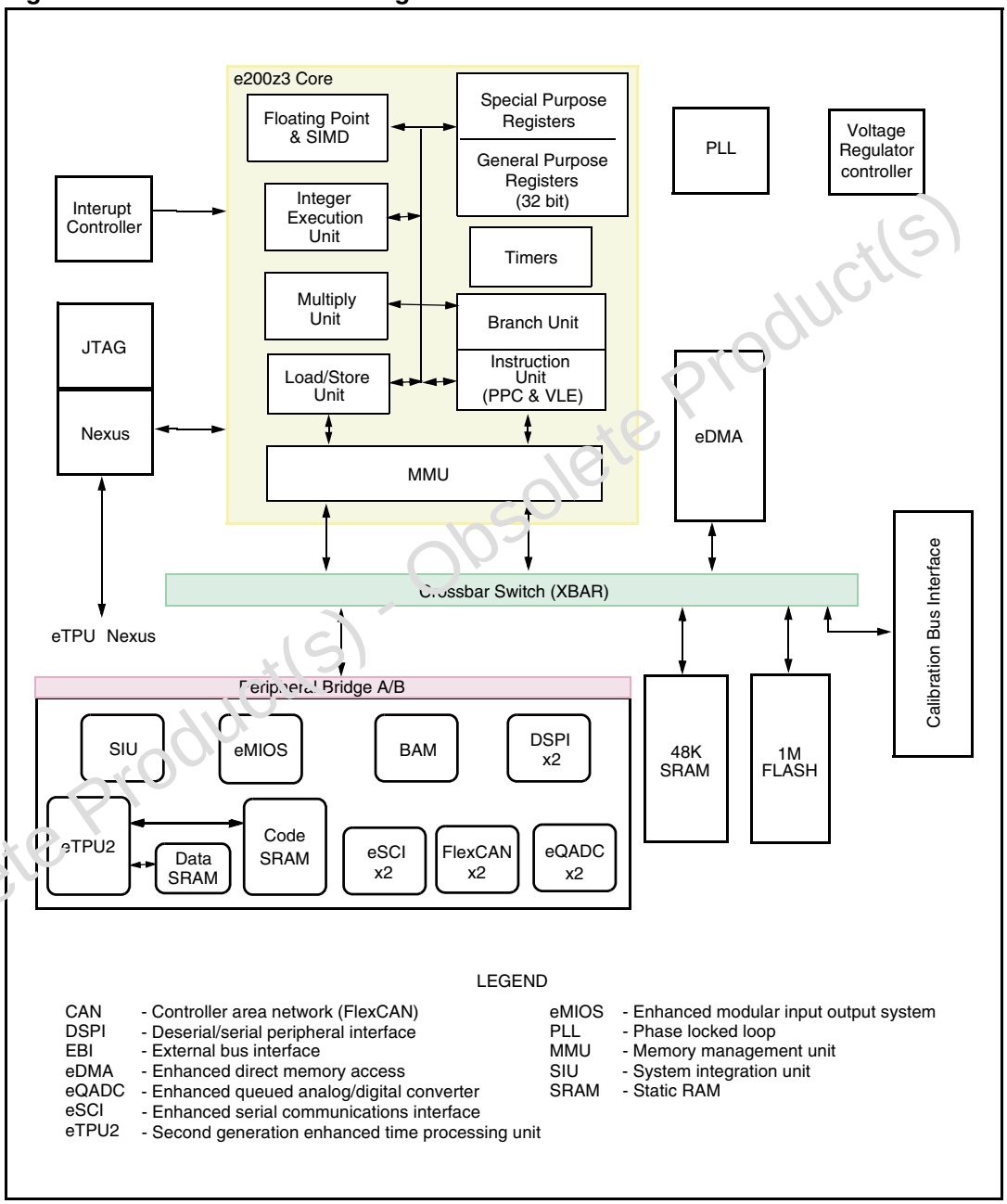
a. PowerPC is a trademark of International Business Machines Corporation.

- Enhanced queued analog-to-digital converters (eQADC) with knock signal support
- Junction temperature sensor
- 2 deserial serial peripheral interface (DSPI) modules (compatible with Microsecond Bus)
- 2 enhanced serial communication interface (eSCI) modules
- 2 Controller area network (FlexCAN) modules, one of them having 64 message objects
- Nexus development interface (NDI) per IEEE-ISO 5001-2003 standard
- Device/board test support per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.7). Including support for compact-JTAG to reduce the number of JTAG pins and increase customer IO
- On-chip voltage regulator controller for regulating 5.0V down to 3.3V for internal functions and Nexus interface
- On-chip voltage regulator controller for regulating 5.0V down to 1.2V for core logic (using external ballast transistor)
- Available in LQFP144 (20mm x 20mm, 0.5mm pitch), LBGA208 & Vertical Calibration System

2 Block diagram

Figure 1 shows a top-level block diagram of JPC563M60.

Figure 1. JPC563M60 block diagram



3 Overview

This section provides a high level description of the features found in the JPC563M60.

- Operating parameters
  - Fully static operation, 0 MHz - 80 MHz (plus 2% frequency modulation - 82MHz)
  - -40° to 150° C junction temperature
  - Low power design
    - Less than 500 milliWatts power dissipation (nominal)
    - Designed for dynamic power management of core and peripherals
    - Software controlled clock gating of peripherals
  - Fabricated in 90nm process
  - 1.2V internal logic
  - Input and output pins with 5.0V +-10% range (4.5V to 5.5V)
    - 40%/70% V_{DDE} CMOS switch levels (with hysteresis)
    - Selectable hysteresis
    - Selectable slew rate control
  - Calibration bus pins support 1.8V to 3.3V +-10% (1.6V - 3.6V) operation
    - Selectable drive strength control
  - Nexus pins support 3.3V or 5.0V +-10% (3.0V - 3.6V or 4.5V - 5.5V) operation
    - Selectable drive strength control
    - Unused pins configurable as GPIO or timed IO
  - Designed with EMI reduction techniques
    - Phase-locked loop
    - Frequency modulateion of system clock frequency
    - On-chip bypass capacitance
    - Selectable slew rate and drive strength
- High performance e200z3 core processor
  - 32-bit *PowerPC Book E* programmer's model
  - Variable length encoding enhancements
    - Allows PPC instruction set to be optionally encoded with a mixture of 16 and 32 bit instructions
    - Results in smaller code size
  - Single issue, 32-bit *PowerPC Book E* compliant CPU
  - In-order execution and retirement
  - Precise exception handling
  - Branch processing unit
    - Dedicated branch address calculation adder
    - Branch acceleration using branch lookahead instruction buffer
  - Load/store unit
    - 1 cycle load latency
    - Fully pipelined

  - Big and Little endian support
  - Misaligned access support
  - Zero load-to-use pipeline bubbles
- Thirty-two 64 bit general purpose registers (GPRs)
- Memory management unit (MMU) with 8-entry fully-associative translation look-aside buffer (TLB)
- Thirty-two 64-bit general purpose registers (GPRs)
- Separate instruction bus and load/store bus
- Vectored interrupt support
- Interrupt latency < 120ns @80 MHz (measured from interrupt request to execution of first instruction of interrupt exception handler)
- Non maskable interrupt input. For handling external events that must produce an immediate response. Such as power down detection. (May not be recoverable)
- Critical Interrupt input. For external interrupt sources that are higher priority than provided by the Interrupt Controller. (Always recoverable)
- New 'Wait for Interrupt' instruction, to be used with new low power modes.
- Reservation instructions for implementing read-modify-write constructs
- Signal processing extension (SPE) APU
  - Operating on all 32 GPRs that are all extended to 64-bit wide
  - Provides a full compliment of vector & scalar integer and floating point arithmetic operations (including integer vector MAC & MUL operations) (SIMD)
  - Provides rich array of extended 64-bit loads and stores to/from extended GPRs
  - Fully code compatible with e200z6 core
- Floating point
  - IEEE 754 compatible with software wrapper
  - Scalar single precision in hardware, double precision with software library
  - Conversion instructions between single precision floating point and fixed point
  - Fully code compatible with e200z6 core
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency
- Extensive system development support through Nexus debug port

- Advanced microcontroller bus architecture (AMBA) crossbar switch (XBAR)
  - 3 master ports, 4 slave ports
    - Masters: CPU Instruction bus; CPU Load/store bus; DMA
    - Slaves: Flash; SRAM; peripheral bridge; calibration EBI
  - 32-bit internal address bus, 64-bit internal data bus
- Enhanced direct memory access (eDMA) controller
  - 32 channels support independent 8, 16 or 32 bit single value or block transfers
  - Supports variable sized queues and circular queues
  - Source and destination address registers are independently configured to post-increment or remain constant
  - Each transfer is initiated by a peripheral, CPU, or eDMA channel request

  - Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- Interrupt controller (INTC)
  - Unique 9-bit vector per interrupt source for 307 interrupt sources
  - 8 software settable interrupt sources
  - 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
  - Priority elevation for shared resources
  - Critical and Non Maskable Interrupts that bypasses the interrupt controller and connects directly to the CPU
- Frequency modulated phase-locked loop (FMPLL)
  - Input clock frequency from 4 MHz to 20 MHz
  - Voltage controlled oscillator (VCO) range from 256MHz to 512MHz.
  - Frequency modulation of system clock to reduce electromagnetic emissions peaks
  - Reduced frequency divider (RFD) for reduced frequency operation without re-lock
  - Lock detect circuitry continuously monitors lock status
  - Loss of clock (LOC) detection for reference and feedback clocks
  - Self-clocked mode (SCM) operation
  - On-chip loop filter (reduces number of external components required)
- Calibration bus interface (EBI)
  - 1.8 to 3.3V ± 10% I/O (1.6V to 3.6V)
  - Memory controller with support for various memory types
  - 16-bit data bus, up to 32-bit address bus
  - Selectable drive strength
  - Configurable bus speed modes
  - Bus monitor
  - Configurable wait states
- System integration unit (SIU)
  - Centralized GPIO control of 77 I/O pins
  - Centralized pad control on a per-pin basis
  - System reset monitoring and generation
  - External interrupt inputs, filtering and control
  - Critical interrupt control
  - Non Maskable Interrupt control
  - Internal multiplexer subblock (IMUX)
- Error correction status module (ECSM)
  - Configurable error-correcting codes (ECC) reporting
- On-chip FLASH
  - 1 MByte flash memory
    - Configured as 64K x 128 bits
    - Accessed via a 64-bit wide bus interface

  - Fetch accelerator
    - Provide single cycle flash access @80MHz
    - Quadruple 128 bit wide prefetch/burst buffers
    - Prefetch buffers can be configured to prefetch code or data or both
  - Censorship protection scheme to prevent flash content visibility
  - Hardware read-while-write feature that allows blocks to be erased/programmed while other blocks are being read. (used for EEPROM emulation & data calibration)
  - 14 blocks (4 x 16k + 4 x 48k + 6 x 128k bytes) to support features such as boot block, operating system block and EEPROM emulation.
  - Hardware programming state machine
- On-chip static RAM
  - 48 KByte general purpose RAM of which 24 KByte are on standby power supply
- Boot assist module (BAM)
  - Enables and manages the transition of MCU from reset to user code execution in the following configurations:
    - Execution from internal
    - Download and execution of code via FlexCAN or eSCI
- System timer
  - 5 channel periodic interrupt timer
    - 32 bit wide down counter with automatic reload
    - 4 channels clocked by system clock
    - 1 channel clocked by crystal clock
    - Each channel can produce periodic software interrupt
    - 4 out of the 5 can produce periodic triggers for eQADC queue triggering
    - 1 out of the 5 can be used as wake-up timer to wake device from low power stop mode
  - Task monitor timer
    - 32 bit up counter with 8 bit prescaler
    - clocked from system clock
    - 4 channel timer compare hardware
    - Each channel can generate a unique interrupt request
    - Design to address AutoSAR task monitor function
  - System watchdog timer
    - 32 bit timer
    - clock by system clock or crystal clock
    - can generate either system reset or non maskable interrupt followed by system reset
    - Enabled out of reset
- Enhanced modular I/O system (eMIOS)
  - 16 channels (Up to 14 channels connected to pins in 144 QFP)
  - 24-bit timer resolution
  - Supports a subset of the timer modes found in eMIOS on MPC5554

  - Three selectable time bases plus shared time or angle counter bus
- Second generation enhanced time processor unit (eTPU2)
  - High level assembler/compiler
  - Enhancements to make ‘C’ compiler more efficient
  - New ‘engine relative’ addressing mode
  - 32 channels (Each channel has dedicated IO pin in 144 QFP)
  - 24-bit timer resolution
  - TCR1 divide-by-one option for improved resolution
  - 12k byte code memory and 2.5K byte data memory
  - Variable number of parameters allocatable per channel
  - Double match/capture channels
  - Angle clock hardware support
  - Nexus class 1 debug support
  - Enhancements to make DMA & interrupt operation more flexible
  - New programmable channel mode, for increased flexibility of channel hardware
- Enhanced queued A/D converter (eQADC)
  - 2 ADCs with 12 bit A/D resolution
  - Selectable resolution for increased conversion speed (8 bit & 10 bit modes)
  - 32 single ended inputs channels (Expandable to 56 channels with external multiplexers)
  - 8 channels can be used as 4 pairs of differential analog input channels.
  - Includes variable gain amplifiers on all channels for improved dynamic range (x1; x2; x4)
  - Differential channels include programmable pull-up and pull down resistors for biasing and sensor diagnostics (200k ohm; 100k ohm; 5k ohm)
  - 10 bit accuracy at 500 ksamples/s, 8 bit accuracy at 1 Msamples/s
  - Supports six queues with fixed priority.
  - Queue modes with priority-based preemption, initiated by software command or internal (eTPU or eMIOS) or external triggers
  - Queue_0 immediate conversion feature. Allows Queue_0 to abort running conversions and start a new conversion without jitter.
  - DMA and interrupt request support
  - Supports all functional modes from QADC (MPC5xx family)
  - Conversion result decimation filter
    - Decimation factor 1-16
    - 4th Order IIR filter or 8th order FIR with programmable coefficients
    - Programmable rounding and saturated modes
    - Pre-fill mode to pre-condition filter before sampling
- 2 deserial serial peripheral interface modules (DSPI)
  - SPI
    - Full duplex communication ports with interrupt and DMA request support
    - Supports all functional modes from QSPI subblock of QSMCM (MPC5xx family)

  - Support for queues in RAM
  - 6 Chip Selects, expandable to 64 with external demultiplexers
  - Programmable frame size, baud rate, clock delay and clock phase on a per frame basis
  - Modified SPI mode for interfacing to peripherals with longer setup time requirements
  - LVDS option for output clock and data to allow higher speed communication
- Deserial serial interface (DSI)
  - Pin reduction by hardware serialization and deserialization of eTPU, EMIOS channels and GPIO
  - 32 bits per DSPI module
  - Triggered transfer control and change in data transfer control (for reduced EMI)
  - Compatible with Microsecond Bus Version 1.0 downlink

- 2 Enhanced serial communication interface (eSCI) modules
  - UART mode provides NRZ format and half or full duplex interface
  - eSCI bit rate up to 1 Mbps
  - Advanced error detection, and optional parity generation and detection
  - Word length programmable as 8, 9, 12 or 13 bits (compatible with Microsecond bus uplink)
  - Separately enabled transmitter and receiver
  - Interrupt request support
- 2 FlexCAN
  - one with 32 message buffers; the second with 64 message buffers
  - Full implementation of the CAN protocol specification, Version 2.0B
  - Based on and including all existing features of the Freescale TouCAN module
  - Programmable acceptance filters
  - Short latency time for high priority transmit messages
  - Arbitration scheme according to message ID or message buffer number
  - Listen only mode capabilities
  - Programmable clock source: system clock or oscillator clock
  - Message buffers may be configured as mailboxes or as FIFO
- Nexus development interface (NDI)
  - Per IEEE-ISTO 5001-2003
  - Real time development support for PowerPC core and eTPU engine through Nexus class 2/1
  - Read and write access (Nexus 3)
  - Support for data value breakpoints / watchpoints
  - Configured via the IEEE 1149.1 (JTAG) port
- IEEE 1149.1 JTAG controller (JTAGC)
  - IEEE 1149.1-2001 Test Access Port (TAP) interface
  - Also supports IEEE 1149.7 Serial JTAG 2 wire interface
  - A 5-bit instruction register that supports IEEE 1149.1-2001 defined instructions

  - A 5-bit instruction register that supports additional public instructions
  - Three test data registers: a bypass register, a boundary scan register, and a device identification register
  - Censorship disable register. By writing the 64 bit serial boot password to this register, Censorship may be disabled till the next reset.
  - A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- On-chip voltage regulator for single 5V supply operation
  - On chip regulator 5V to 3.3V for internal supplies and Nexus interface
  - On chip regulator controller 5V to 1.2V (with external bypass transistor) for core logic
- Low power modes
  - SLOW Mode. Allows device to be run at very low speed (approximately 1MHz), with modules (including the PLL) selectively disabled in software.
  - STOP Mode. System clock stopped to all modules including the CPU. Wake-up timer used to restart the system clock after a predetermined time. Target current 15mA
- Package
  - Available in 144 QFP (20mm x 20mm, 0.5mm pitch), 208 MAPBGA.

3.1 MPC5500/JPC563M family comparison

Table 1. MPC5500/JPC563M family comparison

MPC5500 device	MPC5554 copperhead	MPC5553 mocassin	MPC5534 coral	MPC5565 taipan	MPC5567 tiger	MPC5566 viper	JPC563M60 monaco
Process	130nm	130nm	130nm	130nm	130nm	130nm	90nm
Core	z6	z6	z3	z6	z6	z6	z3
SIMD	Yes	Yes	Yes	Yes	Yes	Yes	Yes
VLE	No	No	Yes	Yes	Yes	Yes	Yes
Cache	32k	8k	No	8k	8k	32k	No
Non maskable interrupt (NMI)	No	No	No	No	No	No	NMI & critical interrupt
MMU	24 entry	24 entry	16 entry	32 entry	32 entry	32 entry	8 entry
xbar	3x5	4x5	4x5	3x5	5x5	4x5	3x4
Windowing software watchdog	No	No	No	No	No	No	Yes
Nexus	3+	3+	3+	3+	3+	3+	2+
SRAM	64k	64k	64k	64k	64k	128k	48k
Flash	2M	1.5M	1M	2M	2M	3M	1M
Flash fetch accelerator	2 x 256 bit	2 x 256 bit	4 x 128 bit	2 x 256 bit	2 x 256 bit	2 x 256 bit	4 x 128 bit
External bus	32 bit	32 bit	16 bit	32 bit	32 bit	32 bit	None

Table 1. MPC5500/JPC563M family comparison (continued)

MPC5500 device	MPC5554 copperhead	MPC5553 moccasin	MPC5534 coral	MPC5565 taipan	MPC5567 tiger	MPC5566 viper	JPC563M60 monaco
Calibration bus	None	None	16 bit	16 bit	16 bit	16 bit	16 bit
DMA	64 channel	32 channel	32 channel	32 channel	32 channel	64 channel	32 channel
DMA Nexus	Class 3	Class 3	None	Class 3	Class 3	Class 3	None
Serial	2	2	2	2	2	2	2
eSCI_A	Yes	Yes	Yes	Yes	Yes	Yes	Yes (MSC uplink)
eSCI_B	Yes	Yes	Yes	Yes	Yes	Yes	Yes (MSC uplink)
CAN	3	2	2	3	5	4	2
CAN_A	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf
CAN_B	64 buf	No	No	64 buf	64 buf	64 buf	No
CAN_C	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf	32 buf
CAN_D	No	No	No	No	64 buf	64 buf	No
CAN_E	No	No	No	No	64 buf	No	No
SPI	4	3	3	3	3	4	2
Microsecond busdownlink	No	No	No	No	No	No	Yes
DSPI_A	Yes	No	No	No	No	Yes	No
DSPI_B	Yes	Yes	Yes	Yes	Yes	Yes	Yes (with LVDS)
DSPI_C	Yes	Yes	Yes	Yes	Yes	Yes	Yes (with LVDS)
DSPI_D	Yes	Yes	Yes	Yes	Yes	Yes	No
FlexRay	No	No	No	No	Yes	No	No
Ethernet	No	Yes	No	No	Yes	Yes	No
System timers	No	No	No	No	No	No	5 PIT chan 4 AutoSAR 1 Watchdog
eMIOS	24 channel	24 channel	24 channel	24 channel	24 channel	24 channel	16 channel
eTPU	64 channel	32 channel	32 channel	32 channel	32 channel	64 channel	32 channel
eTPU_A	Yes	Yes	Yes	Yes	Yes	Yes	Yes (ETPU2)
eTPU_B	Yes	No	No	No	No	Yes	No
Reaction channels	No	No	No	No	No	No	No
Code memory	16k	12k	12k	12k	12k	12k	12k
Data memory	3k	2.5k	2.5	2.5k	2.5k	3k	2.5k

Table 1. MPC5500/JPC563M family comparison (continued)

MPC5500 device	MPC5554 copperhead	MPC5553 moccasin	MPC5534 coral	MPC5565 taipan	MPC5567 tiger	MPC5566 viper	JPC563M60 monaco
Interrupt controller	308 channel	210 channel	210 channel	210 channel	210 channel	308 channel	307 channel
Non-maskable int.	No	No	No	No	No	No	Yes
ADC	40 channel	40 channel	40 channel	40 channel	40 channel	40 channel	32 channel
ADC_A	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ADC_B	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Temp sensor	No	No	No	No	No	No	Yes
Variable gain amp.	No	No	No	No	No	No	Yes
Decimation filter	No	No	No	No	No	No	Yes
Sensor diagnostics	No	No	No	No	No	No	Yes
PLL	FM	FM	FM	FM	FM	FM	FM
VRC	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Supplies	5V, 3.3V	5V, 3.3V	5V, 3.3V	5V, 3.3V	5V, 3.3V	5V, 3.3V	5V
Low power modes	None	None	None	None	None	None	Stop mode Slow mode

4 On-chip modules

The following sections provided detailed information about each of the on-chip modules.

4.1 e200z3 core overview

The e200z3 processor utilizes a four stage pipeline for instruction execution. The Instruction Fetch (stage 1), Instruction Decode/Register file Read/Effective Address Calculation (stage 2), Execute/Memory Access (stage 3), and Register Writeback (stage 4) stages operate in an overlapped fashion, allowing single clock instruction execution for most instructions.

The integer execution unit consists of a 32-bit Arithmetic Unit (AU), a Logic Unit (LU), a 32-bit Barrel shifter (Shifter), a Mask-Insertion Unit (MIU), a Condition Register manipulation Unit (CRU), a Count-Leading-Zeros unit (CLZ), a 32x32 Hardware Multiplier array, result feed-forward hardware, and support hardware for division.

Most arithmetic and logical operations are executed in a single cycle with the exception of the divide instructions. A Count-Leading-Zeros unit operates in a single clock cycle. The Instruction Unit contains a PC incrementer and a dedicated Branch Address adder to minimize delays during change of flow operations. Sequential prefetching is performed to ensure a supply of instructions into the execution pipeline. Branch target prefetching is performed to accelerate taken branches. Prefetched instructions are placed into an instruction buffer capable of holding six instructions.

Branches can also be decoded at the instruction buffer and branch target addresses calculated prior to the branch reaching the instruction decode stage, allowing the branch target to be prefetched early. When a branch is detected at the instruction buffer, a prediction may be made on whether the branch is taken or not. If the branch is predicted to be taken, a target fetch is initiated and its target instructions are placed in the instruction buffer following the branch instruction. Many branches take zero cycle to execute by using branch folding. Branches are folded out from the instruction execution pipe whenever possible. These include unconditional branches and conditional branches with condition codes that can be resolved early.

Conditional branches which are not taken and not folded execute in a single clock. Branches with successful target prefetching which are not folded have an effective execution time of one clock. All other taken branches have an execution time of two clocks. Memory load and store operations are provided for byte, half-word, and word (32-bit) data with automatic zero or sign extension of byte and half-word load data as well as optional byte reversal of data. These instructions can be pipelined to allow effective single cycle throughput. Load and store multiple word instructions allow low overhead context save and restore operations. The load/store unit contains a dedicated effective address adder to allow effective address generation to be optimized. Also, a load-to-use dependency does not incur any pipeline bubbles for most cases.

The condition register unit supports the condition register (CR) and condition register operations defined by the PowerPC architecture. The condition register consists of eight 4-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching. Vectored and autovectored interrupts are supported by the CPU. Vectored interrupt support is provided to allow multiple interrupt sources to have unique interrupt handlers invoked with no software overhead.

The hardware floating-point unit utilizes the IEEE-754 single-precision floating-point format and supports single-precision floating-point operations in a pipelined fashion. The general purpose register file is used for source and destination operands, thus there is a unified storage model for single-precision floating-point data types of 32-bit and the normal integer type. Single-cycle floating-point add, subtract, multiply, compare, and conversion operations are provided. Divide instructions are multi-cycle and are not pipelined.

The Signal Processing Extension (SPE) Auxiliary Processing Unit (APU) provides hardware SIMD operations & supports a full compliment of dual integer arithmetic operation including Multiply Accumulate (MAC) & dual integer multiply (MUL) in a pipelined fashion. The general purpose register file is enhanced such that all 32 of the GPRs are extended to 64 bits wide and are used for source and destination operands, thus there is a unified storage model for 32 x 32 MAC operations which generate greater than 32-bit results.

The majority of both scalar and vector operations (including MAC and MUL) are executed in a single clock cycle. Both Scalar and Vector divides take multiple clocks. The SPE APU also provides extended load and store operations to support the transfer of data to and from the extended 64-bit GPRs. This SPE APU is fully binary compatible with e200z6 SPE APU used in MPC5554 & MPC5553

The CPU includes support for Variable Length Encoding (VLE) instruction enhancements. This allows the classic PowerPC instruction set to be represented by a modified instruction set made up from a mixture of 16-bit and 32-bit instructions. This results in a significantly smaller code size footprint without affecting performance noticeably. The classic PowerPC instruction set and VLE instruction set both available concurrently. Regions of the memory map are designated as PPC or VLE using an additional configuration bit in each of Table Look-aside Buffers (TLB) entries in the MMU.

The CPU core is enhanced by the addition of two additional interrupt sources; Non Maskable Interrupt & Critical Interrupt. These two sources are routed directly from package pins, via edge detection logic in the SIU to the CPU. bypassing completely the Interrupt Controller. Once the edge detection logic is programmed, it can not be disabled, except by reset. The Non Maskable Interrupt is, as the name suggests, completely un-maskable and when asserted will always result in the immediate execution of the respective interrupt service routine. The Non maskable interrupt is not guaranteed to be recoverable. The critical Interrupt is very similar to the Non maskable interrupt, but it can be masked by other exceptional interrupt in the CPU, but is guaranteed to be recoverable (code execution may be resumed from where it stopped).

The CPU core has an additional ‘Wait for Interrupt’ instruction that is used in conjunction with low power STOP mode. When Low Power Stop mode is selected, this instruction is executed to allow the system clock to be stopped. An external interrupt source or the system wake-up timer is used to restart the system clock and allow the CPU to service the interrupt.

4.2 Crossbar

The XBAR multi-port crossbar switch supports simultaneous connections between three master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows for three concurrent transactions to occur from the master ports to any slave port; but each master must access a different slave. If a slave port is simultaneously requested by more than one master port, arbitration logic will select the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port

will be stalled until the higher priority master completes its transactions. Requesting masters will be treated with equal priority and will be granted access to a slave port in 'round robin' fashion, based upon the ID of the last master to be granted access. The crossbar provides the following features:

- Three master ports:
  - e200z3 core complex Instruction port
  - e200z3 core complex Load/Store port
  - eDMA
- Four slave ports
  - Flash
  - calibration bus
  - SRAM
  - Peripheral bridge A/B (eTPU, eMIOS, SIU, DSPI, eSCI, FlexCAN, eQADC, BAM)
- 32-bit internal address, 64-bit internal data paths

4.3 eDMA

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 32 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size. The eDMA module provides the following features:

- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses, transfer size, plus support for enhanced addressing modes
- Transfer control descriptor organized to support two-deep, nested transfer operations
- An inner data transfer loop defined by a "minor" byte transfer count
- An outer data transfer loop defined by a "major" iteration count
- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continuous transfers
  - Peripheral paced hardware requests (one per channel)
- Support for fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
- One interrupt per channel, optionally asserted at completion of major iteration count
- Error termination interrupts are optionally enabled
- Support for scatter/gather DMA processing
- Channel transfers can be suspended by a higher priority channel

4.4 Interrupt controller

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC allows interrupt request servicing from up to 307 interrupt sources (Including 112 sources reserved for compatibility with other family members).

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

Multiple processors can assert interrupt requests to each other through software setable interrupt requests. These same software setable interrupt requests also can be used to break the work involved in servicing an interrupt request into a high priority portion and a low priority portion. The high priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software setable interrupt request to finish the servicing in a lower priority ISR. Therefore these software setable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS. The INTC provides the following features:

- 307 peripheral interrupt request sources
- Eight software setable interrupt request sources
- 9-bit vector addresses
- Unique vector for each interrupt request source
- Hardware connection to processor or read from register
- Each interrupt source can be programmed to one of 16 priorities
- Preemptive prioritized interrupt requests to processor
- ISR at a higher priority preempts executing ISRs or tasks at lower priorities
- Automatic pushing or popping of preempted priority to or from a LIFO
- Ability to modify the ISR or task priority to implement the priority ceiling protocol for accessing shared resources
- Low latency - three clocks from receipt of interrupt request from peripheral to interrupt request to processor

4.5 Frequency modulated PLL (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4MHz to 40MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable.

The PLL has the following major features:

- Input clock frequency from 4MHz to 20 MHz
- Voltage controlled oscillator (VCO) range from 256MHz to 512MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- Three modes of operation
  - Bypass mode with PLL off
  - Bypass mode with PLL running (default mode out of reset)
  - PLL normal mode
- Each of the three modes may be run with a crystal oscillator or an external clock reference
- Programmable frequency modulation
  - Modulation enabled/disabled through software
  - Triangle wave modulation
  - Programmable modulation depth
  - Programmable modulation frequency dependent on reference frequency
- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Clock quality module
  - detects the quality of the crystal clock and cause interrupt request or system reset if error is detected
  - detects the quality of the PLL output clock. If an error is detected, causes a system reset or switches the system clock to the crystal clock and causes an interrupt request.
- Programmable interrupt request or system reset on loss of lock
- Self clocked mode (SCM) operation

4.6 Calibration EBI

The Calibration EBI controls data transfer across the crossbar switch to/from memories or peripherals attached to the VertiCal connector in the calibration address space. The Calibration EBI is only available in the VertiCal Calibration System. The Calibration EBI includes a memory controller that generates interface signals to support a variety of external memories. The Calibration EBI memory controller supports legacy flash, SRAM, and asynchronous memories. In addition, the calibration EBI supports up to 3 regions via chip selects (2 chip selects multiplexed with 2 address bits), along with programmed region-specific attributes. The calibration EBI supports the following features:

- 22-bit address bus (2 most significant signals multiplexed with 2 chip selects)
- 16-bit data bus
- Memory controller with support for various memory types:
  - Asynchronous/legacy flash and SRAM
  - Most standard memories used with the MPC5xx family
- Bus monitor
  - User selectable
  - Programmable time-out period (with 8 external bus clock resolution)

- Configurable wait states (via chip selects)
- Three chip-select (Cal_CS[0], Cal_CS[2:3]) signals (Multiplexed with 2 most significant address signals)
- Two write/byte enable (WE[0:1]/BE[0:1]) signals
- Configurable bus speed modes
  - system frequency
  - 1/2 of system frequency
  - 1/4 of system frequency
- Optional automatic CLKOUT gating to save power and reduce EMI
- Compatible with MPC5xx external bus (with some limitations)
- Selectable drive strengths; 10pF, 20pF, 30pF, 50pF

4.7 SIU

The JPC563M60 SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the RSTOUT pin. The SIU is accessed by the e200z3 core through the crossbar switch. The SIU provides the following features:

- System configuration
  - MCU reset configuration via external pins
  - Pad configuration control
- System reset monitoring and generation
  - Power-on reset support
  - Reset status register provides last reset source to software
  - Glitch detection on reset input
  - Software controlled reset assertion
- External interrupt
  - Sixteen interrupt requests
  - Rising or falling edge event detection
  - Programmable digital filter for glitch rejection
  - Critical Interrupt request
  - Non Maskable Interrupt request
- GPIO
  - GPIO function on 77 I/O pins
  - Virtual GPIO on 64 I/O pins via DSPI serialisation (requires external deserialisation device)
  - Dedicated input and output registers for setting each GPIO pin

- Internal multiplexing
  - Allows serial and parallel chaining of DSPIs
  - Allows flexible selection of eQADC trigger inputs
  - Allows selection of interrupt requests between external pins and DSPI

4.8 ECSM

The error correction status module provides status information regarding platform memory errors reported by error-correcting codes.

4.9 Flash

The JPC563M60 provides 1M bytes of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash module includes a Fetch Accelerator, that optimises the performance of the flash array to match the CPU architecture and provides single cycle random access to the flash @80MHz. The flash module interfaces the system bus to a dedicated flash memory array controller. For CPU 'loads', DMA transfers and CPU instruction fetch, it supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains a four-entry, 128-bit prefetch buffer and a prefetch controller which prefetches sequential lines of data from the flash array into the buffer. Prefetch buffer hits allow no-wait responses. Normal flash array accesses are registered and are forwarded to the system bus on the following cycle, incurring three wait-states. Prefetch operations may be automatically controlled, and are restricted to instruction fetch.

The flash memory provides the following features:

- Supports a 64-bit data bus for instruction fetch, CPU loads and DMA access. Byte, halfword, word and doubleword reads are supported. Only aligned word and doubleword writes are supported.
- Fetch Accelerator
  - Architected to optimise the performance of the flash with the CPU to provide single cycle random access to the flash up to 80MHz system clock speed.
  - Configurable read buffering and line prefetch support.
  - Four line read buffers (128 bits wide) and a prefetch controller
- Hardware and software configurable read and write access protections on a per-master basis.
- Interface to the flash array controller is pipelined with a depth of 1, allowing overlapped accesses to proceed in parallel for interleaved or pipelined flash array designs.
- Configurable access timing allowing use in a wide range of system frequencies.
- Multiple mapping support and mapping based block access timing (0-31 additional cycles) allowing use for emulation of other memory types.
- Software programmable block program/erase restriction control.
- Erase of selected block(s)
- Read page size of 128 bits (4 words)

- ECC with single-bit correction, double-bit detection.
- ECC single bit error corrections are visible to software
- Minimum program size is 2 consecutive 32 bit words, aligned on a 0-modulo-8 byte address, due to ECC.
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Shadow information stored in non volatile shadow block
- Independent program/erase of the shadow block

4.10 SRAM

The JPC563M60 SRAM module provides a general-purpose 64 KByte memory block. The SRAM controller includes these features:

- Supports read/write accesses mapped to the SRAM memory from any master
- 24 KByte block powered by separate supply for standby operation
- Byte, half-word, word and double-word addressable
- ECC performs single bit correction, double bit detection on 32-bit data element

4.11 Memory subsystem access time

Every memory access the CPU performs requires at least 1 system clock cycle for the data phase of the access. Slower memories or peripherals may require additional data phase wait states. Additional data phase wait states may also occur if the slave being accessed, is not 'parked' on the requesting master in the crossbar.

The table below shows the number of additional data phase wait states required for a range of memory accesses.

Table 2. JPC563M60 platform memory access time summary

AHB transfer	Data phase wait states	Description
e200z3 Instruction Fetch	0	FLASH prefetch buffer hit
e200z3 Instruction Fetch	2	FLASH prefetch buffer miss (based on 3-cycle random flash array access time)
e200z3 Data Read	0	RAM read
e200z3 Data Write	0	RAM 32-bit write
e200z3 Data Write	1	RAM 64-bit write (handled as 2 x 32-bit writes)
e200z3 Data Write	1	RAM 8,16-bit write (Read-modify-Write for ECC)
e200z3 Data Flash Read	0	FLASH prefetch buffer hit
e200z3 Data Flash Read	3	FLASH prefetch buffer miss (includes 1-cycle of PFLASH controller arbitration)
e200z3 Peripheral Read	1	Peripheral Bridge read
e200z3 Peripheral Write	1	Peripheral Bridge write

4.12 BAM

The BAM is a block of read-only memory that is programmed once by Freescale. The BAM program is executed every time the MCU is powered-on or reset in normal mode. The BAM supports three different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (a program is downloaded into RAM via eSCI or the FlexCAN and then executed).

The BAM also reads the reset configuration half word (RCHW) from internal flash memory and configures the JPC563M60 hardware accordingly. The BAM provides the following features:

- Sets up MMU to cover all resources and mapping all physical address to logical addresses with minimum address translation
- Sets up the MMU to allow user boot code to execute as either Classic PowerPC Book E code (default) or as Freescale VLE code.
- Detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid
- Supports user programmable 64 bit password protection for serial boot mode
- Supports serial bootloading via FlexCAN bus and eSCI using Freescale protocol
- Supports serial bootloading via FlexCAN bus and eSCI using ST protocol with auto baud rate sensing
- Supports serial bootloading of either Classic PowerPC Book E code (default) or Freescale VLE code
- Supports censorship protection for internal flash memory
- Provides an option to enable the core watchdog timer
- Provides an option to disnable the System watchdog timer

4.13 eMIOS

The eMIOS module provides the functionality to generate or measure events. The JPC563M60 eMIOS implementation is based on the unified channel (UC) module found on MPC5554, MPC5553 & MPC5534, but only implementing a sub-set of the possible channel modes. This architecture, while still providing a consistent user interface, also optimises the timer for cost sensitive applications. These unified channels provide a range of operating mode including the capability to perform dual input capture or dual output compare as well as PWM output.

The eMIOS provides the following features:

- 16 unified channels
- For compatibility with other family members selected channels and timebases are implemented (Reference to MPC5554):
  - Channels 0 - 6, 8 - 15 and 23
  - Timebases A, B and C

- Channels 3, 4, 5, & 6 support modes:-
  - General Purpose Input/Output (GPIO)
  - Single Action Input Capture (SAIC)
  - Single Action Output Compare (SAOC)
- Channels 1, 2, 11 & 13 support all the modes above plus:-
  - Output Pulse Width Modulation Buffered (OPWMB)
- Channels 0, 8, 9, 10, 12, 14, 15, 23 support all the modes above plus:-
  - Input Period Measurement (IPM)
  - Input Pulse Width Measurement (IPWM)
  - Double Action Output Compare {set flag on both matches} (DOAC)
  - Modulus Counter Buffered (MCB)
  - Output Pulse Width & Frequency Modulation Buffered (OPWFMB)
- Unified channel features:
  - 24-bit registers for captured/match values
  - 24-bit internal counter
  - Global prescaler
  - Pin for input/output (Each channel signal is routed to a pin. Most pins are also multiplexed with other signals)
  - Selectable time base
  - Can generate its own time base
- Three 24-bit wide counter buses
  - Counter bus A can be driven by unified channel 23
  - Counter bus B and C are driven by unified channels 0 and 8, respectively
  - Counter bus A can be shared among all unified channels. UCs 0 to 7 and 8 to 15 can share counter buses B and C, respectively
- Shared time bases with the eTPU through the counter buses
- Synchronization among internal and external time bases
- Shadow FLAG register
- State of block can be frozen for debug purposes
- State of block can be frozen for debug purposes

4.14 eTPU2

The eTPU2 is the second generation of the enhanced timing co-processors (ETPU) that were used on the MPC5500 family. ETPU2 is fully upwards compatible with ETPU and will run the same binary code image and can be used with the same tool suite. ETPU2 includes many enhancements to improve efficiency of compilers, functionality, ease of programming and operability; while maintaining the same overall architecture. Some of these enhancements maybe accessible using the same compiler tool chain, while other enhancements will require updates to the compiler before use.

Operating in parallel with the host CPU, the eTPU2 processes instructions and real-time input events, performs output waveform generation, and accesses shared data without host intervention. Consequently, for each timer event, the host CPU setup and service times are minimized or eliminated. A powerful timer subsystem is formed by combining the eTPU2

with its own instruction and data RAM. High-level assembler/compiler and documentation allows customers to develop their own functions on the eTPU2. The eTPU2 supports several features of older TPU versions, making it easy to port older applications. The eTPU2 includes these distinctive features:

- 32 standard channels, each one associated with one input and one output signal.
  - Enhanced input digital filters on the input pins for improved noise immunity.
  - Identical, orthogonal channels: each channel can perform any time function. Each time function can be assigned to more than one channel as a given time, so each signal can have any functionality.
  - Each channel has an event mechanism which supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal and equal-only comparators
  - Input and output signal states visible from the host
  - New programmable channel mode to allow the individual sub-blocks within the channels, to interact together in customer specific configurations. This makes it much easier to use the channel input separately from the channel output.
- Two independent 24-bit time bases for channel synchronization
  - First time base clocked by system clock with programmable prescale division from 1 to 512 (in steps of 2), or external clock pin (New feature - division by 1)
  - Second time base clocked by system clock with programmable prescale division from 8 to 512 (in steps of 8), or external clock pin
  - Second time base counter can work as an angle counter, enabling angle based applications to match angle instead of time.
  - Both timebases visible from the host
- Event triggered microengine:
  - 32 bit fixed length instruction execution in two system clock cycle
  - 12k bytes of code memory (SCM)
  - 2.5k bytes of shared parameter (data) RAM (SPRAM)
  - Parallel execution of data memory, ALU, channel control and flow control subinstructions in selected combinations
  - 32 & 24 bit wide microengine and ALU, with 2 system clock cycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single bit manipulation, shift operations, sign extension and conditional execution
  - 24 bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands
  - New ‘engine relative’ addressing mode to better support ‘C’ compiler
- Resource sharing features support channel use of common channel registers, memory and microengine time:
  - Hardware scheduler works as a “task management” unit, dispatching event service routines by pre-defined, host-configured priority.
  - Automatic channel context switch when a “task switch” occurs, i.e., one function thread ends and another begins to service a request from other channel: channel

specific registers, flags and parameter base address are automatically loaded for the next serviced channel

  - SPRAM shared between host CPU and eTPU, supporting communication either between channels and host or inter-channel
  - Dual-parameter coherency hardware support allows atomic access to two parameters by host
  - Enhancements to DMA & Interrupt structure to allow any channel to assert any interrupt source or DMA trigger.
- Test and development support features:
  - IEEE-ISTO 5001-2003 standard class 1 compliant for the eTPU (Nexus)
  - SCM continuous signature-check built-in self test (MISC - multiple input signature calculator), runs concurrently with eTPU normal operation

4.15 eQADC

The enhanced queued analog to digital converter (eQADC) block provides accurate and fast conversions for a wide range of applications. The eQADC provides a parallel interface to a single on-chip analog to digital converters (ADC), and a single master to single slave serial interface to an off-chip external device. The on-chip ADCs are architected to allow access to all the analog channels.

The eQADC prioritises and transfers commands from six command conversion command ‘queues’ to the on-chip ADCs or to the external device. The block can also receive data from the on-chip ADCs or from an off-chip external device into the six result queues, in parallel, independently of the command queues. The 6 command queues are prioritised with Queue_0 having the highest priority and Queue_6 the lowest. Queue_0 also has the added ability to bypass all buffering and queuing and abort a currently running conversion on either ADC and start a Queue_0 conversion. This means that Queue_0 will always have a deterministic time from trigger to start of conversion, irrespective of what tasks the ADCs were performing when the trigger occurred. The eQADC supports software and external hardware triggers from other blocks to initiate transfers of commands from the queues to the on-chip ADCs or to the external device. It also monitors the fullness of command queues and result queues, and accordingly generates DMA or interrupt requests to control data movement between the queues and the system memory, which is external to the eQADC.

The ADCs also support features designed to allow the direct connection of high impedance acoustic sensors that might be used in a system for detecting engine knock. These features include differential inputs; integrated variable gain amplifiers for increasing the dynamic range; programmable pull-up & pull-down resistors for biasing and sensor diagnostics.

The eQADC also integrates a programmable decimation filter capable to taking in ADC conversion results at a high rate, passing them through a hardware low pass filter, then down-sampling the output of the filter and feeding the lower sample rate results to the result FIFOs. This allows the ADCs to sample the sensor at a rate high enough to avoid aliasing of out-of-band noise; while providing a reduced sample rate output to minimise the amount DSP processing bandwidth required to fully process the digitised waveform.

The eQADC provides the following features:

- Dual On-chip ADCs.
  - 2 x 12 Bit ADC resolution
  - Programmable resolution for increased conversion speed (12 bit, 10 bit, 8 bit)
    - 12 bit conversion time - 1uS (1M sample/sec.)
    - 10 bit conversion time - 867nS (1.2M sample/second)
    - 8 bit conversion time = 733nS (1.4M sample/second)
  - Up to 10 bit accuracy at 500 KSample/s and 8 bit accuracy at 1 MSample/s
  - Differential conversions
  - Single-ended signal range from 0 to 5V
  - Variable gain amplifiers on all inputs (x1, x2, x4)
  - Sample times of 2 (default), 8, 64 or 128 ADC clock cycles
  - Provides time stamp information when requested
  - Parallel interface to eQADC CFIFOs and RFIFOs
  - Supports both right-justified unsigned and signed formats for conversion results
- 32 input channels (accessible by both ADCs)
- 8 additional internal channels for measuring control and monitoring voltages inside the device
  - Including Core voltage, IO voltage, LV voltages, etc.
- 4 pairs of differential analog input channels
  - Programmable pull-up/pull-down resistors on each differential input
- Silicon die temperature sensor
  - provides temperature of silicon as an analogue value
  - read using an internal ADC analogue channel
  - may be read with either ADC
- Decimation filter
  - Programmable decimation factor (2 to 16)
  - Selectable IIR or FIR filter
  - Up to 4th order IIR or 8th order FIR
  - Programmable coefficients
  - Saturated or non-saturated modes
  - Programmable Rounding (Convergent; Two's Complement; Truncated)
  - Pre-fill mode to pre-condition the filter before the sample window opens
- Full duplex synchronous serial interface to an external device
  - Free-running clock for use by an external device
  - Supports a 26-bit message length

- Priority based queues
  - Supports six queues with fixed priority. When commands of distinct queues are bound for the same ADC, the higher priority queue is always served first
  - Queue_0 can bypass all prioritisation, buffering and abort current conversions to start a Queue_0 conversion a deterministic time after the queue trigger.
  - Supports software and hardware trigger modes to arm a particular queue
  - Generates interrupt when command coherency is not achieved
- External hardware triggers
  - Supports rising edge, falling edge, high level and low level triggers
  - Supports configurable digital filter
- Supports 4 external 8-to-1 muxes which can expand the input channels to 56 channels total.

4.16 DSPI

The deserial serial peripheral interface (DSPI) block provides asynchronous serial interface for communication between the JPC563M60 MCU and external devices. The DSPI supports pin count reduction through serialization and deserialization of eTPU channels and memory-mapped registers. The channels and register content are transmitted using a SPI-like protocol. There are two identical DSPI blocks on the JPC563M60 MCU. The DSPI pins support 5V logic levels or Low Voltage Differential Signalling (LVDS) to improve high speed operation.

The DSPIs have four configurations:

- Serial peripheral interface (SPI) configuration where the DSPI operates as a SPI with support for queues
- Deserial serial interface (DSI) configuration where the DSPI serializes eTPU output channels and deserializes the received data by placing it on the eTPU input channels
- Combined serial interface (CSI) configuration where the DSPI operates in both SPI and DSI configurations interleaving DSI frames with SPI frames, giving priority to SPI frames
- Enhanced deserial serial interface (DSI) configuration where DSPI serializes up to 32bits with 3 possible sources per bit
  - eTPU, eMIOS, new 32bit output port as possible bit source
  - programmable inter-frame gap in continuous mode
  - bit source selection allows microsecond bus downlink with command or data frames up to 32bits
- 5V logic levels or LVDS for data and clock signals

For queued operations, the SPI queues reside in system memory external to the DSPI. Data transfers between the memory and the DSPI FIFOs are accomplished through the use of the eDMA controller or through host software.

4.17 eSCI

The enhanced serial communications interface (eSCI) allows asynchronous serial communications with peripheral devices and other MCUs. It includes special support to

interface to local interconnect network (LIN) slave devices. The eSCI block provides the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection
- Programmable 8-bit, 9-bit, 12-bit, 13-bit data format
- Automatic parity generation
- LIN support
  - Autonomous transmission of entire frames
  - Configurable to support all revisions of the LIN standard
  - Automatic parity bit generation
  - Double stop bit after bit error
  - 10 or 13-bit break support
- Separately enabled transmitter and receiver
- Programmable transmitter output parity
- Two receiver wake up methods, idle line and address mark
- Interrupt-driven operation with flags
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection
- DMA support for both transmit and receive data
  - Global error bit stored with receive data in system RAM to allow post processing of errors

4.18 FlexCAN

The JPC563M60 MCU contains two controller area network (FlexCAN) blocks. The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. FlexCAN module contains 32 message buffers (MB) for CANa and 64 message buffers for CANc.

The FlexCAN module provides the following features:

- Based on and including all existing features of the Freescale TouCAN module
- Full Implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - Zero to eight bytes data length
  - Programmable bit rate up to 1 Mb/s
- Content-related addressing
- 32 or 64 message buffers of zero to eight bytes data length
- Each MB configurable as Rx or Tx, all supporting standard and extended messages

- Message buffers configurable as mailboxes or as FIFO
- Includes 1056 / 528 bytes of embedded memory for MB storage
- Programmable loop-back mode supporting self-test operation
- Three programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- Multi master concept
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode, with programmable wake up on bus activity

4.19 System timer

The system timers provide two distinct types of system timer:- periodic interrupts/triggers using the Peripheral Interrupt Timer (PIT); and operating system task monitors using the System Timer Module (STiM). The PIT provides 5 independant timer channels, capable of producing periodic interrupts and periodic triggers. The PIT has no external input or output pins; and is intended to be used to provide system 'tick' signals to the operating system, aswell as periodic triggers for eQADC queues. Of the 5 channels in the PIT, 4 are clocked by the system clock, 1 is clocked by the crystal clock. This one channel is also refered to as Real Time Interrupt (RTI) and is used to wakeup the device from low power stop mode. The System Timer Module (STiM) is designed to implemented the software task monitor as defined by AutoSAR. It consists of a single 32 bit counter, clocked by the system clock, and 4 independant timer comparators. These comparators produce a CPU interrupt when the timer exceeds the programmed value.

The following features are implemented in the PIT:

- 5 independent timer channels
- Each channel includes 32 bit wide down counter with automatic reload
- 4 channels clocked from system clock
- 1 channel clocked from crystal clock (wake-up timer)
- Wake-up timer remains active when System STOP mode is entered. Used to restart system clock after predefined time-out period
- Each channel can optionally generate interrupt request when timer reaches zero
- 4 channels can optionally produce trigger event when timer reaches zero (used to trigger eQADC queues)

The following features are implemented in the STiM:-

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

4.20 System software watchdog

The system software watchdog is a second watchdog module to compliment the standard PowerPC watchdog integrated in the CPU core. The system software watchdog is a 32 bit modulus counter clocked by the system clock that can provide a system reset or interrupt request, when the correct software key is not written within the required time window.

The following features are implemented:

- 32 bit modulus counter
- clocked by system clock
- 25% - 100% watchdog window
- Can optionally cause system reset or interrupt request on time-out
- Reset by writing a software key to memory mapped register
- Enabled out of reset
- Configuration is protected by a software key or a write-once register

4.21 Nexus

The NDI (Nexus Debug Interface) block provides real-time development support capabilities for the JPC563M60 PowerPC-based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI block is an integration of several individual Nexus blocks that are selected to provide the development support interface for the JPC563M60. The NDI block interfaces to the host processor, eTPU, and internal buses to provide development support as per the IEEE-ISTO 5001-2003 standard. The development support provided includes program trace & run-time access to the MCUs internal memory map and access to the PowerPC and eTPU internal registers during halt. The Nexus interface also supports a JTAG only mode using only the JTAG pins. The following features are implemented:

- 5 pin JTAG port (JCOMP, TDI, TDO, TMS, and TCK)
  - Always available in production package (no alternate function)
  - Supports JTAG mode
  - 3.3V interface
  - Supports Nexus class 1 features
  - Supports Nexus class 3 read/write feature
- 3 pin Serial JTAG port (JCOMP, TMS & TCK)
  - Optional replacement of 5 pin JTAG port above
  - 2 unused JTAG pins may be used as IO
  - Complies with IEEE 1149.7 Serial JTAG specification
- 9 pin Reduce Port interface in 144 QFP production package
  - Alternate function as IO
  - 5V or 3.3V interface

  - Auxiliary output port
    - 1 MCKO (message clock out) pin
    - 4 MDO (message data out) pins
    - 2 $\overline{\text{MSEO}}$ (message start/end out) pins
    - 1 $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port
    - 1 $\overline{\text{EVTI}}$ (event in) pin
- 17 pin full port interface in VertiCal calibration package
  - 3.3V interface
  - Auxiliary output port
    - 1 MCKO (message clock out) pin
    - 4 or 12 MDO (message data out) pins (8 extra full port pins shared with calibration bus)
    - 2 $\overline{\text{MSEO}}$ (message start/end out) pins
    - 1 $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port
    - 1 $\overline{\text{EVTI}}$ (event in) pin
- Host processor (e200) development support features
  - IEEE-ISTO 5001-2003 standard class 2 compliant
  - Program trace via branch trace messaging (BTM). Branch trace messaging displays program flow discontinuities (direct branches, indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus, static code may be traced.
  - Watchpoint trigger enable of program trace messaging
  - Data value breakpoints. Allows CPU to be halted when the CPU write a specific value to a memory location
    - 4 data value breakpoints
    - CPU only
    - Detects “equal” & “not equal”
    - Byte, half word, word (naturally aligned)
    - Imprecise due to CPU pipelining
  - Subset of PowerPC Book E software debug facilities with OnCE block (Nexus class 1 features)
- eTPU development support features
  - IEEE-ISTO 5001-2003 standard class 1 compliant for the eTPU
  - Nexus based breakpoint configuration and single step support.
- Run-time access to the on-chip memory map via the Nexus read/write access protocol. This feature supports accesses for run-time internal visibility, calibration variable acquisition, calibration constant tuning, and external rapid prototyping for powertrain automotive development systems.
- All features are independently configurable and controllable via the IEEE 1149.1 I/O port.
- Power-on-reset status indication during reset via MDO[0] in disabled and reset modes

4.22 JTAG

The JTAGC (JTAG Controller) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 and IEEE 1149.7 standards, and supports the following features:

- IEEE 1149.1-2001 Test Access Port (TAP) interface 4 pins (TDI, TMS, TCK, and TDO)
- IEEE 1149.7 Serial JTAG Test Access Port interface 2 pins (TMS, TDO)
- JTAG may operate in either 4 pins mode or 2 pins mode
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD, HIGHZ, CLAMP
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC, ACCESS_AUX_TAP_ONCE, ACCESS_AUX_TAP_eTPU
- Three test data registers: a bypass register, a boundary scan register, and a device identification register. The size of the boundary scan register is parameterized to support a variety of boundary scan chain lengths
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- Censorship inhibit register.
  - 64 bit Censorship password register
  - If the external tool writes a 64 bit password that matches the Serial Boot password stored in the internal flash shadow row, Censorship is disabled until the next system reset

5 LQFP144 pin-out diagram

LQFP144 pin out

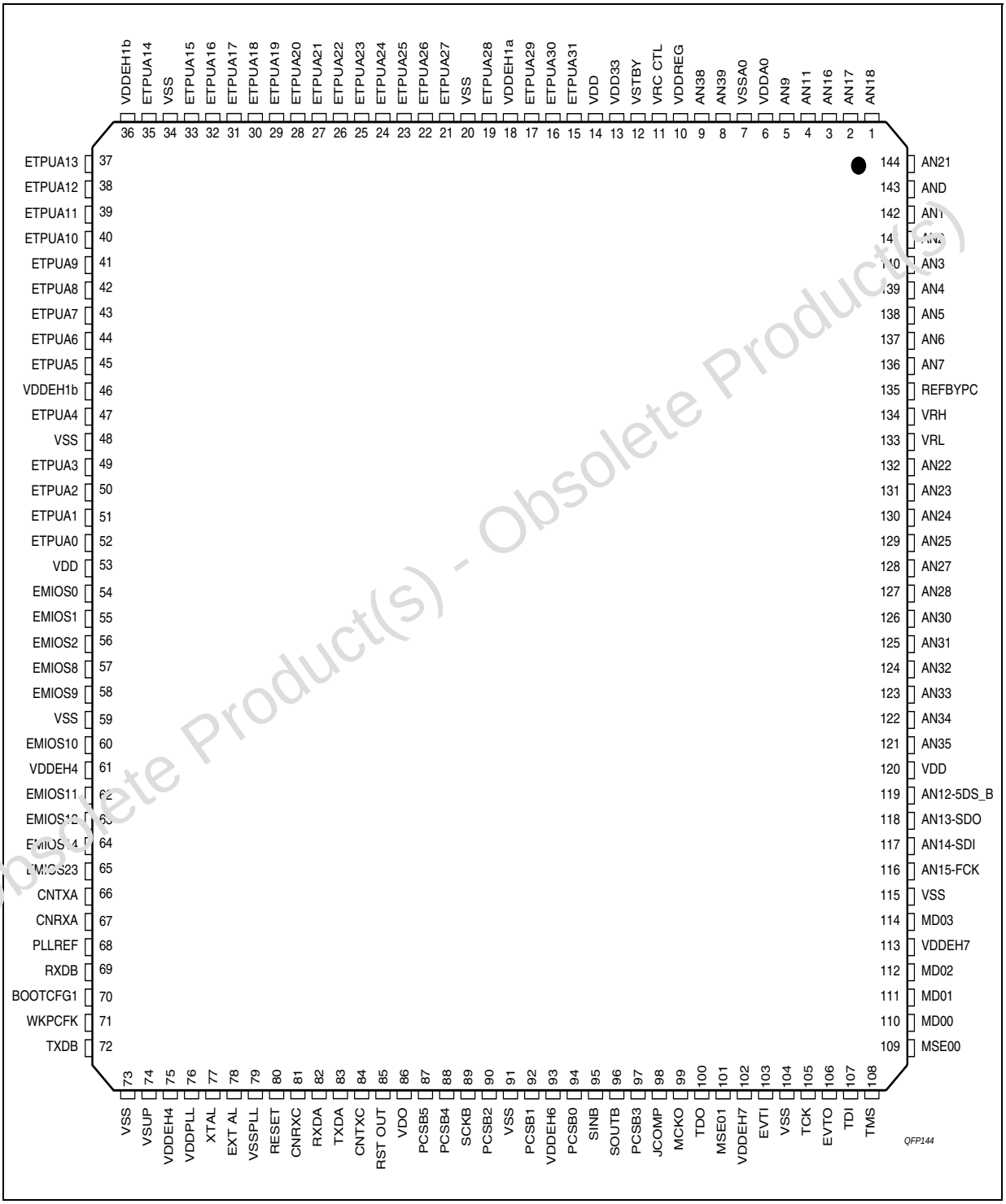


Table 3. Pin description of the LQFP144 device

Pin number	Primary function name	Primary function description	Alternate function name	Second alternate function name
1	AN 18	Single Ended Analog Input		
2	AN 17	Single Ended Analog Input		
3	AN16	Single Ended Analog Input		
4	AN11	Single Ended Analog Input	ANZ	
5	AN9	Single Ended Analog Input	ANX	
6	VDDAO	Analogue 5V Supply		
7	VSSA0	Analogue Ground		
8	AN 39	Single Ended Analog Input	ANY	AN10
9	AN 38	Single Ended Analog Input	ANW	AN8
10	VDDREG	Voltage Regulator Control Supply		
11	VRCCTL	voltage Regulator Control Output		
12	VSTBY	SRAM Standby Power Input		
13	VDD33	Internal 3.3V Supply		
14	VDD	Internal Logic Supply Input		
15	ETPUA31	eTPU_A Channel	PCSC4	ETPUA13
16	ETPUA30	eTPU_A Channel	PCSC3	ETPUA11
17	ETPUA29	eTPU_A Channel	PCSC2	
18	VDDEH1a	External 10 Supply Input		
19	ETPUA28	eTPU A Channel	PCSC1	
20	VSS	Ground		
21	ETPUA27	eTPU A Channel	IRQ15	SOUTC LVDS-
22	ETPUA26	eTPU_A Channel	IR011	SOUTC_LVDS+
23	ETPUA25	eTPU A Channel	IRQ13	SCKC LVDS-
24	ETPUA24	eTPU A Channel	IRQ12	SCKC LVDS+
25	ETPUA23	eTPU A Channel	IRQ11	ETPUA21
26	ETPUA22	eTPU A Channel	IRQ10	ETPUA17
27	ETPUA21	eTPU A Channel	IRQ9	
28	ETPUA20	eTPU A Channel	IRQ8	
29	ETPUA19	eTPU_A Channel		
30	ETPUA18	eTPU A Channel		
31	ETPUA17	eTPU A Channel		
32	ETPUA16	eTPU A Channel		
33	ETPUA15	eTPU_A Channel	PCSB5	

Table 3. Pin description of the LQFP144 device (continued)

Pin number	Primary function name	Primary function description	Alternate function name	Second alternate function name
34	VSS	Ground		
35	ETPUA14	eTPU A Channel	PCSB4	ETPUA9
36	VDDEH1b	External I/O Supply Input		
37	ETPUA13	eTPU_A Channel	PCSB3	
38	ETPUA12	eTPU_A Channel	PCSB1	
39	ETPUA11	eTPU_A Channel	ETPUA23	
40	ETPUAI0	eTPU_A Channel	ETPUA22	
41	ETPUA9	eTPU_A Channel	ETPUA21	
42	ETPUA8	eTPU_A Channel	ETPUA20	SOUTB LVDS-
43	ETPUA7	eTPU_A Channel	ETPUA19	SOUTB LVDS+ETPU6
44	ETPUA6	eTPU_A Channel	ETPUA18	SCKB LVDS-
45	ETPUA5	eTPU_A Channel	ETPUA17	SCKB LVDS+
46	VDDEH1b	External I/O Supply Input		
47	ETPUA4	eTPU_A Channel	ETPUA16	
48	VSS	Ground		
49	ETPUA3	eTPU_A Channel	ETPUA15	
50	ETPUA2	eTPU_A Channel	ETPUA14	
51	ETPUA1	eTPU_A Channel	ETPUA13	
52	ETPUA0	eTPU_A Channel	ETPUA12	ETPUA19
53	VDD	Internal Logic Supply Input		
54	EMIOS0	eMIOS Channel	ETPUA0	ETPUA25
55	EMIOS1	eMIOS Channel	ETPUA1	
56	EMIOS2	eMIOS Channel	ETPUA2	
57	EMIOS8	eMIOS Channel	ETPUA8	
58	EMIOS9	eMIOS Channel	ETPUA9	
59	VSS	Ground		
60	EMIOS10	eMIOS Channel		
61	VDDEH4	External I/O Supply Input		
62	EMIOS11	eMIOS Channel		
63	EMIOS12	eMIOS Channel	SOUTC	ETPUA27
64	EMIOS14	eMIOS Channel	IRQ0	ETPUA29
65	EMIOS23	eMIOS Channel		

Table 3. Pin description of the LQFP144 device (continued)

Pin number	Primary function name	Primary function description	Alternate function name	Second alternate function name
66	CNTXA	CAN_A Transmit	TXDA	
67	CNRXA	CAN_A Receive	RXDA	
68	PLLREF	PLL Mode Selection	IRQ4	ETRIG0
69	RXDB	SCI_B Receive		
70	BOOTCFG1	Boot Configuration Inpt	IRQ3	ETRIG1
71	WKPCFK	Weak Pull Configuration Input	NMI	
72	TXDB	SCI_B Transmit		
73	VSS	Ground		
74	VSUP	Ground		
75	VDDEH4	External I/O Supply Input		
76	VDDPLL	Clock Synthesizer Power Input		
77	XTAL	Crystal Oscillator Out mt		
78	EXTAL	G stal Oscillator In put		
79	VSSPLL	Clock Synthesizer Ground Input		
80	RESET	External Reset Input		
81	CNRXC	CAN C Receive		
82	RXDA	SCI _A Receive	EMIOS15	
83	TXDA	SCI A Transmit	EMIOS13	
84	CNTXC	CAN C Transmit		
85	RSTOUT	External Reset Output		
86	VDD	Internal Logic Supply Input		
87	PCSB5	DSPI B Peripheral Chip Select	PCSCO	
88	PCSB4	DSPI B Peripheral Chip Select	SCK C	
89	SCKB	DSPI B Clock	PCSC1	
90	PCSB2	DSPI B Peripheral Chip Select	SOUTC	
91	VSS	Ground		
92	PCSB1	DSPI B Peripheral Chip Select		
93	VDDEH6	External I/O Supply Input		
94	PCSBO	DSPI B Peripheral Chip Select		
95	SINB	DSPI B Data In put	PCSC2	
96	SOUTB	DSPI B Data Output	PCSC5	
97	PCSB3	DSPI B Peripheral Chip Select	SINC	
98	JCOMP	JTAG TAP Controller Enable		

Table 3. Pin description of the LQFP144 device (continued)

Pin number	Primary function name	Primary function description	Alternate function name	Second alternate function name
99	MCKO	Nexus Message Clock Out	CLKOUT	OSCCLK
100	TDO	JTAG Test Data Output	EMIOS6	
101	MSE01	Nexus Message Stan End Out	ETPUA29	
102	VDDEH7	External I/O Supply Input		
103	EVTI	Nexus Event In	ETPUA2	
104	VSS	Ground		
105	TCK	JTAG Test Clock Input		
106	EVTO	Nexus Event Out	ETPUA4	
107	TDI	JTAG Test Data Input	EMIOS5	
108	TM S	JTAG Test Mode Select Input		
109	61SE00	Nexus Message Stan End Out	ETPUA27	
110	61D00	Nexus Message Data Out	ETPUA13	
111	61D01	Nexus Message Data Out	ETPUA19	
112	61D02	Nexus Message Data Out	ETPUA21	
113	VDDEH7	External I/O Supply Input		
114	61D03	Nexus Message Data Out	ETPUA25	
115	VSS	Ground		
116	AN15-FCK	Single Ended Analog Input	ETPUA29	
117	AN14-SDI	Single Ended Analog Input	ETPUA27	
118	AN13-SDO	Single Ended Analog Input	ETPUA21	
119	AN12-SDS B	Single Ended Analog Input	ETPUA19	
120	VDD	Internal Logic Supply Input		
121	AN35	Single Ended Analog Input		
122	AN 34	Single Ended Analog Input		
123	AN33	Single Ended Analog Input		
124	AN32	Single Ended Analog Input		
125	AN31	Single Ended Analog Input		
126	AN30	Single Ended Analog Input		
127	AN28	Single Ended Analog Input		
128	AN27	Single Ended Analog Input		
129	AN25	Single Ended Analog Input		
130	AN24	Single Ended Analog Input		
131	AN23	Single Ended Analog Input		

Table 3. Pin description of the LQFP144 device (continued)

Pin number	Primary function name	Primary function description	Alternate function name	Second alternate function name
132	AN22	Single Ended Analog Input		
133	VRL	Voltage Reference Low		
134	VRH	Voltage Reference High		
135	REFBYPC	B pass Capacitor In put		
136	AN7	Single Ended Analog Input		
137	AN6	Single Ended Analog Input		
138	AN5	Single Ended Analog Input		
139	AN4	Single Ended Analog Input		
140	AN3	Single Ended Analog Input		
141	AN2	Single Ended Analog Input		
142	AN1	Single Ended Analog Input		
143	AN0	Single Ended Analog Input		
144	AN21	Single Ended Analog Input		

6 Documentation

Table 4 lists other documents that provide information related to the JPC563M60 and its development support tools. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, the Freescale literature distribution center, or through the Freescale world-wide web address at http://www.freescale.com

Table 4. JPC563M60 and related documentation

Freescale document number	Title	Revision	Status
JPC563M60RM	JPC563M60 reference manual	N/A	TBD
AN2706/D	EMC guidelines for MPC5500 based systems	2004	Available
AN1259/D	System design and layout techniques for noise reduction in MCU Based Systems	1995	Available
AN2613	MPC5554 minimum board configuration	Revision 0	Available
AN2614	Nexus interface options for the MPC5500 family	Revision A	Available

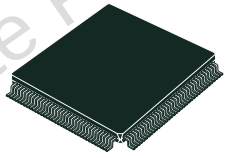
7 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

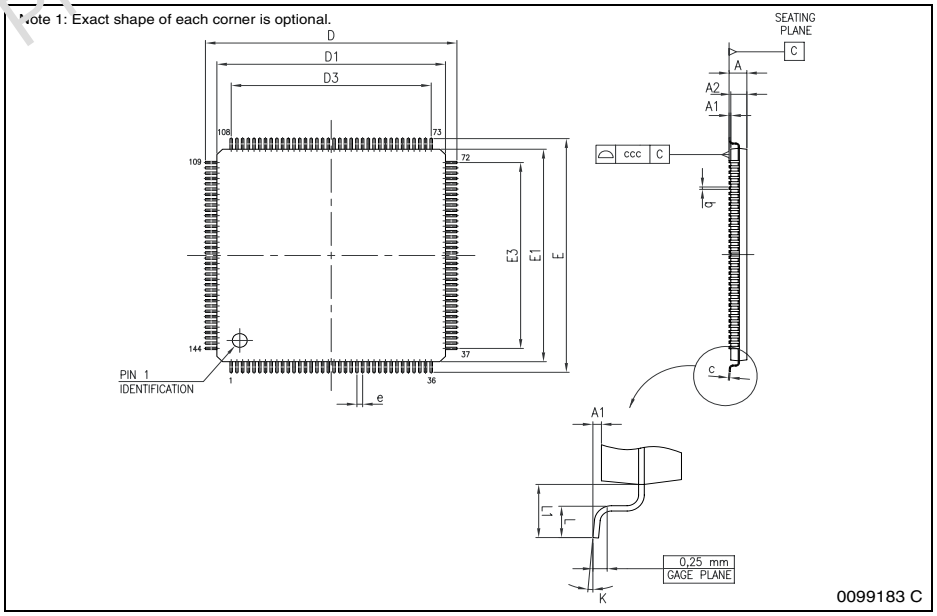
Figure 2. LQFP144 mechanical data and package dimension

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3		17.500			0.6890	
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3		17.500			0.6890	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0° (Min.); 3.5° (Typ.); 7° (Max.)					
ccc			0.080			0.0031

OUTLINE AND MECHANICAL DATA



LQFP144 (20x20x1.40mm)



8 Revision history

Table 5. Document revision history

Date	Revision	Changes
05-Apr-2007	1	Initial release.
05-Apr-2007	2 - 3	N/A(1)
10-Apr-2007	4	Version alignment with external documents.

1. Revision history for versions 2 and 3 are not available, due to a targeted version alignment procedure.