SPC570S40E1, SPC570S40E3 SPC570S50E1, SPC570S50E3

32-bit Power Architecture® microcontroller for automotive ASILD Chassis & Safety applications

Data brief

eTQFP100 (14 x 14 x 1.0 mm)   eTQFP64 (10 x 10 x 1.0 mm)

Features

- Features
  - High performance e200z0h dual core
  - 32-bit Power Architecture technology CPU
  - Core frequency as high as 80 MHz
  - Single issue 4-stage pipeline in-order execution core
  - Variable Length Encoding (VLE)
- Up to 544 KB (512 KB code + 32 KB data, suitable for EEPROM emulation) on-chip flash memory: supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- Up to 48 KB on-chip general-purpose SRAM
- Multi-channel direct memory access controller (eDMA) with 16 channels
- Comprehensive new generation ASILD safety concept
  - Safety of bus masters (core+INTC, DMA) by delayed lockstep approach
  - Safety of storage (Flash, SRAM) by mainly ECC
  - Safety of the data path to storage and periphery by mainly End-to-End EDC (E2E EDC)
  - Clock and power, generation and distribution, supervised by dedicated monitors
  - Fault Collection and Control Unit (FCCU) for collection and reacRev 4tion to failure notifications
  - Memory Error Management Unit (MEMU) for collection and reporting of error events in memories
  - Boot time MBIST and LBIST for latent faults

- Check of safety mechanisms availability and error reaction path functionality by dedicated mechanisms
- Safety of the periphery by application-level measures supported by replicated peripheral bridges and by LBIST
- Safety of the periphery by application-level measures supported by replicated peripheral bridges and by LBIST
- Further measures on dedicated peripherals (e.g. ADC supervisor)
- Junction temperature sensor
- 8-region system memory protection unit (SMPU) with process ID support (tasks isolation)
- Enhanced SW watchdog
- Cyclic redundancy check (CRC) unit
- Dual phase-locked loops with stable clock domain for peripherals and FM modulation domain for computational shell
- Nexus Class 3 debug and trace interface
- Communication interfaces
  - 2 LINFlexD modules
  - 3 deserial serial peripheral interface (DSPI) modules
  - Up to 2 FlexCAN interfaces with 32 message buffers each
- On-chip CAN/UART Bootstrap loader with Boot Assisted Flash (BAF). Physical Interface (PHY) can be
  - UART
  - CAN
- Two enhanced 12-bit SAR analog converters
  - 1.5 µs conversion time
  - 16 physical channels (fully shared between the 2 SARADC units)
  - Supervisor ADC concept
  - Programmable Cross Triggering Unit (CTU)
- Single 3.3 V or 5V voltage supply
- 4 general purpose eTimer units (6 channels each)
- Junction temperature range –40 °C to 150 °C

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1.1   Document overview

This document provides an overview and describes the features of the SPC570Sx series of microcontroller units (MCUs). For functional characteristics, refer to the device reference manual. For electrical specifications, pin assignments, and package diagrams, refer to the device datasheet.

1.2   Description

The 32-bit SPC570Sx automotive microcontrollers, (ASIL-D compliant) are a family of system-on-chip (SoC) devices designed to meet the challenges of the next generation of entry-level vehicle safety critical applications such as ABS and Airbag.

The SPC570Sx microcontrollers operate at speeds up to 80 MHz and offer high performance processing with low power consumption. They are compatible with the existing development infrastructure of current Power Architecture® devices and are supported with software drivers, operating systems and configuration code to assist with application development.

2   Block diagram

Figure 1 shows the top-level block diagram.

Figure 1. Family Superset block diagram

GAPG2901151032RI
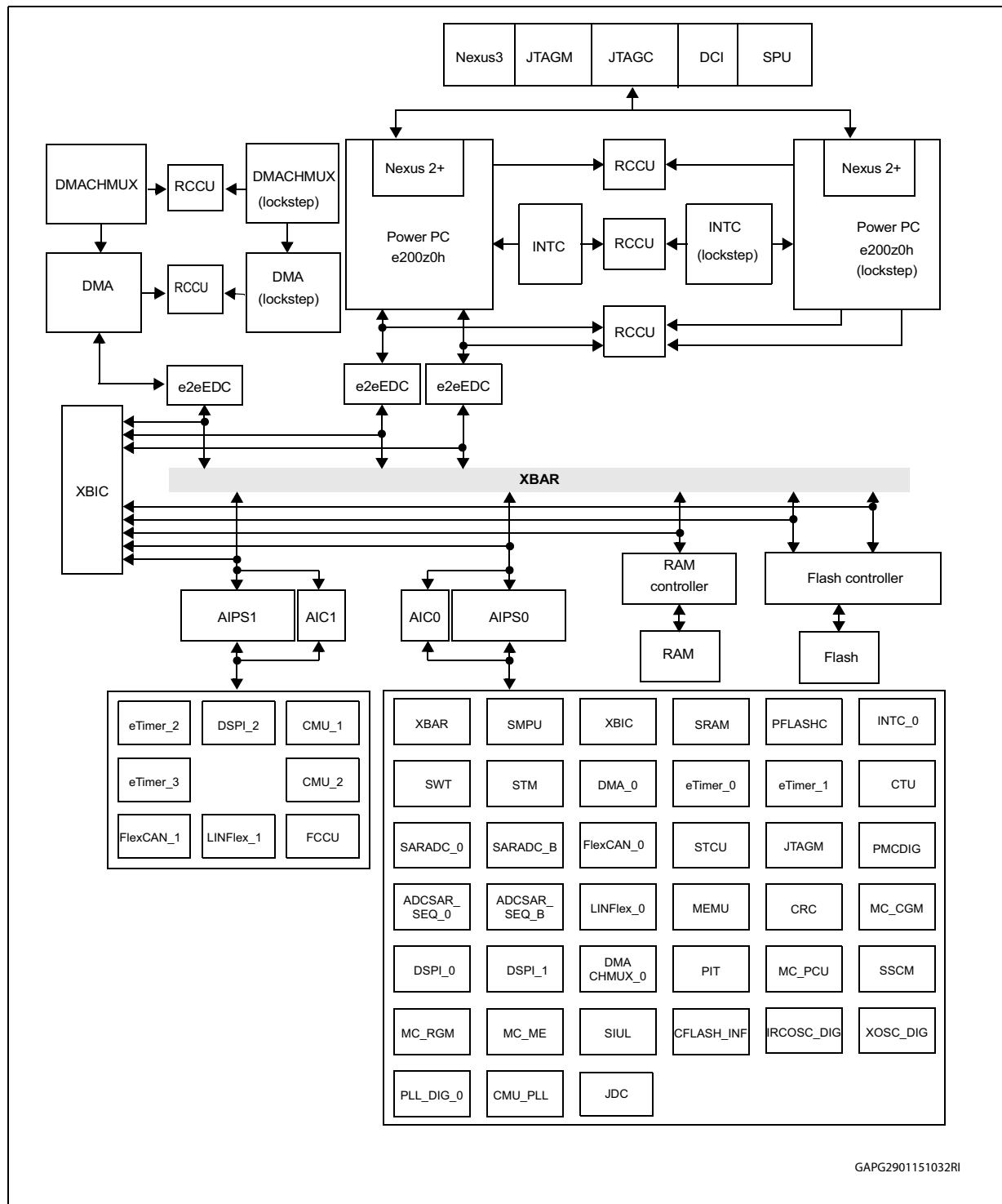
3 SPC570Sx family overview

3.1 Introduction

The following sections provide high-level descriptions of the features found on the SPC570Sx family of devices.

3.2 Device summary

Table 1. SPC570Sx device feature summary (Family Superset Configuration)

Feature		Description
Process		55 nm
Main processor	Core	e200z0h
	Number of main cores	1
	Number of checker cores	1
	VLE	Yes
	Main processor frequency	80 MHz[1]
Interrupt controllers		2 (one in lockstep)
Software watchdog timer		1
System timers		1 AUTOSAR® STM 1 PIT with four 32-bit channels
DMA channels		2 x 16
SMPU		Yes (8 regions)[2]
System SRAM		48 KB
Code flash memory		512 KB
Data flash memory (suitable for EEPROM emulation)		32 KB
UTEST flash memory		8 KB
Boot assist flash (BAF)		8 KB
CRC		1
LINFlexD		2
FlexCAN		2
DSPI		3
eTimer		4 x 6 channels
ADC (SAR)		2[3]
CTU (Cross Triggering Unit)		1
Temperature sensor		1
Self-test control unit (memory and logic BIST)		1
FCCU		1

Table 1. SPC570Sx device feature summary (Family Superset Configuration)

Feature		Description
MEMU		1
PLL		Dual PLL with FM
Nexus		3[4]
Sequence processing unit (SPU)		1
External power supplies		5 V[5] 3.3 V[5]
Junction temperature		−40 to 150 °C
Packages	Device SPC570SxxE3	eTQFP100
	Device SPC570SxxE1	eTQFP64

1. Includes user programmable CPU core and one safety core. The two e200z0h processors in the lockstep pair run at 80 MHz. The e200z0h is compatible with the Power Architecture embedded specification.

2. SMPU with process ID support extension

3. One ADC can be used as supervisor ADC

4. Including trace for the crossbar masters (data & instruction trace on core and data trace on eDMA). 4 MDO pin Nexus trace port

5. All I/Os can be supplied at 3.3 V or 5 V (mutually exclusive)

Table 2. SPC570S40Ex, SPC570S50Ex device configuration differences

	SPC570S40 (full option configuration)	SPC570S50 (full option configuration)
Flash	256 KB[1]	512 KB
RAM	32 KB[2]	48 KB
CAN	1[3]	2
Others	aligned to the *SPC570Sx device feature summary (Family Superset Configuration)* described in *Table 1*	

1. Flash blocks excluded on SPC570S40:
 128K Block 0 [0x0100_0000 … 0x0101_FFFF]
 128K Block 1 [0x0102_0000 … 0x0103_FFFF]

2. SRAM area excluded on SPC570S40
 [0x4000_8000…0x4000_BFFF]

3. FlexCAN1 excluded on SPC570S40

3.3 Detailed feature list

- Operating parameters
  - Fully static operation, up to 80 MHz
  - Up to −40 °C to 140 °C ambient temperature operating range
- Power management features
  - HALT mode — core clocks are stopped but the PLL is configurable
  - STOP mode — all clocks are stopped including the PLLs
  - Software-controlled clock gating of peripherals
- High performance, low cost e200z0h core processor
  - 32-bit CPU core complex (e200z0h)
  - Compliant with the Power Architecture® embedded category
  - Includes an instruction set enhancement allowing variable length encoding (VLE) for code size footprint reduction. Optional encoding of mixed 16-bit and 32-bit instructions makes it possible to achieve significant code size footprint reduction.
- 1.2 V internal logic for low power consumption
- Single power supply with 5.0 V ± 10% or 3.3 V ± 10% with internal regulator to provide 1.2 V for the core
- Designed with EMI reduction techniques
  - Internal phase-locked loop
  - Frequency modulation of system clock frequency
  - On-chip regulator
  - Controlled I/O slew rate
- Advanced microcontroller bus architecture (AMBA) crossbar switch (XBAR) providing concurrent access to peripherals, flash memory and SRAM
  - 3 master ports: e200z0 CPU IBUS, e200z0 CPU DBUS, and DMA
  - 5 slave ports: Flash Controller Port 0, Flash Controller Port 1, RAM Controller, PBRIDGE0 and PBRIDGE1
- 32-bit internal address bus, 32-bit internal data bus
- ECC (Error Correction Code) flash memory with flash controller
  - Up to 512 KB Code Flash—single module with prefetch buffer and 128-bit data access port
  - 32 KB Data Flash—single module with prefetch buffer and 128-bit data access port
- Up to 48 KB ECC RAM with RAM controller
- 8 KB dedicated ROM for embedded boot code
  - Boot Assisted Flash (BAF)
  - Supports internal flash programming via a serial link (UART)
- System timers:
  - 1 X STM (AUTOSAR®)
    1 X PIT (4 channels)
    4 X eTimers (6 channels each)

- System watchdog timer (SWT)

  32-bit timer

  Programmable selection of system or oscillator clock for timer operation

  Programmable selection of reset or interrupt on an initial time-out

  Enabled out of reset

- Safety and integrity features:
  - Clock Monitor Unit (CMU) for safe oscillator/PLL control using internal RC oscillator reference
  - Watchdog with time window for reload
  - Memory Protection Unit (MPU): 8 regions with 32-bit granularity
  - Register protected accesses to critical peripherals
- Interrupt controller (INTC) with dedicated interrupt source channels, including software interrupts and 32 priority levels
- 12-bit analog-to-digital converter (ADC) with a conversion time of 1.5 µs
  - 16 high-precision channels
  - Up to 16 channels
- 4 general purpose eTimer units, with 6 channels each
- Up to 2 Local Interconnect Network (LIN) controller modules capable of autonomous message handling (master), autonomous header handling (slave mode), and UART support. Compliant with LIN protocol rev. 2.1
- 4 DSPI (Deserial Serial Peripheral Interface) modules for full-duplex, synchronous, communications with external devices
- Up to 2 Controller Area Network (FlexCAN) modules compliant with the CAN protocol version 2.0 B. The bit rate can be programmed up to 1 Mbit/s.
- Frequency-modulated phase-locked loop (FMPLL)
- Configurable general purpose pins supporting input and output operations: 33 GPIO + 10 GPI/ADC input only (eTQFP64), and 63 GPIO + 16 GPI/ADC input only (eTQFP100)
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class 3
- Device/board boundary scan testing supported with per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- SPC570Sx family members are offered in the following package types:
  - 64-pin eTQFP, 0.5 mm pitch, 10 mm × 10 mm outline
  - 100-pin eTQFP, 0.5 mm pitch, 14 mm × 14 mm outline

3.4   Description of features

3.4.1   Low-power operation

 SPC570Sx devices have two dynamic power modes—STOP and HALT.

HALT mode is a reduced activity, low-power mode during which the clock to the core is disabled. It can be configured to switch off analog peripherals like clock sources, flash, main regulator, etc. for efficient power management at the cost of higher wakeup latency.

STOP mode is an advanced low-power mode during which the clock to the core is disabled. It can be configured to switch off most of the peripherals including clock sources for efficient power management at the cost of higher wakeup latency. In this mode, the primary and secondary PLL are switched off. This mode can be used to stop all clock sources and thus preserve the chip status. When exiting the STOP mode, the 16 MHz internal RC oscillator clock is selected as the system clock until the target clock is available.

3.4.2 e200z0h core processor

The e200z0h processor is similar to other processors in the e200zx series but supports only the VLE instruction set and does not include the signal processing extension for DSP applications or a floating point unit.

The e200z0h processor utilizes a four stage in-order pipeline for instruction execution. The Instruction Fetch (stage 1), Instruction Decode/Register file Read/Effective Address Calculation (stage 2), Execute/Memory Access (stage 3), and Register Writeback (stage 4) stages operate in an overlapped fashion, allowing single clock instruction execution for most instructions.

The integer execution unit consists of a 32-bit Arithmetic Unit (AU), a Logic Unit (LU), a 32-bit Barrel shifter (Shifter), a Mask-Insertion Unit (MIU), a Condition Register manipulation Unit (CRU), a Count-Leading-Zeros unit (CLZ), an 8×32 Hardware Multiplier array, result feed-forward hardware, and a hardware divider.

Most arithmetic and logical operations are executed in a single cycle with the exception of the divide and multiply instructions. A Count-Leading-Zeros unit operates in a single clock cycle. The Instruction Unit contains a PC incrementer and a dedicated Branch Address adder to minimize delays during change of flow operations. Sequential prefetching is performed to ensure a supply of instructions into the execution pipeline. Branch target prefetching is performed to accelerate taken branches. Prefetched instructions are placed into an instruction buffer capable of holding two instructions.

Conditional branches not taken execute in a single clock. All other taken branches have an execution time of two clocks.

Memory load and store operations are provided for byte, halfword, and word (32-bit) data with automatic zero or sign extension of byte and halfword load data as well as optional byte reversal of data. These instructions can be pipelined to allow effective single cycle throughput. Load and store multiple word instructions allow low overhead context save and restore operations. The load/store unit contains a dedicated effective address adder to allow effective address generation to be optimized. Also, a load-to-use dependency does not incur any pipeline bubbles for most cases.

The Condition Register unit supports the condition register (CR) and condition register operations defined by the Power Architecture. The condition register consists of eight 4-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching.

Vectored and autovectored interrupts are supported. Vectored interrupt support is provided to allow multiple interrupt sources to have unique interrupt handlers invoked with no software overhead.

The CPU includes support for Variable Length Encoding (VLE) instruction enhancements. This allows the classic Power Architecture instruction set to be represented by a modified

instruction set made up from a mixture of 16-bit and 32-bit instructions. This results in a significantly smaller code size footprint without affecting performance noticeably.

The CPU core has an additional 'Wait for Interrupt' instruction that is used in conjunction with low-power STOP mode. When Low-Power Stop mode is selected, this instruction is executed to allow the system clock to be stopped. An external interrupt source or the system wakeup timer is used to restart the system clock and allow the CPU to service the interrupt.

3.4.3 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between three master ports and five slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows for three concurrent transactions to occur from the master ports to any slave port; but each master must access a different slave. If a slave port is simultaneously requested by more than one master port, arbitration logic will select the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access. The crossbar provides the following features:

- 3 master ports:
    - CPU instruction bus
    - CPU data bus
    - DMA
- 5 slave ports
    - Flash controller Port 0
    - Flash controller Port 1
    - RAM controller
    - Peripheral bridge 0
    - Peripheral bridge 1
- 32-bit internal address, 32-bit internal data paths

3.4.4 DMA

The enhanced direct memory access (eDMA) controller is capable of performing complex data transfers with minimal intervention from a host processor. The DMA engine is able to perform source- and destination-address calculations and the actual data-movement operations, along with local memory containing transfer control descriptors for each of the DMA channels.

The DMA has the following features:
- Up to 16 DMA channels

3.4.5 DMACHMUX

The DMA channel multiplexer allows to route a defined number DMA peripheral sources to the DMA channels. Each DMACHMUX source can request a DMA channel transfer through a trigger signal and report to the requesting peripheral source the transfer status through a

''complete/ not complete'' acknowledge signal. The trigger source for each DMA channel can be configured through a dedicated register.

DMACHMUX includes the following features:

- 3 operation modes for each DMA channel
    - Disabled mode
    - Normal mode
    - Periodic trigger mode
- 16 output channels (input triggers for the DMA)
- 64 input triggers
    - 4 input periodic triggers
    - 4 always ON input periodic triggers

3.4.6   Flash memory

The SPC570Sx provides up to 512 KB of programmable, non-volatile flash memory for code and 32 KB for data. Each flash module includes a Prefetch Buffer that optimizes the performance of the flash array to match the CPU architecture and provides single cycle access to the flash at 80 MHz.

The flash memory provides the following features:

- 32-bit data bus for instruction fetch and CPU loads. Byte, halfword, word and doubleword (i.e. 64 bits) reads are supported. Only aligned doubleword writes are supported.
- Hardware and software configurable read and write access protections on a per-master basis
- Configurable access timing allowing use in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (0–31 additional cycles) allowing use for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page size of 128 bits (4 words)
- Embedded hardware program and erase algorithm

3.4.7   Flash memory controller

The Flash controller is connected between the XBAR slave ports and the Flash memory module and it acts as an interface between the system bus and the Flash memory module. The Flash controller is configured through a set of registers available through the IPS interface.

The flash modules interface to the system bus via a dedicated flash memory array controller and memory protection unit. For CPU loads and CPU instruction fetch, it supports a 32-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains a four-entry, 128-bit prefetch buffer, and a prefetch controller which prefetches sequential lines of data from the flash array into the buffer. Prefetch buffer hits allow no-wait responses. Normal flash array accesses are registered and are forwarded to the system bus on the following cycle, incurring three wait-states. Prefetch operations may be automatically controlled, and are restricted to instruction fetch.

The flash memory controller provides the following features:

- 2 flash controller ports connected to the XBAR slave ports
- 32-bit data bus
- 64-bit Flash write data bus
- 128-bit Flash read data bus
- No overlay RAM
- ECC with single-bit correction, double-bit detection
- ECC single-bit error corrections can be made visible to software
- Minimum program size is two consecutive 32-bit words, aligned on a 0-modulo-8 byte address, due to ECC
- Prefetch Buffer
    - Architected to optimize the performance of the flash with the CPU to provide single cycle access to the flash up to 80 MHz system clock speed
    - Configurable read buffering and line prefetch support
    - 4 line read buffers (each 128 bits wide) and a prefetch controller

3.4.8   SRAM

The SPC570Sx SRAM module provides a memory block of up to 48 KB. The SRAM controller includes these features:

- Supports read/write accesses mapped to the SRAM memory from any master
- Byte, halfword and word addressable for optimal use of memory
- ECC performs single-bit correction, double-bit detection on 32-bit data element
- User transparent ECC encoding and decoding for byte, half word, and word accesses
- Typical SRAM access time: 0 wait-state for reads and 32-bit writes; 1 wait-state for 8 and 16-bit writes if back to back with a read to same memory block

3.4.9   RAM controller

The RAM controller acts as an interface between the system bus and the integrated system RAM. It converts the protocols between the system bus and the dedicated RAM array interface. The RAM controller supports a 32-bit RAM interface. The RAM controller can apply one wait state for RAM access, by writing a bit within the registers accessible through the IPS interface.

3.4.10   MEMU

The MEMU collects and reports error events associated with ECC (Error Correction Code) logic used on SRAM, DMA RAM and Flash memory.

MEMU implements the following features:

- Supports up to 128 error sources per Reporting Block (System RAM ECC and MBIST, DMA RAM or Flash memory ECC)
- Support for error reporting from the following category of error sources (both for ECC and MBIST):
  - System RAM
  - DMA RAM
  - Flash memory
- Unique reported errors are logged into the module's reporting table which is accessible to CPU via memory mapped CPU register programming interface.
- MEMU handles overflow during error assertion and reports status accordingly
- Unique errors are stored in correctable and non correctable section of the reporting table and corresponding indication is generated to the FCCU
- CPU programs the known errors into the reporting table to avoid their rereporting by MEMU
- CPU clears the reporting table errors

3.4.11   Interrupt controller (INTC)

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC allows interrupt request servicing from software and peripheral interrupt vectors.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The software settable interrupt requests can be used to break the work involved in servicing an interrupt request into a high priority portion and a low priority portion. The high priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software settable interrupt request to finish the servicing in a lower priority ISR. Therefore these software settable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS (real-time operating system).

The INTC provides the following features:

- 178 interrupt triggers
- 4 interrupt vectors
- Each interrupt source can be programmed to one of 32 priorities
- Preemptive prioritized interrupt requests to processor
- ISR at a higher priority preempts executing ISRs or tasks at lower priorities
- Automatic pushing or popping of preempted priority to or from a LIFO
- Ability to modify the ISR or task priority to implement the priority ceiling protocol for accessing shared resources
- Low latency – three clocks from receipt of interrupt request from peripheral to interrupt request to processor

3.4.12 System clocks and clock generation

The following list summarizes the system clock and clock generation on the SPC570Sx microcontroller:

- System clock can be derived from:
    - Non-modulated PLL
    - External crystal oscillator 8-40 MHz (XOSC)
    - FMPLL
    - Internal RC oscillator 16 MHz (IRCOSC)
- Programmable output clock divider of system clock (1 to 8)
- Separate programmable peripheral bus clock divider ratio (1 to 16) applied to system clock
- Non-modulated PLL
    - Output independent of core clock frequency
    - Selectable clock source from external oscillator or internal 16 MHz RC oscillator
- Frequency-modulated phase-locked loop (FMPLL)
    - Selectable clock source from external oscillator or non-modulated PLL
    - Lock detect circuitry continuously monitors lock status
    - Loss-of-clock detection for reference and feedback clocks
    - On-chip loop filter (for improved electromagnetic interference performance and reduces number of external components required)
- On-chip crystal oscillator supports 8 MHz to 40 MHz crystals
- Dedicated 16 MHz internal RC oscillator
    - Used as default clock source out of reset
    - Provides a clock for rapid start-up from low-power modes
    - Provides a back-up clock in the event of PLL or external oscillator clock failure
    - Offers an independent clock source for the Watchdog timer
    - 3% accuracy over the operating temperature range
    - Trimming registers to support frequency adjustment with in-application calibration

3.4.13 IRCOSC

The Internal RC Oscillator digital interface (IRCOSC) controls the internal 16 MHz RC oscillator system. This oscillator system includes the main internal RC oscillator (MRC), as well as an internal temperature sensor and an internal voltage regulator used to compensate external variations in temperature and voltage. It also provides access to trimming information (the values are read by the SSCM and sent to the IRCOSC block during the reset sequence) used for safety implementations. The value of the loaded trimming is read from a read-only register. The trimming is further adjusted through the IRCOSC register interface.

3.4.14 XOSC

The XOSC digital interface controls the on-chip oscillator (XOSC) and provides the register interface for the programmable features. It supports a frequency range of 8-40 MHz.

3.4.15 System timers

The system timers include:

- System Timer Module (STM) timers
- Periodic Interrupt Timer (PIT) timers

The System Timer Module (STM) is a 32-bit timer designed to support commonly required system and application software timing functions. The STM includes a 32-bit up counter and four 32-bit compare channels with a separate interrupt source for each channel. The counter is driven by the system clock divided by an 8-bit prescaler value (1 to 256).

The PIT is an array of timers that can be used to raise interrupts and trigger DMA channels. It features the following:

- Up to 4 general purpose interrupt timers
- Up to 2 interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by system clock frequency
- 32-bit counter for real-time interrupt, clocked from main external oscillator

3.4.16 System software watchdog

The system software watchdog is a second watchdog module to complement the standard Power Architecture watchdog integrated in the CPU core. The system software watchdog is a 32-bit modulus counter clocked by the system clock or the crystal clock that can provide a system reset or interrupt request, when the correct software key is not written within the required time window.

The following features are implemented:

- 32-bit modulus counter
- Clock source: internal 16 MHz RC oscillator
- Supports normal or windowed mode
- Configurable response on timeout: reset, interrupt, or interrupt followed by reset
- Reset by writing a software key to memory mapped register
- Enabled out of reset
- Support for protected access to watchdog control registers with optional soft and hard locks
    - Soft lock allows temporary locking of configuration
    - Hard lock prevents any changes until after a Reset, once enabled
- Supports halting during low-power modes

3.4.17   FCCU

The FCCU collects fault event notification from the rest of the system and translates them into internal and/or external system reactions. It implements a state machine to handle the input fault triggers, the associated states, and the output pins. It also includes the following features:

- 1 to 128 faults (static parameter) management
- HW or SW fault recovery management
- Fault detection collection
- Fault injection (fake faults)
- External reaction (fault state): EOUT signaling
- Internal (SOC) reactions (alarm state): interrupt request
- Internal (SOC) reactions (fault state): long functional reset, short functional reset
- Bi-Stable, Dual-Rail and Time Switching SW controlled protocol with automatic HW reaction in case of fault
- Watchdog timer for the re-configuration phase
- Configuration lock

3.4.18   System integration unit lite (SIUL)

The SIUL features the following:

- Up to 4 levels of internal pin multiplexing, allowing exceptional flexibility in the allocation of device functions for each package

- 3 output interrupt triggers driven by 6 input interrupt triggers

- Centralized general purpose input output (GPIO) control of up to 63 input/output pins (package-dependent)

- All GPIO pins independently configurable to support pull-up, pull down, or no pull

- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports

- All peripheral pins can be alternatively configured as both general purpose input or output pins except ADC channels which support alternative configuration as general purpose inputs

- Direct readback of the pin value supported on all digital output pins through the SIUL

- Configurable digital input filter that can be applied to up to 16 general purpose input pins for noise elimination on external interrupts

- Register configuration protected against change with soft lock for temporary guard or hard lock to prevent modification until next reset (register-dependent)

3.4.19   FlexCAN

The SPC570Sx MCU contains up to two controller area network (FlexCAN) modules. The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B.

The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth.

Each FlexCAN module in the SPC570Sx includes two embedded memories, one for storing Message Buffers (MB) and another for storing Rx Individual Mask Registers. Support for 32 Message Buffers is provided.

The bxCAN bit timing logic can operate with either the system clock or external main oscillator clock (XOSCHS).

The FlexCAN modules provide the following features:

- Full implementation of the CAN protocol specification, version 2.0B
    - Standard data and remote frames
    - Extended data and remote frames
    - 0 to 16 bytes data length
    - Programmable bit rate up to 1 Mbit/s
- 32 mailboxes, each configurable as transmit or receive
    - Mailboxes configurable while module remains syncronized to CAN bus
- Transmit features
    - Supports configuration of multiple mailboxes to form message queues of scalable depth
    - Arbitration scheme according to message ID or message buffer number
    - Internal arbitration to guarantee no inner or outer priority inversion
    - Transmit abort procedure and notification
- Receive features
    - Individual programmable filters for each mailbox
    - 8 mailboxes configurable as a 6-entry receive FIFO
    - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
    - non FMPLL output
    - Direct oscillator clock to avoid PLL jitter
- Listen only mode capabilities

3.4.20 LINFlex

The LINFlexD consists of an 8-byte buffer for transmission/reception data. It also provides support for the basic UART transfers of 8-bit, 9-bit, 16-bit and 17-bit frames. The LINFlexD supports multi-channels and parametric DMA Tx/Rx interface in LIN/UART operating mode.

The LINFlex module includes the following features:

- Bit rates up to 20 Kbps
- Master/slave mode
- Classic and enhanced checksum calculation and check
- Single 8-byte buffer or FIFO for transmission/reception
- Timeout management
- Identifier filters
- DMA interface
- Supports a maximum of 16 possible identifiers
- Master mode with autonomous message handling
- Extended frame mode for in-application programming purposes
- Wake-up event on dominant bit detection
- True LIN field state machine
- Advanced LIN error detection
- Header, response and frame timeout
- Slave mode
  - Autonomous header handling
  - Autonomous transmit/receive data handling
- Identifier filters for autonomous message handling in Slave mode

The UART mode implements the follwoing features:

- Full-duplex communication
- Baud rate up to 1 Mbps in UART mode
- Separate clock for baud rate calculation
- 15/16/7/8 bits data, parity
- 1/2 stop bits
- 12 bit+parity reception
- 4-byte buffer for reception, 4-byte buffer for transmission
- 12-bit counter for timeout management

3.4.21 Deserial serial peripheral interface (DSPI)

The DSPI blocks provide a synchronous serial bus for communication between the MCU and external peripheral devices. Each DSPI module operates as a basic SPI or as a queued SPI through the use of internal FIFOs. For queued operations the SPI queues reside in system RAM, external to the DSPI. Data transfers between the queues and the DSPI FIFOs are accomplished through host software.

3.4.22 eTimer

Each eTimer module is equipped with six 16-bit general purposes up/down timer/counter, which can be cascaded. Each counter channel can be used as input capture or output compare function.

It includes the following features:

- 6 output compare triggers
- Up to 12 input capture register
- 2 DMA requests per eTimer block
- Watchdog is present

3.4.23 Analog-to-digital converter module (ADC)

The ADC module contains advanced features for Normal, Injected and triggered injected conversion. It supports an interface to the cross triggering unit (CTU).

There are three types of input channels available: internal precision channels. Control registers within the ADC can be programmed to configure which channel is to be converted. A conversion timing register that allows to configure different sampling is associated to each type of channel.

The ADC provides 12-bit conversion with a conversion time of 1.5 µs. It features one shot/scan mode conversion, hardware chain injection mode. It also provides four watchdog channels to monitor whether signals remain within a defined range. A dedicated power-down mode is implemented to save power consumption.

The ADC features the following:

- 2 equivalent ADC units (main and supervisor)
- 0 to V_{REF} conversion range
- Minimum conversion speed 1.5. µs (user channels)
- Up to 16 single-ended input channels (user channels) fully shared (main and supervisor)
- Single or dual conversion mode (via cross-triggering unit)
- +/- 6 LSB TUE for reference voltage greater than 3V
- 8 internal channels for testing/monitoring (ADC VREFH, temperature, core supply) at lower speed

3.4.24 CTU

The CTU (Cross Trigger Unit) provides commands to the ADC and triggers other IPs. The CTU is organized into two main blocks: TGS (Trigger Generator Unit), which is used for generate up to eight trigger events from a combination of input signals and SU (Scheduler Unit), which uses a commands list in order to select the command to send to the ADC when a trigger event occurs.

The CTU implements the following features:

- Cross triggering between ADC, eTimer, and external pins
- Double buffered trigger generation unit with up to 8 independent triggers generated from external triggers
- Maximum operating frequency less than or equal to 80 MHz
- Trigger generation unit configurable in sequential mode or in triggered mode
- Trigger delay unit compensates the delay of external low pass filter
- Double buffered global trigger unit allows eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with up to 24 ADC commands
- Each trigger capable of generating consecutive commands
- ADC conversion command allows control of ADC channel from each ADC, single or synchronous sampling, independent result queue selection
- DMA support with safety features

3.4.25   Temperature sensor

The temperature sensor monitors the device temperature. It also provides an analog output voltage, proportional to the current temperature. It incudes the following features:

- The temperature measurement is calibrated by 12-bit trimmer value
- The temperature sensor is controlled by MC_PMC block
- There are three digital outputs , used to signal under- and over-temperature operating conditions

3.4.26   BIST

MBIST and LBIST are provided to avoid the accumulation of latent faults in the functional logic as well as the safety integrity mechanisms. Dedicated mechanisms are provided to check the availability of safety mechanisms and the functionality of each error reaction path (such as by fake fault injection).

In case an error is detected during MBIST, the following information shall be transmitted from the STCU/MBIST/MBIST collar to the MEMU:

- Single-Bit-Error vs. Multi-Bit-Error
- Address of error (the tested address)
- Bit position of the error (if a single bit error)

LBIST detects latent faults:

- Platform diagnostic coverage greater than or equal to 90%
- Peripherals diagnostic coverage greater than or equal to 60%

3.4.27   Nexus port controller

The IEEE-ISTO 5001-2003 standard defines an extensible auxiliary port which is used in conjunction with the JTAG port in the e200z0h. The Nexus modules are coupled to the core and monitor a variety of signals including addresses, data, control signals, status signals, etc.

The NPC (Nexus Port Controller) block provides real-time development support capabilities for the SPC570Sx Power Architecture-based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The development support provided includes program trace and run-time access to the MCU's internal memory map and access to the e200z0h processor core during halt. The Nexus interface also supports a JTAG only mode using only the JTAG pins.

Supported Nexus 2 Plus features include:

– Static debug

– Watchpoint messaging

– Ownership trace messaging

– Program trace messaging

– Real-time read/write of any internally memory mapped resources through JTAG pins

– Overrun control, which selects whether to stall before Nexus overruns or keep executing and allow overwrite of information

– Watchpoint triggering, watchpoint triggers program tracing

3.4.28 Nexus Multimaster Trace Client

The NXMC module monitors the system bus and provides real-time trace information to debug or development tools. This also provides the capability of sending user defined messages for the peripherals attached to it.

The NXMC implements the following features:

- Data trace via Data Write Messaging (DWM) and Data Read Messaging (DRM). This provides the capability for the development tool to trace reads and/or writes to (selected) internal memory resources.

- Multi-master tracing capability for multiple master accesses

- Watchpoint messaging based on internal/external triggers, via the auxiliary pins

- Watchpoint trigger events out based on internal/external triggers

- Watchpoint trigger enable of data trace messaging

- Peripheral interface for data message transfers based on In Circuit Trace Message (ICTM) format

- Optional timestamping of the messages based on timer value and controls received at the interface

3.4.29 JTAG Master

The JTAG Master (JTAGM) module acts as JTAG master inside the device. The module has a parallel interface that can exchange data with another serial communication module or via customer software.

The data transferred to this module is transformed to produce TCK, TMS, and TDI outputs and to accept TDO inputs. The JTAGM is connected in the device to allow these five signals to connect to the JTAGC as if the JTAG data is coming from an outside tool. The JTAGM generates all required JTAG scan chains to allow software and high speed serial communication access to all JTAG mapped resources.

The JTAGM implements the following features:

- Provides efficient handshake to the external tool to read any memory mapped address location within the device
- Provides software the option to write data for driving JTAG

3.4.30 JTAG Data Communication Module

The JTAG Data Communication (JDC) module provides the capability to move register data between the IPS and JTAG domains. This facilitates communication between internal resources that access memory mapped register space and an external tool that accesses the JTAG port. The JDC module consists of IPS accessible registers, JTAG accessible registers, and associated logic to coordinate movement of data from one register domain to another.

3.4.31 On-chip voltage regulator (VREG)

The on-chip regulator in the SPC570Sx regulates input to generate all internal supplies. It comprises of a single regulator. The nominal target output is 1.2 V with a full current load range 0 to 200 mA provided through internal PMOS ballasts.

3.4.32 PBRIDGE

The Peripheral Bridge is the interface between the AMBA AHB 2.v6 interface and on-chip IPS v3.0 peripherals. The PBRIDGE generates module enables, the module address, transfer attributes, byte enables and write data as inputs to the IPS peripherals. Separate interface ports are provided for on-platform and off-platform peripherals. The PBRIDGE memory space occupies a 64 MB portion of the processor address space. A 0.5 MB portion of this space is allocated to on-platform peripherals. The remaining 63.5 MB are reserved. The register maps of the IPS peripherals are located on 16 KB boundaries. Each IPS peripheral is allocated one 16 KB block of the memory map, and is activated by one of the module enables from the PBRIDGE.

It includes the following main features:

- 32-bit wide AHB data bus port
- IPs are partitioned on two different AIPS bridge
- Peripheral access is regulated by acess protection rules
- Signal integrity checkers are used to guarantee the AIPS signal integrity

3.4.33 SSCM

During the boot phase, the SSCM module retrieves a set of system and blocks configurations and dispatches them to the proper modules. SSCM provides information about the current state and configuration of the system. The SSCM includes the following features:

- Connects to the Flash through a 128-bit port
- Stores the configuration into 64-bits record called DCF (Device Configuration Format)
- Management of life cycle for security

3.4.34 MC_ME

The MC_ME controls the chip mode and mode transition sequences in all functional states. It also contains configuration, control and status registers accessible for the application. It includes the following features:

- Sets the main core execution address
- Configures and controls the current execution mode
- Peripheral clock gating
- Captures the current peripheral and core clock/gated enabled status
- Progressive system clock switching when transitioning from a lower power consumption mode to a higher power consumption mode, and viceversa
- MC_ME supports the following modes:
  - Reset
  - DRUN
  - SAFE
  - RUN0..3
  - HALT
  - STOP
- The ME module generates the following interrupts:
  - Invalid mode interrupt
  - SAFE mode interrupt
  - Mode transition complete interrupt

3.4.35 MC_RGM

The reset generation module (MC_RGM) centralizes the different reset sources and manages the reset sequence of the chip. It provides a register interface and the reset sequencer. The MC_RGM module includes the following features:

- "Destructive" resets management
- "Functional" resets management
- Converts reset events to SAFE mode or interrrupt request events
- Short reset sequence configuration
- The escalation of recurring "functional resets" to "destructive resets" is configurable
- The escalation of recurring "destructive resets" to "functional resets" is configurable, to keep the chip in reset state until the next power-on reset

3.4.36 MC_PMC

The power management controller (PMC) consists of two blocks: an analog block and a digital block. The digital block of the PMC, acts as a bridge interface between the analog block and the SW application. It contains all the registers and the digital logic to generate all enable signals, trim control bits, POR reset generation, and test mode logic for the analog block.

It includes the following features:

- Contains registers that enable/disable the various voltage monitors
- Handles the Temperature Sensor output

3.4.37   MC_CGM

The MC_CGM module regulates the clock changes, guaranteeing a smooth clock transition, which, in turn, avoids abrupt power changes. It also contains a set of registers that configure the various clock dividers and the configuration for the auxiliary clocks going to the various modules.

It includes the following features:

- Generates system and peripheral clocks
- Selects and enables/disables the system clock supply from system clock sources according to MC_ME control
- Performs progressive system clock frequency change depending on MC_ME mode configuration
- Contains a set of registers to control clock dividers for divided clock generation

3.4.38   Memory protection unit (MPU)

The MPU provides 8 region descriptors and 32-byte granularity. Features include:

- Support for overlapping regions
- Protection attributes can optionally include process ID
- Access control based on Process ID
- Protection offered for three concurrent read ports
- Read and write attributes for all masters
- Execute and supervisor/user mode attributes for processor masters

3.4.39   Wakeup

The Wakeup Unit translates the NMI input alternate function trigger into one of the possible system reactions: a non-maskable interrupt triggers a "Critical Exceptions" directly to the CPU or a functional reset to the MC_RGM. The NMI alternate function pin is used to trigger the wake-up unit, which in turns generates different system reactions. The input NMI trigger is filtered by an anti-glitch circuitry.

3.4.40   CRC

The Cyclic Redundancy Check (CRC) computing unit is dedicated to the computation of CRC, off-loading this work from the CPU.

3.4.41   STCU2

The STCU2 IP is used to handle the BIST procedure. The BIST is divided into LBIST (BIST on the logic) and MBIST (BIST on the memory). The STCU2 runs the BIST on different partitions sequentially or concurrently. It includes the following features:

- Watchdog is available and is automatically started to monitor the BIST execution
- CRC check is available to report an error or mismatch between a pre-calculated signature and a dynamically calculated one.
- A BIST error is reported to the FCCU through two different trigger signals

3.4.42   XBIC

The Crossbar Integrity Checker (XBIC) verifies the integrity of the attribute information for crossbar transfers and signals the Fault Collection and Control Unit (FCCU) when an error is detected.

The XBIC includes the following features:

- Verification of attribute information for all crossbar transfers
- Error injection for testing
  - Programmable master and slave port specifiers
- Programmable integrity check enable on a per-slave-port basis

3.4.43   Register protection

The register protection module protects several registers against accidental writing, locking their value till the next reset phase. Once a module is eligible for protection, its register is visible in two different address spaces, within the module IPS register space. The original register location is accessed as for any other module registers. The registers in the mirrored space, each one shifted by a fixed value, acts as a write-and-lock resource. Once data is written to these registers, the register itself becomes write-locked. The lock status bits are accessible at a specific area, within the module address space. The lock bits can be over-written, with the optional programmable possibility to lock the writing capability till the next reset and/or by supervisor access only.

3.4.44   PASS

The PASS module programs a set of Flash memory access protections, based on user-programmable passwords. It also maintains access states. The PASS module is organized as a set of flags, which gates or enables certain resource access. It includes the following distinct features:

- Password comparison
- 4 kinds of flags which constitute the PASS module:
  - Flash block program/erase (one flag per block)
  - Flash block read (one flag for region)
  - Debug activation

3.4.45   SPU

The Sequence Processing Unit (SPU) provides an on-device trigger functions similar to those found on a logic analyzer. In a complex SoC, performance monitor functions are available at two levels: system level and CPU level. Complex trigger and system performance monitor functions are implemented in the SPU module. System level performance monitor functions are integrated into the SPU complex trigger logic, and thus allow counting and timing of any debug trigger combinations supported by the SPU.

The SPU includes the following features:

- Input watchpoints/triggers selection
- Input debug triggers for instruction execution selection
- Input interrupt selection

3.4.46 Debug and Calibration Interface

The Debug and Calibration Interface (DCI) module provides debug features for the MCU. It includes a standard 1149.1/1149.7 compatible JTAG interface which is used to connect with an external JTAG tool using a low frequency clock interface.

It also features a software based debug mode which can be controlled by the MCU without using an external tool. Additionally, the DCI provides features for debug control using break-points and synchronous restart of the cores.

The DCI implements the following features:

- Debug mode enable control for connected tool or software
- Debug break and cross-triggering control
- Synchronous restart control for all CPUs when exiting debug mode
- Tool hot plug capability
- Security access control
- Debug reset control

4   Developer support

The SPC570Sx MCU family uses tools and third-party developers which offer a widespread, established network of tool and software vendors. The SPC570Sx MCU also features a high-performance Nexus debug interface. The following development support is available:
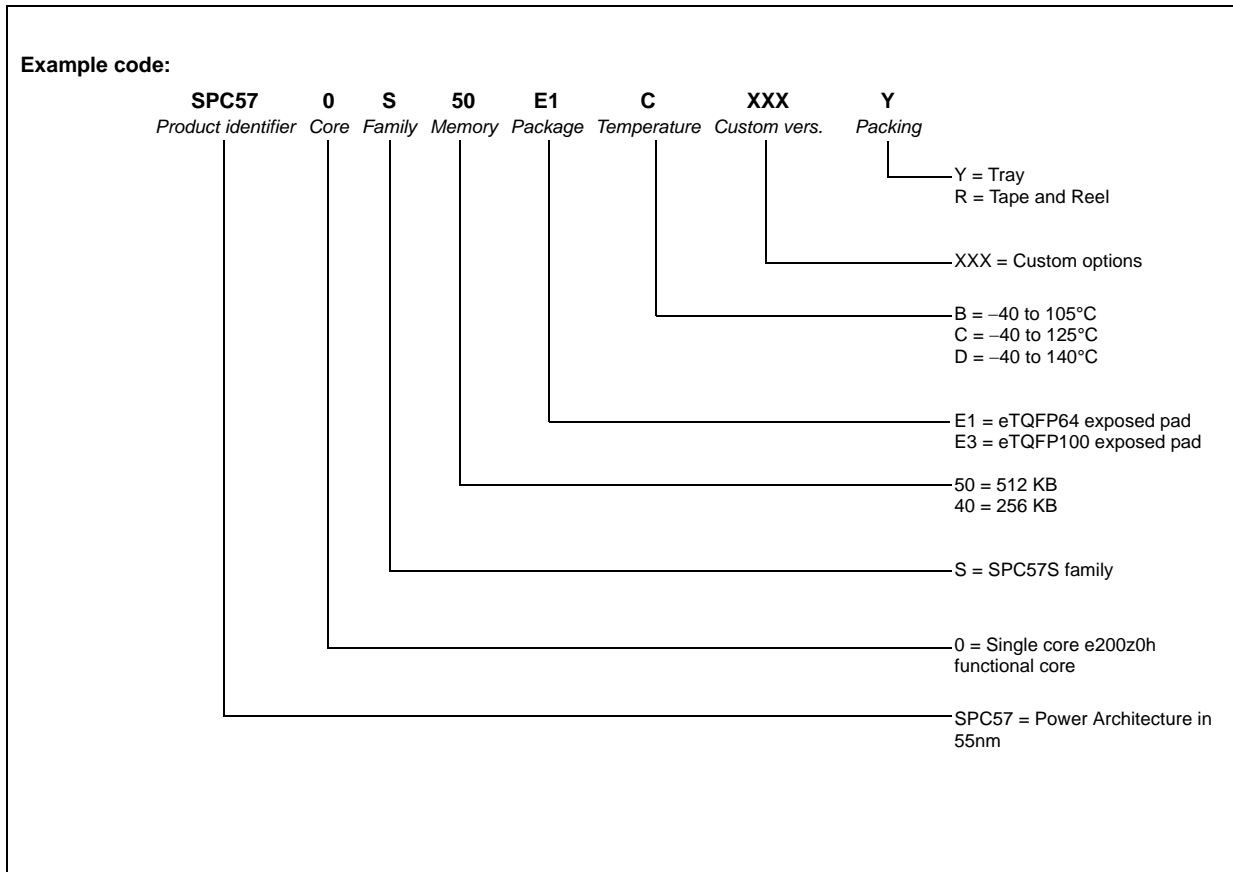
- Automotive evaluation boards (EVB) featuring CAN, LIN interfaces, and more
- Compilers
- Debuggers
- JTAG and Nexus interfaces

The following software support is available:

- OSEK solutions are available from multiple third parties
- CAN and LIN drivers
- AUTOSAR package

5   Ordering information

Figure 2. Ordering information scheme

Example code:

SPC57	0	S	50	E1	C	XXX	Y
Product identifier	*Core*	*Family*	*Memory*	*Package*	*Temperature*	*Custom vers.*	*Packing*

Y = Tray
R = Tape and Reel

XXX = Custom options

B = −40 to 105°C
C = −40 to 125°C
D = −40 to 140°C

E1 = eTQFP64 exposed pad
E3 = eTQFP100 exposed pad

50 = 512 KB
40 = 256 KB

S = SPC57S family

0 = Single core e200z0h functional core

SPC57 = Power Architecture in 55nm

6   Revision history

Table 3. Document revision history

Date	Revision	Changes
14-Dec-2012	1	Initial release
19-Dec-2012	2	Cover page and *Table 1: SPC570Sx device feature summary (Family Superset Configuration)*, specified that EEPROM is a data Flash memory suitable for EEPROM emulation *Figure 1: Family Superset block diagram*: removed lockstepped DMACHMUX block and connected RCCU block; inverted positions of AIPS0 and AIPS1 blocks *Figure 2: Ordering information scheme*, fixed formatting issues
09-Feb-2015	3	Updated *Features* in cover page. Updated *Table 1: SPC570Sx device feature summary (Family Superset Configuration)* and *Table 2: SPC570S40Ex, SPC570S50Ex device configuration differences* Replaced SPC570S50Lx by SPC570Sx in all document.
03-Mar-2015	4	Error typo.

IMPORTANT NOTICE – PLEASE READ CAREFULLY