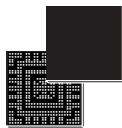
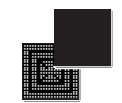


# SR6 G7 line of Stellar integration MCUs — 32-bit Arm® Cortex®-R52, Cortex®-M4 automotive MCU 6x cores, HW virtualization, 20.5 MB NVM (with 2x 19.5 MB "OTA X2" storage), HSM, ASIL-D



FPBGA 476  
(21 x 21 mm)



FPBGA 292  
(17 x 17 mm)



## Features

- AEC-Q100 automotive qualification on going
- Stellar integration MCUs:
  - Have superior real-time and safe performance (with highest ASIL-D capability)
  - Bring HW based virtualization technology to MCUs for simplified multiple SW integration at optimized performance
  - Have built-in fast and cost effective OTA reprogramming capability (with built-in dual image storage)
  - Offer high speed security cryptographic services, for example for network authentication

## Cores

- 32-bit Arm® v8-R compliant CPU cores:
  - 6 Cortex®-R52 cores (4 of them with checker cores, 2 in split-lock configuration) allowing usage as either 6 cores (4 of them in lockstep configuration) or 5 cores (all of them in lockstep configuration), single precision FPU, new privilege level for real-time virtualization
  - 2 NEON extensions (for example SIMD, dual precision FPU)
- 2 Cortex®-M4 multi purpose accelerators (data move and [pre]-processing). 1 in lockstep configuration
- 4 eDMA engines in lockstep configuration

## Memories

- Up to 20.5 MB on-chip NVM non volatile memory
  - PCM (phase change memory) as non volatile memory
  - 19.5 MB code NVM, with embedded memory replication for OTA (over-the-air) reprogramming with up to 2x 19.5 MB
  - 1024 KB HSM dedicated code NVM
- 640 KB data NVM (512 KB + 128 KB dedicated to HSM)
- Up to 8576 KB on-chip general-purpose SRAM

## Security: hardware security module - 2<sup>nd</sup> generation

- On-chip high performance security module with EVITA full support
- Symmetric and asymmetric cryptography processor
- High performance lock-stepped AES-light security sub-system for fast ASIL-D cryptographic services

## Safety: comprehensive new generation ASIL-D safety concept

- New state of the art safety measures at all level of the architecture for most efficient implementation of ISO26262 ASIL-D functionalities
- Complete HW virtualization architecture build on Cortex®-R52 new privilege mode (best-in class SW isolation, real-time support for multiple virtual machine/ applications)

| Part number | Package   |
|-------------|-----------|
| SR6G7C5     | FPBGA 476 |
| SR6G7C3     | FPBGA 292 |

### Device stand-by / low power modes

- Ultra low power: stand by mode for lowest quiescent current with optimized active subsystem (for example stand-by RAM) and wakeup capability
- Smart low power: stand-by mode enhanced with active Cortex<sup>®</sup>-M4 subsystem and extended COM interfaces and ADC peripheral.

### Peripheral, IOs, communication interfaces

- 28 LINFlexD modules
- 2 dual-channel FlexRay controllers
- 10 queued serial peripheral interface (SPIQ) modules
- 2 SENT modules (15 channels each)
- 2 PSI5 modules (2 channels each)
- Enhanced analog-to-digital converter system with
  - 12 separate 12-bit SAR analog converters (including one supervisor/safety ADC).
  - 4 separate 9-bit SAR analog converters (2 channels each) with fast comparator mode
  - One 9-bit SAR analog converter for device stand-by / low power mode
  - Interconnection with GTM timer for autonomous ADC/GTM subsystem operation
- Advanced timed I/O capability
  - Generic timer module (GTM4154)
- Communication interfaces
  - 2 ethernet controllers 100/1000 Mbps, compliant IEEE 802.3-2008: IPv4 and IPv6 checksum modules, AVB, VLAN and EMC optimized SGMII
  - 19 modular controller area network (MCAN) modules, and 1 time-triggered controller area network (M-TTCAN), all supporting flexible data rate (ISO CAN-FD)

### External memory interfaces

- 2 OctalSPI to support Hyperbus<sup>™</sup> memory (Flash/RAM) devices
- 1 SDMMC interface

## 1 Introduction

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### 1.1 Document overview

This document provides a summary of the target specification and features of the devices. For detailed information, refer to the device Datasheet and device Reference manual.

*Note:* For information on the Cortex®-R52 and Cortex®-M4 cores refer to the Cortex®-R52 and Cortex®-M4 technical reference manuals, available from the [www.arm.com](http://www.arm.com) website.



### 1.2 Description

Stellar integration MCUs have been designed to meet the requirements of domain controllers and ECUs with high integration requested in the architectures of connected update-able automated and electrified cars. They have superior real-time and safe performance (with highest ASIL-D capability). Bringing HW based virtualization technology to MCUs, they ease the development and integration of multiple source SW onto the same HW while maximizing the resulting SW performance. They offer high efficiency OTA reprogramming capability with fast new image download and activation at almost no memory overhead thanks to SR6 unique built-in dual image storage tailored to OTA reprogramming needs and provide high speed security cryptographic services, for instance for network authentication.

**Table 1. SR6G7x overview**

| Feature   |   | SR6G7x   |
|---|---|--|
| Cortex®-R52 cores (+ checker cores)   |   | 6 cores (+4 checkers), configurable as 5 cores (+5 checkers) |
| NEON (with SIMD, dual precision floating point)   |   | 2  |
| Cache (instruction / data) per core in Kbyte  |   | 32 / 32  |
| Core memory protection unit (regions), several additional protection mechanisms in the architecture, for example: NOC firewalls | Hypervisor (EL2)                            | 24   |
|   | OS (EL1)                                    | 24   |
| Code NVM in Mbyte   | Overall including HSM in Mbyte              | 20.5   |
|   | Cluster code NVM in Mbyte                   | 19.5   |
|   | HSM code NVM in Kbyte                       | 1024   |
| Code NVM Built-in memory replication for OTA reprogramming (not supported by HSM) in Mbyte                                      |   | Up to 2x 19.5  |
| Data NVM in Kbyte   | Overall                                     | 640  |
| RAM in Kbyte  | Overall                                     | 8576   |
| Hardware security module (HSM) - 2 <sup>nd</sup> generation   |   | Yes  |
| AES-Light (cryptographic services - in lockstep)  |   | 4  |
| Arm® Cortex®-M4   | Multi-purpose accelerator (DSPH)            | 1  |
|   | Multi-purpose accelerator in lockstep (DME) | 1  |
| Stand-by and smart power modes  |   | Yes  |
| LIN and UART (LINFlexD)   |   | 28   |
| CAN   | Overall                                     | 20   |
| SPIQ (with LVDS channel)  |   | 10 (2)   |
| Microsecond channel   |   | 0  |
| Microsecond channel plus  |   | 0  |
| SENT  | Unit  | 2  |
|   | Channel/unit                                | 15   |
| I2C   |   | 2  |
| PSI5  | Unit  | 2  |
|   | Channel/unit                                | 2 channels   |
| FlexRay (dual channel)  |   | 2  |
| Gigabit ethernet IEEE 802.3-2008 compliant (with MII, RMII, RGMII, SGMII)   |   | 2  |
| Generic timer modules (GTM4)  | GTM4154                                     | 1  |
| High-resolution timer   |   | 2 x 8 ch   |
| 12-bit SAR analog converters  |   | 12   |
| 16-bit sigma-delta analog converters (units with DSPL)  |   | 0  |
| 9-bit SAR analog comparators  |   | 8  |
| OctalSPI (support Hyperbus™ memory devices)   |   | Yes  |
| SDMMC interface   |   | Yes  |
| Max temperature (target)  | Junction temperature                        | 150 °C   |
| Packages  | FPBGA 476                                   | X  |
|   | FPBGA 292                                   | X  |

## Revision history

**Table 2. Document revision history**

| Date        | Version | Changes  |
|-------------|---------|--|
| 01-Jun-2021 | 1       | Initial release.   |
| 12-Aug-2021 | 2       | Package and part number: <ul style="list-style-type: none"> <li>• Replaced FPBGA 516 with FPBGA 476 package in the whole document,</li> <li>• Updated FPBGA 292 package silhouette,</li> <li>• Replaced SR6G7C7 with SR6G7C5 part number.</li> </ul> |

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