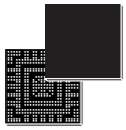
Stellar SR6 G7 line — 32-bit Arm® Cortex®-R52+ automotive integration MCU 6x Cortex®-R52+ cores, 20.5 MB NVM (2x 19.5 MB “OTA X2”) 9.1 MB RAM, with embedded virtualization, safety and security



FPBGA 476
(21.3 x 21.3 mm)

FPBGA 292
(17 x 17 mm)

Part number	Package
SR6G7C6	FPBGA 476
SR6G7C4	FPBGA 292

Features

- AEC-Q100 automotive qualification on going
- SR6 integration MCUs:
  - Have superior real-time and safe performance (with highest ASIL-D capability)
  - Bring HW based virtualization technology to MCUs for simplified multiple SW integrations at optimized performance
  - Have built-in fast and cost effective OTA reprogramming capability (with built-in dual image storage)
  - Offer high speed security cryptographic services, for example for network authentication

Cores

- 32-bit Arm® v8-R compliant CPU cores:
  - 6 Cortex®-R52+ cores (4 of them with checker cores, 2 in split-lock configuration) allowing usage as either 6 cores (4 of them in lockstep configuration) or 5 cores (all of them in lockstep configuration), single precision FPU, new privilege level for real-time virtualization
  - 2 NEON extensions (for example SIMD, dual precision FPU)
- 2 Cortex®-M4 multipurpose accelerators (data move and [pre]-processing). Both in lockstep configuration
- 4 eDMA engines in lockstep configuration

Memories

- Up to 20.5 MB on-chip NVM non-volatile memory:
  - PCM (phase change memory) as non-volatile memory
  - 19.5 MB code NVM, with embedded memory replication for OTA (over-the-air) reprogramming with up to 2x 19.5 MB
  - 1024 KB HSM dedicated code NVM
- 640 KB data NVM (512 KB + 128 KB dedicated to HSM)
- Up to 9280 KB on-chip general-purpose SRAM

Security: hardware security module - 2nd generation

- On-chip high-performance security module with EVITA full support
- Symmetric and asymmetric cryptography processor
- High performance lock-stepped AES-light security sub-system for fast ASIL-D cryptographic services

Safety: comprehensive new generation ASIL-D safety concept

- New state-of-the-art safety measures at all levels of the architecture for most efficient implementation of ISO26262 ASIL-D functionalities
- Complete HW virtualization architecture built on Cortex®-R52+ new privilege mode (best-in class SW isolation, real-time support for multiple virtual machine/applications)

Device stand-by / low-power modes

- Versatile low-power modes
- Ultra low-power: stand-by mode for lowest quiescent current with optimized active subsystem (for example stand-by RAM) and wakeup capability
- Smart low-power: smart power mode with Cortex®-M4 subsystem and extended COM interfaces and ADC peripheral

Peripheral, IOs, communication interfaces

- 28 LINFlexD modules
- 2 dual-channel FlexRay controllers
- 10 queued serial peripheral interface (SPIQ) modules
- 2 SENT modules (15 channels each)
- 2 DSPI with shifted PWM serialization support for lighting applications
- 2 PSI5 modules (2 channels each)
- Enhanced analog-to-digital converter system with:
  - 8 separate 12-bit SAR analog converters (including one supervisor/safety ADC).
  - One 9-bit SAR analog converter for device stand-by / low-power mode
  - Interconnection with GTM timer for autonomous ADC/GTM subsystem operation
- Advanced timed I/O capability:
  - Generic timer module (GTM4154)
- Communication interfaces:
  - 2 ethernet controllers 10/100/1000 Mbps, compliant with IEEE 802.3-2008: IPv4 and IPv6 checksum modules, AVB, VLAN and EMC optimized SGMII
  - 19 modular controller area network (MCAN) modules, and 1 time-triggered controller area network (M-TTCAN), all supporting flexible data rate (ISO CAN-FD)

External memory interfaces

- 2 OctoSPI to support HyperBus™ memory (Flash/RAM) devices
- 1 SDMMC interface

1 Introduction

1.1 Document overview

This document provides a summary of the target specification and features of the SR6G7x devices. For detailed information, refer to the device Datasheet and device Reference manual.

Note: For information on the Cortex®-R52+ and Cortex®-M4 cores refer to the Cortex®-R52+ and Cortex®-M4 technical reference manuals, available from the www.arm.com website.

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1.2 Description

Stellar integration MCUs have been designed to meet the requirements of domain controllers and ECUs with high integration requested in the architectures of connected update-able automated and electrified cars. They have superior real-time and safe performance (with highest ASIL-D capability). Bringing HW based virtualization technology to MCUs, they ease the development and integration of multiple source SW onto the same HW while maximizing the resulting SW performance. They offer high efficiency OTA reprogramming capability with fast new image download and activation at almost no memory overhead thanks to SR6 unique built-in dual image storage tailored to OTA reprogramming needs and provide high speed security cryptographic services, for instance for network authentication.

Table 1. SR6G7x overview

Feature		SR6G7x
Cortex®-R52+ cores (+ checker cores)		6 cores (+4 checkers), configurable as 5 cores (+5 checkers)
NEON (with SIMD, dual precision floating point)		2
Cache (instruction / data) per core in Kbyte		32 / 32
Core memory protection unit (regions), several additional protection mechanisms in the architecture, for example: NOC firewalls	Hypervisor (EL2)	24
	OS (EL1)	24
Code NVM	Overall including HSM in Mbyte	20.5
	Cluster code NVM in Mbyte	19.5
	HSM code NVM in Kbyte	1024
Code NVM built-in memory replication for OTA reprogramming (not supported by HSM) in Mbyte		Up to 2x 19.5
Data NVM in Kbyte		640
RAM in Kbyte		9280
Hardware security module (HSM) - 2nd generation		Yes
AES-Light (cryptographic services - in lockstep)		4
Arm® Cortex®-M4	Multi-purpose accelerator in lockstep (DSPH)	1
	Multi-purpose accelerator in lockstep (DME)	1
Stand-by and smart power modes		Yes
eDMA engines (number of channels, more channels through muxes/channel)	Engine	4
	Channel	3 x 32 1 x 64
LIN and UART (LINFlexD)		28
CAN-FD		20

Feature		SR6G7x
CAN-XL		No
SPIQ (with LVDS channel)		10 (2)
Microsecond channel (MSC)		No
Microsecond channel plus (MSCP)		No
SENT	Unit	2
	Channel/unit	15
I^2C		2
PSI5	Unit	2
	Channel/unit	2 channels
FlexRay (dual channel)		2
Gigabit ethernet IEEE 802.3-2008 compliant (with MII, RMII, RGMII, SGMII)		2
SIPI / LFAST interprocessor bus		2
Generic timer modules (GTM4)	GTM4154	1
High-resolution timer		No
12-bit SAR analog converters		8
16-bit sigma-delta analog converters (units with DSPL)		No
9-bit SAR analog comparators		No
OctalSPI (support HyperBus™ memory devices)		Yes
SDMMC interface		Yes
Debug port	Main debug port (JTAG+SWD)	Yes
	Secondary debug port (SWD)	Yes
High speed off-chip trace lane (multi GBit/s, Aurora™ protocol)		4
Max temperature (target)	Junction temperature	150 °C
Packages	FPBGA 476	X
	FPBGA 292	X

1.3 Block diagram

The figure below shows the top-level block diagram.

Figure 1. Block diagram

1: emulated by GTM

Revision history

Table 2. Document revision history

Date	Version	Changes
01-Jun-2021	1	Initial ST Restricted release.
12-Aug-2021	2	Second ST Restricted release.
21-Jun-2022	3	Initial public release.
24-Jun-2022	4	Figure 1. Block diagram: replaced Cortex®-R52 by Cortex®-R52+.
23-Sep-2022	5	In the whole document, minor editorial changes. • document title: updated RAM size from 8.9 to 9.1 MB • Peripheral, IOs, communication interfaces: – updated "12 separate 12-bit SAR..." to "8 separate 12-bit SAR... – removed bullet "High-resolution timer..." • Section 1.1 Document overview: added "SR6G7x" in the first sentence • Table 1. SR6G7x overview: – "Arm®Cortex®-M4, Multi-purpose accelerator (DSPH)" line: added in lockstep – set "CAN-XL" to "No" – set "High-resolution timer" "SR6G7x" column to "No" – set "16-bit sigma-delta analog converters (units with DSPL)" "SR6G7x" column to "No" – "12-bit SAR analog converters": changed 12 to 8 – set "9-bit SAR analog comparators" "SR6G7x" column to "No"

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