

# Stellar SR6 P3E line—32-bit Arm<sup>®</sup> Cortex<sup>®</sup>-R52+ automotive integration MCU 4× Cortex<sup>®</sup>-R52+ cores, 19.5 MB xMemory, 1.8 MB RAM, with embedded virtualization, safety, and security



FPBGA476  
(21.3 × 21.3 mm)



FPBGA292  
(17 × 17 mm)



## Features

### Highlights

- AEC-Q100 qualified
- SR6 integration *MCUs*:
  - Have superior real-time and safe performance (with highest *ASIL-D* capability)
  - Bring hardware-based virtualization technology to *MCUs* for simplified multiple software integrations at optimized performance
  - Have built-in no downtime *OTA* reprogramming capability (with built-in dual-image mechanism)
  - Offer high-speed security cryptographic services, for example for network authentication

### Cores and accelerators

- 4 × 32-bit Cortex<sup>®</sup>-R52+ cores (2 in split-lock configuration):
  - Configurable as either 4 cores (2 of them in lockstep configuration) or 3 cores (all of them in lockstep configuration)
  - Arm<sup>®</sup> v8-R compliant
  - Single precision floating-point unit (*FPU*)
  - New privilege level for real-time virtualization
  - Up to 500 MHz
- 1 Cortex<sup>®</sup>-M4 multipurpose accelerator running at up to 200 MHz, in lockstep configuration
- 4 *eDMA* engines

### Neural processing unit

- Neural ART Accelerator™ 11
- Energy efficient *NPU* capable of accelerating a wide range of neural network models

### Memories

- *xMemory*: up to 19.5 MB extensible on-chip nonvolatile memory (NVM) depending on ordered part number:
  - PCM (phase-change memory) as nonvolatile memory
  - Up to 19 MB code NVM, with A/B swap *OTA* mechanism (up to 2× 9.5 MB)
  - 512 KB HSM-dedicated code NVM
- 384 KB data NVM (256 KB + 128 KB dedicated to HSM)
- Up to 1792 KB on-chip general-purpose SRAM

### Product summary

Part number	Package
SR6P3EC4	FPBGA292
SR6P3EC6	FPBGA476

### Security: 2<sup>nd</sup> generation hardware security module

- Cybersecurity: ISO/SAE 21434 compliance (refer to the cybersecurity reference manual for details)
- On-chip high-performance security module with full support for e-safety vehicle intrusion protected applications (EVITA)
- Symmetric and asymmetric cryptography processor
- High-performance lock-stepped AES-light security subsystem for fast ASIL-D cryptographic services

### Safety: comprehensive new-generation ASIL-D safety concept

- New state-of-the-art safety measures at all levels of the architecture for most efficient implementation of ISO 26262 ASIL-D functionalities
- Complete hardware virtualization architecture built on Cortex<sup>®</sup>-R52+ new privilege mode (best-in-class software isolation, real-time support for multiple virtual machines/applications)

### Device standby/low-power modes

- Versatile low-power modes
- Ultra-low power: standby mode for lowest quiescent current with optimized active subsystem (for example standby RAM) and wake-up capability
- Smart low-power: smart power mode with Cortex<sup>®</sup>-M4 subsystem, extended communications interfaces, and ADC peripheral

### Peripheral, I/O, and communication interfaces

- 8 LINFlexD modules
- 1 dual-channel FlexRay controller
- 10 queued serial peripheral interface (SPIQ) modules
- 2 microsecond channels (MSC)
- 2 I<sup>2</sup>C interfaces
- 2 SENT modules (10 channels each)
- 2 PSI5 modules (1 channel each)
- Enhanced analog-to-digital converter system with:
  - 12 separate 12-bit SAR analog converters (including one supervisor/safety ADC).
  - 4 separate 9-bit SAR analog converters (2 channels each) with fast comparator mode
  - 1× 9-bit SAR analog converter for device standby/low-power mode
  - 10 separate 16-bit sigma-delta analog converters with embedded DSP processor on each *SDADC*
  - Enhanced interconnection with GTM timer for autonomous ADC/GTM subsystem operation
- Advanced timed I/O capability:
  - Generic timer module (GTM4134)
  - High-resolution timer
- Communication interfaces:
  - One 10/100/1000 Mbit/s Ethernet controller compliant with IEEE 802.3-2008: IPv4 and IPv6 checksum modules, AVB, VLAN, and optionally supporting 10BASE-T1S with the OPEN Alliance 3-pin (OA3p) interface (depending on the ordered part number)
  - 8 modular controller area network (MCAN) modules, supporting CAN classic and CAN FD<sup>®</sup>
  - 2 XS\_CAN modules supporting CAN classic, CAN FD<sup>®</sup> and CAN XL<sup>®</sup>

# 1 Introduction

## 1.1 Document overview

This document provides a summary of the target specification and features of the SR6P3EC4 and SR6P3EC6 devices. For detailed information, refer to the device datasheet and reference manual.

The SR6P3EC4 and SR6P3EC6 devices are based on Arm® cores. For information on the Arm®-Cortex®-R52 and Arm® Cortex®-M4 cores, refer to the technical reference manuals, available from the [www.arm.com](http://www.arm.com) website.

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## 1.2 Description

Stellar integration MCUs are designed to meet the requirements of domain controllers and ECUs with high integration, as required in the architectures of connected, updatable, automated, and electrified cars. They have superior real-time and safe performance (with the highest ASIL-D capability). Bringing hardware-based virtualization technology to MCUs, they ease the development and integration of multiple-source software on the same hardware while maximizing the resulting software performance. They offer high-efficiency OTA reprogramming capability with fast new image download and activation. They also provide high-speed security cryptographic services, for instance for network authentication.

**Table 1. SR6P3EC4 and SR6P3EC6 overview**

Feature		SR6P3EC4 and SR6P3EC6
Cortex®-R52+ cores (+ checker cores)		4 cores (+2 checkers), configurable as 3 cores (+3 checkers)
Neon™ (with SIMD, dual precision floating point)		No
Cache (instruction/data) per core in Kbyte		16/8
Core memory protection unit (regions), several additional protection mechanisms in the architecture, for example: NOC firewalls	Hypervisor (EL2)	24
	OS (EL1)	24
Code NVM	Overall including HSM in Mbytes	Up to 19.5 MB xMemory (depending on the ordered part number)
	Cluster code NVM in Mbytes	Up to 19 MB xMemory (depending on the ordered part number)
	HSM code NVM in Kbytes	512
Data NVM in Kbytes		384
RAM in Kbytes		1792
Hardware security module (HSM) - 2 <sup>nd</sup> generation		Yes
AES-Light (cryptographic services)		2
Arm® Cortex®-M4	Multipurpose accelerator in lockstep (DSPH)	1
	Multi-purpose accelerator in lockstep (DME)	No
eDMA engines (number of channels, more channels through muxes/channel)	Engine	4
	Channel	4× 32
LIN and UART (LINFlexD)		8
CAN_FD		10
CAN_XL		2 (2 common with above CAN_FD channels)

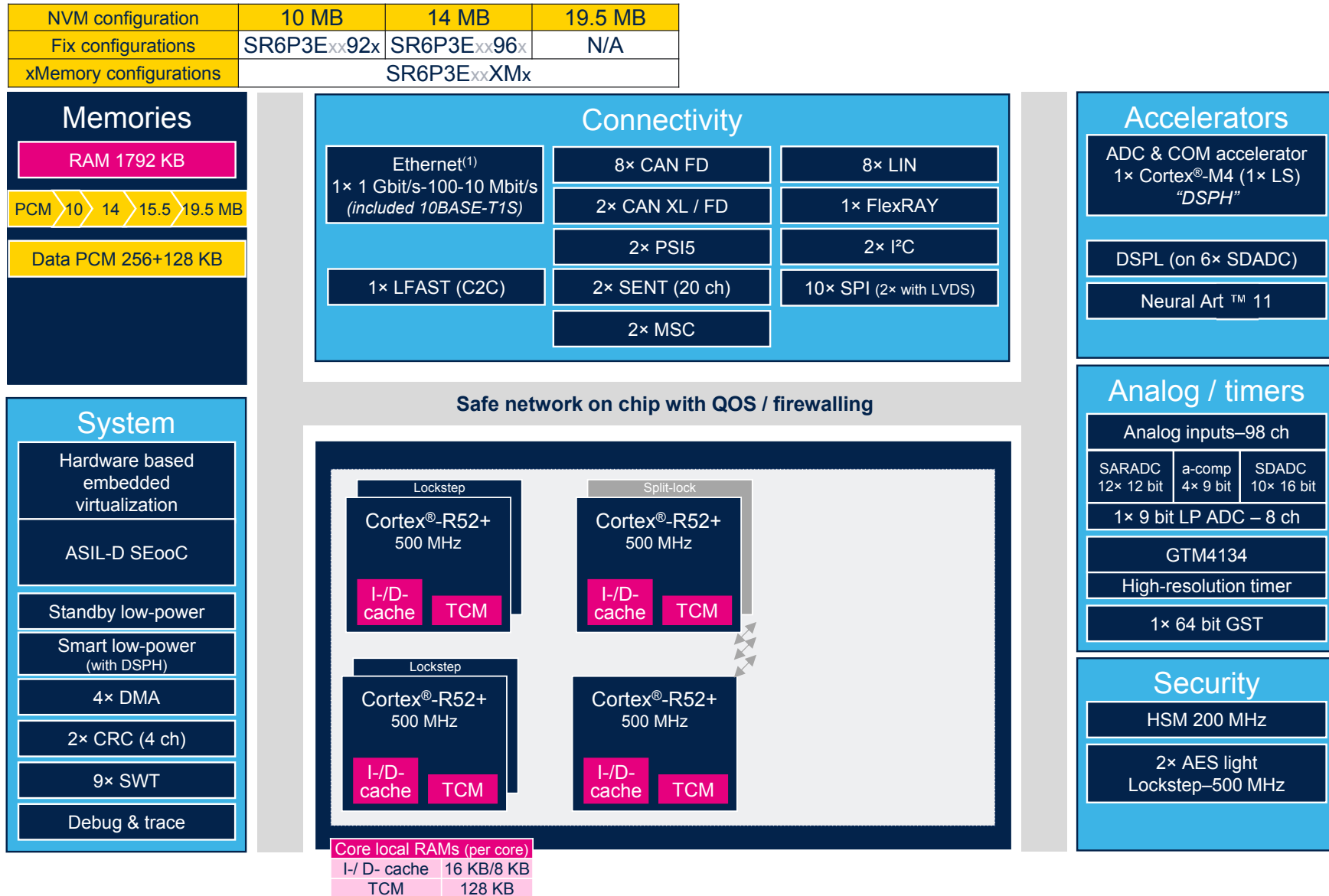
Feature		SR6P3EC4 and SR6P3EC6
SPIQ (with LVDS channel)		10 (2)
Microsecond channel (MSC)		2
SENT	Unit	2
	Channel/unit	10
I <sup>2</sup> C		2
PSI5	Unit	2
	Channel/unit	1 channel
FlexRay™ (dual channel)		1
10/100/1000 Mbit/s Ethernet IEEE 802.3-2008 compliant	Total	1
	With MII, RMII, RGMII, and 10BASE-T1S/OA3pin <sup>(1)</sup>	1
SIPI/LFAST interprocessor bus		1
Generic timer modules GTM4134		Yes 5 MCS (multithreading cores), 40 channels, 120 KB RAM 5 TIM (8 channels each) 3 TOM (16 channels each) 6 ATOM (8 channels each) 4 TIO (8 channels each)
High-resolution timer		2 × 8 channels
12-bit SAR analog converters		12
16-bit sigma-delta analog converters (units with DSPL)		10
9-bit SAR analog comparators		4 units (2 channels each)
Octo-SPI (support HyperBus™ memory devices)		No
Debug port	Main debug port (JTAG+SWD)	Yes
	Secondary debug port (SWD)	Yes
High-speed off-chip trace lane (multi Gbit/s, Aurora™ protocol)		1
Maximum temperature (target)	Junction temperature	150°C
Packages	FPBGA516	—
	FPBGA476	X
	FPBGA348	—
	FPBGA292	X

1. Optional (depending on the ordered part number).

### 1.3 Block diagram

The figure below shows the top-level block diagram.

Figure 1. Block diagram



## 2 Ordering information

Table 2. Ordering information scheme

Example:	SR6	P3E	C6	XM	C5FX	0	R
<b>Device family</b>							
SR6: "Stellar" SR6 family							
<b>Serie / line</b>							
P3E: SR6 P series, P3E line							
<b>Package</b>							
C4: FPBGA292							
C6: FPBGA476							
<b>Memory size</b>							
XM: xMemory configuration, extensible from 10 MB to 19.5 MB							
92: 10 MB fixed memory configuration							
96: 14 MB fixed memory configuration							
<b>Device options</b>							
C5FX: default, without 10BASE-T1S							
C5EX: with 10BASE-T1S							
Others: reserved							
<b>Reserved</b>							
<b>Packing</b>							
Y: Tray							
R: Tape and reel (pin 1 top right)							

## Revision history

**Table 3. Document revision history**

Date	Version	Changes
20-Jan-2025	1	Initial release.
21-Jan-2025	2	<ul style="list-style-type: none"> <li>Peripheral, I/O, and communication interfaces: added "1 dual-channel FlexRay controller" and "Enhanced interconnection with GTM time..."</li> </ul>
15-Jan-2026	3	<ul style="list-style-type: none"> <li>In the whole document,               <ul style="list-style-type: none"> <li>removed the SR6P3EC5 part number and the associated package FPBGA348: document titles, package silhouette, product summary, Table 1. SR6P3EC4 and SR6P3EC6 overview</li> <li>minor editorial changes</li> </ul> </li> <li>changed classification level to "public"</li> <li>Highlights: updated</li> <li>Cores and accelerators: updated section title</li> <li>Memories: updated</li> <li>Peripheral, I/O, and communication interfaces: updated</li> <li>Table 1. SR6P3EC4 and SR6P3EC6 overview: updated</li> <li>Figure 1. Block diagram: updated</li> <li>Table 2. Ordering information scheme: added</li> <li>Glossary updated</li> </ul>
18-Feb-2026	4	<p>The 10BASE-T1S feature is optional. Its availability depends on the ordered part number:</p> <ul style="list-style-type: none"> <li>Peripheral, I/O, and communication interfaces: updated</li> <li>Table 1. SR6P3EC4 and SR6P3EC6 overview: added footnote</li> <li>Figure 1. Block diagram: added footnote</li> <li>Table 2. Ordering information scheme: added new "Device option" code</li> </ul>

## Glossary

**ADC** Analog-to-digital converter

**AEC** Automotive Electronics Council. Also known as CDF-AEC for Chrysler-Delco-Ford Automotive Electronics Council. Shortened to AEC.

**AES** Advanced encryption standard. Cryptographic algorithm.

**ASIL** Automotive safety integrity level - a risk classification system defined by the ISO 26262 standard for the functional safety of road vehicles; there are four ASILs identified by ISO 26262 — A, B, C, and D, from the lowest to the highest degree of automotive hazard

**ATOM** ARU-connected timer output module

**CAN** Controller area network

**CAN FD**<sup>®</sup> Controller area network flexible data rate

**CAN XL**<sup>®</sup> Controller area network extra long

**CPU** Central processing unit

**CRC** Cyclic redundancy check

**DCF** Device configuration format

**DMA** Direct memory access

**DSP** Digital signal processing

**eDMA** Enhanced direct memory access

**EMC** Electromagnetic compatibility

**EVITA** e-safety vehicle intrusion protected applications

**FCCU** Fault collection and control unit

**FPBGA** Fine-pitch-ball-grid-array

**FPU** Floating-point unit

**GB** Gigabyte

**GPIO** General-purpose input/output

**GTM** Generic timer module

**HSM** Hardware security module

**I/O** Input/output

**I2C** Inter-integrated circuit

**IEC** International Electrotechnical Commission

**IEEE** Institute of Electrical and Electronics Engineers

**IPv4** Internet protocol version 4

**IPv6** Internet protocol version 6

**ISO** International Organization for Standardization

**JTAG** Joint Test Action Group

**KB** Kilobyte

**LIN** Local interconnect network

**LVDS** Low-voltage differential signaling

**M\_TTCAN** Time-triggered controller area network

**MB** Megabyte

**MCAN** Modular controller area network

**MCS** Multichannel sequencer

**MCU** Microcontroller unit

**MII** Media-independent interface

**NoC** Network-on-chip

**NPU** Neural processing unit

**NVM** Nonvolatile memory - a memory that retains its contents even when powered down, such as flash memory or EEPROM

**OA3p** OPEN Alliance 3-pin (interface)

**OS** Operating system

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<b>OSR</b>	Oversampling ratio	<b>XS_CAN</b>	Controller area network extra small
<b>OTA</b>	Over the air		
<b>PHY</b>	Physical layer		
<b>PLL</b>	Phase-locked loop		
<b>PSI5</b>	Peripheral sensor interface (PSI5). An interface for automotive sensor applications.		
<b>RAM</b>	Random access memory		
<b>RGMII</b>	Reduced gigabit media-independent interface		
<b>RMII</b>	Reduced media-independent interface		
<b>SAR</b>	Successive approximation register		
<b>SDADC</b>	Sigma-delta analog-to-digital converter		
<b>SENT</b>	Single-edge nibble transmission for automotive applications		
<b>SIMD</b>	Single-instruction multiple data		
<b>SIPI</b>	Serial interprocessor interface		
<b>SPI</b>	Serial peripheral interface		
<b>SPIQ</b>	Queued serial peripheral interface		
<b>SRAM</b>	Static random-access memory		
<b>SRC</b>	Sample rate converter		
<b>ST</b>	STMicroelectronics		
<b>SWD</b>	Serial wire debug		
<b>TIM</b>	Timer input module		
<b>TIO</b>	Timer input/output module		
<b>TOM</b>	Timer output module		
<b>UART</b>	Universal asynchronous receiver/transmitter		
<b>VLAN</b>	Virtual local area network		
<b>xMemory</b>	Extensible embedded nonvolatile memory		

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