Secure dual interface microcontroller with enhanced security and up to 450 Kbytes of Flash memory

Features

Hardware features

- Arm® SecurCore® SC000™ 32-bit RISC core cadenced at up to 55 MHz
- 10 Kbytes of User RAM
- Up to 450 Kbytes of secure User high-density Flash memory including 512 bytes of User OTP area:
  - 25-year data retention
  - 500 000 Erase/Write cycle endurance
  - Page Erase time: 0.8 ms
  - Programming performance up to 2 µs/byte in chained mode
  - Flash Erase/Write protection programmable on 32-Kbyte sectors
- Operating temperature: –25 °C to +85 °C
- Three 16-bit timers with interrupt
- Watchdog timer
- 2.7 V to 5.5 V supply voltages
- External clock frequency up to 10 MHz
- Power-saving Standby state
- Contact assignment compatible with ISO/IEC 7816-3 standards
- ESD protection (HBM): 6 kV HBM for ISO pads and 4 kV for AC0/AC1 contactless pads
- Asynchronous receiver transmitter (IART) with RAM buffer for high speed serial data support (ISO/IEC 78163 T=0/T=1 and EMV compliant)

Contactless features

- Complies with ISO/IEC 14443 Type A and EMVCo™
- 68 pF tuning capacitor
- Automatic CPU frequency adaptation for optimum power consumption
- 13.56 MHz carrier frequency
- RFUART (RF universal asynchronous receiver transmitter) up to 848 kbps
- 1-Kbyte RF frame buffer in dedicated RFUART RAM
- MIFARE Classic®, MIFARE Plus® and MIFARE® DESFire® EV2 hardware and software implementation

Security features

- Active shield
- Monitoring of environmental parameters
- Three-key Triple DES accelerator
- AES accelerator
- AIS-31 Class PTG.2 compliant true random number generator (TRNG)
- NESCRIPT coprocessor for public key cryptography algorithm
- ISO/IEC 13239 CRC calculation block
- Unique serial number on each die
- Highly efficient protection against fault attacks
1 Description

Designed for secure ID and banking applications, the ST31P450 devices are serial access microcontrollers that incorporate the most recent generation of Arm® processors for embedded secure systems. Their SecurCore® SC000™ 32-bit RISC core is built on the Cortex® M0 core with additional security features to help to protect against advanced forms of attacks.

Cadenced at 55 MHz, the SC000™ core brings great performance and excellent code density thanks to the Thumb®-2 instruction set.

Certain devices implement the MIFARE Classic®, MIFARE® DESFire® EV2 or MIFARE Plus® technology. An RF interface including an RF universal asynchronous receiver (RFUART) enables contactless communication up to 848 kbps compatible with the ISO/IEC 14443 Type A standard. The ST31P450 devices also offer a serial communication interface fully compatible with the ISO/IEC 7816-3 standard (T=0, T=1).

Three 16-bit general-purpose timers are available as well as a watchdog timer.

The ST31P450 devices feature hardware accelerators for advanced cryptographic functions. The AES accelerator provides a high-performance implementation of the AES-128, AES-192 and AES256 algorithms. The 3-key Triple DES accelerator (EDES+) peripheral enables Cipher block chaining (CBC) mode, fast DES and triple DES computation based on three key registers and one data register, while the NESCRYPT cryptoprocessor efficiently supports the public key algorithm with native operations up to 4096 bits long.

The ST31P450 devices operate in the –25 to +85 °C temperature range, in the 2.7 V and 5.5 V supply voltage ranges in Contact mode, and comply with ISO/IEC 14443 specification limits. A comprehensive range of power-saving modes enables the design of efficient low-power and contactless applications.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere. MIFARE, MIFARE Classic, MIFARE DESFire and MIFARE Plus are trademarks of NXP B.V. and are used under license.
## Revision history

### Table 1. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>29-Jun-2018</td>
<td>1</td>
<td>Initial release.</td>
</tr>
<tr>
<td>09-Aug-2019</td>
<td>3</td>
<td>Modified ESP protection (HBM) value in Features. Updated MIFARE Classic® data in Features and in Section 1 Description. Removed Figure 1.</td>
</tr>
</tbody>
</table>
IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics – All rights reserved