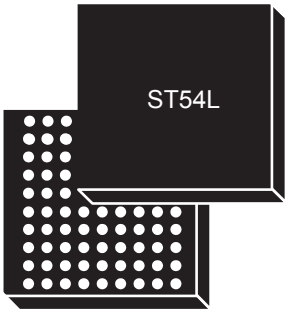
NFC controller and secure element system in package



90 ball WLCSP

Product status link
ST54L

Features

- Single die integrating an NFC controller (contactless front-end - CLF) and a secure element (SE)
- Small package WLCSP90, ECOPACK-compliant

NFC controller

- Arm® Cortex®-M3 microcontroller
- 100% re-flashing capability for firmware update
- Enhanced active load modulation technology
- Enhanced Tx drive up to 2W
- Support of external DC/DC up to 5.5 V
- Highest output power with optimized power transfer
- Optimized for extremely small or metal frame antennas
- Optimized Low-power consumption modes
- Selectable ultralow power hibernate state
- Battery voltage monitoring
- Proprietary in-frame synchronization (IFS) in card emulation (CE) to ensure stability in battery low and switched off modes
- Improved XOR mode on all technologies
- OOFS with external reference clock in CE
- System clock
  - Fractional-N PLL input range of 19.2 to 76.8 MHz
  - Support of multiple external crystal oscillator (27.12 MHz and 54.24 MHz)
- 32.768 kHz, 16MHz and 32MHz support for EMC tests
- Automatic wakeup via communication interfaces, GPIO, RF field or tag detection and power supply detection

RF communications

- Active and passive peer-to-peer
  - ISO/IEC 18092 - NFCIP-1 initiator and target
- Reader/writer mode
  - NFC Forum™ Type 1/2/3/4/5 tags
  - FeliCa™
  - ISO/IEC 15693
  - MIFARE®(1)
- Card emulation mode
  - ISO/IEC 14443 Type A & B
  - FeliCa™
  - Intelligent Card Switching
  - MIFARE®

1. *MIFARE R/W mode feature availability is pending on license conditions. Contact your local ST representative for further information.*

Communication interfaces

- I3C interfaces:
  - ST54L_CLF
    - 1 target up to 12.9 MHz
    - 1 controller - target up to 12.9 MHz
    - 1 controller up to 12.9 MHz
  - ST54L_SE
    - 1 target up to 12.9 MHz
    - 1 target up to 10 MHz
    - 1 controller - target up to 12.9 MHz
- SPI interface:
  - ST54L_CLF:
    - 1 master up to 17 MHz
    - 1 master (up to 17 MHz) - slave (up to 26 MHz)
  - ST54L_SE:
    - 1 slave up to 26 MHz
    - 1 master (up to 21 MHz) - slave (up to 26 MHz)
- I^2C interface supporting standard, Fast, and Fast+ modes.
- SWP master interfaces up to 1.695 Mbit/s:
  - 2 SWP UICC support
  - 1 SWP external SE support
- ISO/IEC 7816-3 interface
- GPIOs
- Dedicated Chip Enable pins for the ST54L_SE/ST54L_CLF

Secure microcontroller

- Arm® Cortex® M35P 32-bit RISC core
- 3.3 Mbytes of flash memory
- 4 Kbytes memory cache
- 100 Kbytes of user RAM
- Selectable ultralow power hibernate and standby states
- Supports state-of-the-art secure element operating systems
- CC EAL6+ certification
- Hardware security-enhanced DES & AES accelerators
- MIFARE Classic®(1) cryptography hardware accelerator
- NESCRYPT coprocessor for public key cryptography algorithm
- Supports embedded-SIM (eSIM) applications in compliance with the GSMA specification
- Secure ranging support in connection with an external UWB sub-system

Electrical characteristics

- Battery voltage support from 2.4 V to 5.1 V
- I/O dedicated voltage level (V_{PS_IO}): 1.2 V and 1.8 V compatibility
- Supports Class B and C operating conditions for UICC – Class D ready
- Ambient operating temperature -30 to + 85 °C

Application

- Mobile devices

- Wearable devices
- Smartwatch
- Secure connected devices

1 Description

The ST54L is a single-die solution integrating a contactless front-end (ST54L_CLF) and a secure element (ST54L_SE). It is designed for integration in mobile devices and NFC-compliant products.

1.1

The ST54L_CLF includes near-field communication (NFC) functions in the three operating modes: card emulation, reader/writer and peer-to-peer communication. It is based on an advanced Arm® Cortex®-M3 32-bit microcontroller. The ST54L_CLF is designed to increase RF communication distances, ease NFC technology integration, and operate in efficient low power modes.

The ST54L_CLF is best in class in terms of RF output power, working up to 2W. Maximum power can be safely used to communicate thanks to a dynamic control: when a card is close, power is automatically reduced to ensure interoperability and standard compliance. To go with this outstanding output power, demodulation sensitivity is improved to maximize the communication distance with all types of cards.

The ST54L_CLF card emulation mode does not require any external oscillator nor reference clock source. Thanks to active load modulation and automatic adjustments based on field strength, communication distance is maximized, and interoperability is ensured.

The ST54L_CLF can operate in a very low power modes while detecting, thanks to an improved field detection sensitivity and a stable and efficient low power card detection mechanism, the presence of a reader, a card, or a tag beyond its rated communication distance.

The ST54L_CLF exchanges data with the device application processor over the NCI 2.1 logical interface on top of the I^2C connection. It features three external SWP master interfaces and one internal SWP master interface to control the embedded SE (ST54L_SE). Thanks to an enhanced power switch system, the ST54L_CLF manages its own power supply and that of the associated secure elements (comprising ST54L_SE, UICC_1 and UICC_2).

1.2 ST54L_SE

The ST54L_SE is a serial access microcontroller designed for secure mobile applications. It incorporates the most recent generation of Arm® processors for embedded secure systems. Their SecurCore® Cortex®-M35P 32-bit RISC core is built on the Cortex®-M33 core with additional security features to help protect against advanced forms of attack.

The ST54L_SE provides high performance thanks to a fast Cortex®-M35P processor, crypto-accelerators and improved flash memory operation. The Cortex®-M35P core and its cache memory bring great performance and excellent code density thanks to the Thumb®-2 instruction set.

Strong and multiple fault protection mechanisms ensure a guaranteed high-detection coverage that facilitates the development of highly secure software. This is achieved by using two CPUs in locked-step mode, error codes in sensitive memories and hardware logic.

The ST54L_SE features hardware accelerators for advanced cryptographic functions. The EDES peripheral provides a secure DES (Data encryption standard) algorithm implementation, while the NESCRYPT FAST cryptographic processor efficiently supports the public key algorithm. The AES peripheral ensures secure and fast AES algorithm implementation.

A comprehensive range of power-saving modes enables the design of efficient low-power applications.

The ST54L_SE platform offers a serial communication interface that is fully compatible with the ISO/IEC 7816-3 standard (T=0, T=1), and is intended for use in embedded SIM (eSIM) applications.

It includes a single-wire protocol (SWP) interface that internally connects to the ST54L_CLF.

Multiple ST54L_SE interfaces provide flexible connection to subsystems such as UWB companion device to manage CCC Digital Key Release 3.0 compliant and FiRa compliant secure ranging.

The MIFARE® R/W mode feature availability depends on the license conditions. Contact your local ST representative for further information.

1.3 ST54L package

The ST54L is manufactured in an ECOPACK-compliant, 3.475 × 3.667 mm, 90-ball wafer-level chip-scale package (WLCSP). To meet integration needs, the WLCSP is available in two thicknesses, 0.33 mm and 0.51 mm.

In order to meet environmental requirements, ST offers the ST54L devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

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Revision history

Table 1. **Document revision history**

Date	Revision	Changes
07-Jun-2023	1	Initial release
17-Oct-2023	2	Updated Section Features

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