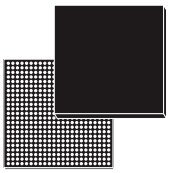
STA1195

Telemaco3 family of telematics and connectivity processors

Data brief



LFBGA529
(19x19x1.7 mm)

GADG1711161004PS

Features

Core and infrastructure

- ARM® Dual Core CortexA7 up to 600 MHz, with NEON instructions
- Memory organization:
  - L1 Cache: 32 KB instruction, 32 KB data
  - 256 KB L2 Cache
  - Total 768 KB embedded SRAM
  - 16/32-bit DDR3 Controller at 667 MHz
  - Serial SQI NOR interface
  - 16bit Parallel NAND Controller
- 32-bit watchdog timer
- 16-channels DMA
- 8x 32-bit free running times/counters
- 5x 16-bit extended function timer (EFT) with input capture/output compare and PWM
- Real time clock (RTC) with fraction readout

Media interfaces

- 3x Secure-digital multimedia memory card Interface
- 2x USB 2.0 Dual Role with integrated PHY; charger function supported
- 1x RMII/RGMII Ethernet AVB MAC

Embedded secure vehicle interface microcontroller

- Dedicated Cortex M3 core
- 256 KB Isolated embedded memory (part of the total 768 KB core eSRAM)
- Secured NOR interface
- 3x CAN port, 2x supporting FD CAN
- Hardware Crypto Engine
- Programmable OTP for key storage, lifecycle management, anti-rollback

I/O Interfaces

- 16-channels 12-bits ADC
- 3x I2C multi-master/slave interfaces
- 4x UART Controller
- 3x Synchronous Serial Port (SSP/SPI)
- 5x 32-bit GPIO ports
- JTAG based in-circuit emulator (ICE) with Embedded Trace Module

Optional Audio Subsystem

- Sound processing DSP (450 MIPS)
- 3 Stereo channels Hardware Sample Rate converter
- 3x Audio DAC with 100 dB SNR
- 6x Rx/Tx Audio interfaces (I2S/ multi-channel ports, with SPI mode)
- 2x Differential Mono ADC for Voice/Tel-IN with internal switching logic; 105 dB SNR
- 1x Stereo AUX ADC

Operating Conditions

- VDD: 1.14 V - 1.26 V
- VDDIO: 3.3 V ±10%
- DDR3 VDDQ: 1.35 V ±5%
- DDR3 VREF: VDDQ/2
- VDDIOON: 3.3 V ±10%
- Ambient temperature range: -40 to 85 °C

Table 1. Device summary

Order code	Package	Packing
STA1195	LFBGA529 19x19x1.7mm	Tray

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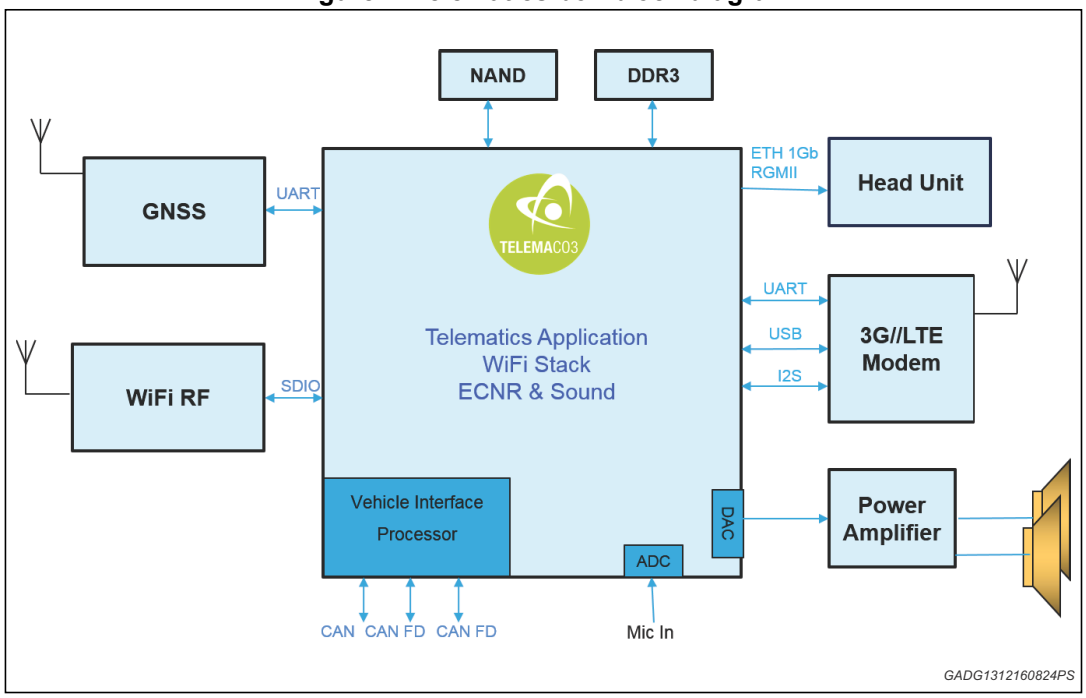
1 Description

STA1195 is a fully automotive, multi-processor System-On-Chip, targeting processor-centric Telematics Applications offering superior processing power for high-bandwidth data traffic management.

It features:

- A powerful Dual CortexA7 processor;
- A dedicated ARM - Cortex M3 controller for real-time CAN / Vehicle Interface Processing;
- An HW Crypto engine for efficient security performances;
- A complete set of standard connectivity interfaces including 1Gbit Ethernet;
- An optional Audio Subsystems tailored to Audio Connectivity applications (i.e. Sound Boxes).

Figure 1. Telematics box block diagram



2 System description

2.1 Application processor

STA1195 processing capability relies on an ARM Dual Cortex-A7 running at up to 600MHz, delivering ~2400 DMIPS with minimal heat dissipation requirements. The application processor has 32 KB of instruction cache and 32 KB of data cache, as well as 256 KB of L2 cache for high throughput and low latency tasks. The dual core implementation is equipped with a dedicated PLL and power domain, in order to achieve best thermal/MIPS performance compromise in all application scenarios.

The application processor is connected to the system via an efficient bus matrix infrastructure, implementing flexible QoS and trust zone features.

2.2 Memory architecture

2.2.1 Embedded memory

STA1195 embeds 768 KB of 64 bits SRAM memory clocked at 200MHz, which can be used for secure data storage. The whole embedded memory is also cacheable and can be accessed by DMA.

2.2.2 DDR controller

DDR controller supports DDR3 JEDEC interface 16 or 32 bits wide, clocked at up to 667 MHz, allowing an optimal solution for throughput intensive applications.

Such memory is cacheable, can be accessed by DMA, and is flexibly configurable as secure/non-secure.

2.2.3 SQI NOR interface

The SQIO controller allows interfacing Serial Quad I/O flash memories up to 133MHz (SDR)

Main features are:

- Direct flash memory access;
- Fast memory access through page buffer (256 bytes);
- Programmable single or quad I/O flash interface.

SQI memory space can be partitioned in order to reserve a portion of the NOR device to the Secure CAN Subsystem.

2.2.4 Parallel memory interface

FSMC static memory controller, provides a generic 16-bits parallel interface suitable to connect SRAM and NAND devices. This peripheral allows execution in-place from SRAMs, as well as DMA accesses. Such interface can be used to store boot code into NAND.

2.3 SD/MMC

STA1195 is equipped with 3 SDMMC controllers, which allow interfacing to either mass storage devices, or to Wi-Fi modules.

Two interfaces implement the following specification:

- eMMC - MultiMedia Card 5.1:
  - 26/52 MHz,
  - 1, 4, 8-bit of data.
- SD/SDIO 3.0:
  - 4-bit interface,
  - SDSC/SDHC/SDXC up to SDR25 (0-50 MHz).

Both interfaces can be used in conjunction with DMA to efficiently implement data transfer with minimal CPU load for handling interrupts.

A third controller, with dedicated DMA engine implementing:

- eMMC - MultiMedia Card 5.1:
  - 26/52 MHz,
  - 1, 4, 8-bit of data.
- SD/SDIO 3.0:
  - 4-bit interface,
  - SDSC/SDHC/SDXC up to SDR50 (0-100 MHz).

2.4 USB

STA1195 has two Dual role USB HS controllers, both with embedded PHY, allowing to efficiently connect to mass storage devices, as well as portable devices (phones, pads). Along with USB connectivity, STA1195 fully supports USB charger specification, implementing DCP protocol specification to provide high current to connected DP devices. The controller supports HS 480-Mbps using an EHCI Host Controller, as well as FS and LS modes through an integrated OHCI interface.

USB controller implements a boot-able interface, useful for production flashing, as well as to debug system post production.

2.5 Sound Subsystem

STA1195 implements a DSP subsystem which allows to efficiently handle intensive sound processing tasks, such as audio chimes generation, spatialization, equalizer or ECNR, without loading the main CPU with interrupt intensive tasks. The sound subsystem is composed of a set of audio interfaces, an isochronous bus, a DSP delivering 450 MIPS, and a 3 stereo channels sample rate converter.

2.5.1 Audio Interfaces

A complete set of audio interfaces is provided, in order to simplify integration with amplifiers, and input sources. Each interface can be routed to the sound subsystem. A complete list of audio interfaces is provided below:

- 1x AUX ADC;
- 2x Voice ADC for high quality Hands Free at 8/16/24kHz;
- 3x Stereo DAC delivering;
- 3x i2s IN;
- 3x i2s OUT;
- 1x MSP IN/OUT, TDM capable.

2.5.2 Routing and Sample Rate Converter

Each audio interface can be routed in both directions (IN/OUT) through sample rate converters, which allow normalizing the sampling rate to the sound processing engine. The audio routing infrastructure is designed to deliver high quality sample rate conversion on multiple channels, allowing simultaneous audio streams, such as Bluetooth Hands Free and audio media playback, to be handled without CPU load.

In order to generate multiple sampling rate audio frequencies, a dedicated fractional PLL is also provided.

2.5.3 Sound DSP

STA1195 is equipped with three 150 MIPS 24-bit fixed point Harvard architecture DSPs (for a total of 450 MIPS) dedicated to sound processing, fully integrated with the sound subsystem with a specific isochronous bus. DSPs are provided with an integrated sound processing library implementing effects like Gain, Balancing and Equalizer.

Each DSP is connected to other DSPs and audio peripherals by means of a programmable isochronous bus infra-structure which guarantees a controlled throughput and latency for all audio transfers.

2.6 Ethernet MAC Controller

Connection to Ethernet infrastructure is supported by the ETH MAC, which can be connected to an external phy with either RGMII or RMII interfaces. Ethernet MAC also implements AVB features, and is compatible with the following standards:

- IEEE 1588-2008 for precision networked clock synchronization.
- IEEE 802.1AS-2011 and 802.1-Qav-2009 for Audio Video (AV) traffic.
- RGMII/RTBI specification version 1.3 from HP/Marvell.
- RMII specification version 1.2 from RMII consortium.

MAC controller has separate channels or queues for AV data transfer in 100 Mbps and 1000 Mbps modes with single Tx/Rx FIFOs for all selected queues.

2.7 System DMA

DMA is designed to efficiently perform memory to memory, and memory to peripherals transfers, offloading such tasks from the processor, thus reducing interrupt handling load. DMA provides 16 independent channels which can be dynamically assigned to different data-path. Complex Scatter/gather transfers can be implemented by programming specific DMA command linked lists.

2.8 Secure CAN Subsystem

STA1195 allows isolating critical code from main application by implementing a dedicated subsystem based on ARM Cortex-M3, along with:

- 256 KB dedicated embedded SRAM (part of total 768 KB eSRAM mentioned in *2.2.1*;
- Interrupt controller;
- Timers;
- 1x CAN controller, implementing CAN;
- 2x CAN Controllers implementing FD-CAN;
- Dedicated GPIOs;
- Dedicated Wakeup lines;
- Back-up RAM in always on domain;
- Local RTC;
- Secure OTP, user programmable, for secure key storage, life cycle management, monotonic counter for anti-rollback protection.

All of the above can be completely isolated from the rest of the system. This subsystem can be dedicated to implement secure features, such as boot authentication, as well as interrupt intensive tasks to offload main CPU. The secure subsystem communicates with the application running on CortexA7 using a Hardware Mailbox interrupt based mechanism.

2.9 Crypto Accelerator Engine

In order to efficiently support security,STA1195 embeds a dedicated, flexible hardware accelerator for the following set of cryptographic operations:

- DES, TripleDES;
- AES 128, 192, 256:
  - Modes of operation: ECB, CBC, CTR, XTS, CCM, GCM, CFB, OFB, CMAC;
- SHA1, SHA256, SHA384, SHA512 with HMAC;
- Public Key Accelerator for RSA, DH, Elliptic Curve Cryptography;
- TRNG, for Random number generation, compliant with NIST SP800-90B;

These cryptographic acceleration features, along with the embedded secure OTP, the trustZone aware bus infrastructure, and secure ROM boot, provide a complete set of components to build a secure system, for data confidentiality, integrity, as well as code integrity and rollback protection.

2.10 General Purpose ADC

The system is equipped 16-inputs SAR ADC with a resolution of 12-bits and sampling frequency up to 2.5 MHz. 6 of them are capable of HW continuous threshold comparison.

2.11 GPIOs

STA1195 has a total of 160 GPIOs, which can be independently configured either as INPUT or OUTPUT. In order to make the system flexible, these IOs are multiplexed on PINs with other peripherals (alternate function scheme is provided as a separate document).

GPIOs are divided into 3 sets:

- 128 Application GPIOs:

  Most of system digital IOs are exposed as alternate functions of application GPIOs. This allows maximum flexibility in system definition.
- 16 Secure GPIOs (s_GPIO):

  This set of GPIOs can be selectively configured as secure, in order to securely control IO functionality, for secure blocks which expose an interface.
- 16 M3_GPIOs:

  This set of IOs is dedicated, in secure-mode, to the Cortex-M3 microcontroller and its peripherals. Cortex A7 can access them in non-secure mode only.

2.11.1 Application GPIO Alternate function mapping

Table 2. Application GPIO Alternate function mapping

GPIO	ALT A	ALT B	ALT C
GPIO0	SDMMC1_CMD	SDMMC0_DAT2_DIR	SAI4_TX1
GPIO1	SDMMC1_CLK	SDMMC0_DAT31_DIR	SAI4_TX2
GPIO2	SDMMC1_DATA_0	SDMMC0_DATA_4	SAI4_TX0
GPIO3	SDMMC1_DATA_1	SDMMC0_DATA_5	SAI4_BCLK
GPIO4	SDMMC1_DATA_2	SDMMC0_DATA_6	SAI4_FS
GPIO5	SDMMC1_DATA_3	SDMMC0_DATA_7	SAI4_RX0
GPIO6	SQI_FDBSCK	CD_SS_MON_1	SDMMC1_DAT0_DIR
GPIO7	AUDIO_REFCLK	SAI2_TX	I2S2_TX
GPIO8	SAI3_BCLK	SDMMC1_CMD	SAI4_RX2
GPIO9	SAI3_FS	SDMMC1_CLK	SAI4_RX1
GPIO10	SAI3_RX2	SDMMC1_DATA_0	EFT2_OCMP1
GPIO11	SAI3_TX1	SDMMC1_DATA_1	EFT2_ICAP1
GPIO12	SAI3_TX2	SDMMC1_DATA_2	UART2_TX
GPIO13	SAI3_RX1	SDMMC1_DATA_3	UART2_RX
GPIO14	SAI3_TX0	SDMMC0_DAT0_DIR	I2C2_SCL
GPIO15	SAI3_RX0	SDMMC1_DAT31_DIR	I2C2_SDA
GPIO16	SAI2_BCLK	FSMC_DACK	I2S2_BCLK
GPIO17	SAI2_FS	FSMC_DREQ	I2S2_FS
GPIO18	SAI2_RX/TX	SPDIF_RX	I2S2_RX
GPIO19	SAI1_BCLK	SPI2_TXD	EFT2_OCMP0
GPIO20	SAI1_FS	SPI2_RXD	EFT2_OCMP1
GPIO21	SAI1_RX	SPI2_SCK	EFT2_EXTCK
GPIO22	I2S0_BCLK	SAI4_BCLK	–
GPIO23	I2S0_FS	SAI4_FS	–
GPIO24	I2S0_TX	SAI4_TX0	–
GPIO25	I2S0_RX	SAI4_RX0	–
GPIO26	EFT0_ICAP0	EFT0_EXTCK	SPI2_SS
GPIO27	EFT0_ICAP1	SDMMC0_CMDDIR	SPI2_TXD
GPIO28	EFT0_OCMP0	UART1_TX	SPI2_RXD
GPIO29	EFT0_OCMP1	UART1_RX	SPI2_SCK
GPIO30	EFT1_ICAP0	EFT1_EXTCK	USB1_DRVVBUS
GPIO31	EFT1_ICAP1	SDMMC0_FBCLK	FSMC_DACK
GPIO32	EFT1_OCMP1	SDMMC0_PWR	SDMMC1_FBCLK

Table 2. Application GPIO Alternate function mapping (continued)

GPIO	ALT A	ALT B	ALT C
GPIO33	EFT1_OCMP0	SDMMC0_DAT31_DIR	FSMC_DREQ
GPIO34	SPI1_SS	EFT0_EXTCK	I2C1_SCL
GPIO35	SPI1_TXD	EFT1_EXTCK	I2C1_SDA
GPIO36	SPI1_RXD	EFT1_OCMP1	UART3_TX
GPIO37	SPI1_SCK	EFT1_OCMP0	UART3_RX
GPIO38	ETH_MDIO	UART1_TX	EFT1_ICAP0
GPIO39	ETH_MDC	UART1_RX	EFT1_ICAP1
GPIO40	UART1_TX	SDMMC0_DATA_4	SDMMC1_DATA_4
GPIO41	UART1_RX	SDMMC0_DATA_5	SDMMC1_DATA_5
GPIO42	UART2_RX	SDMMC0_DATA_6	SDMMC1_DATA_6
GPIO43	UART2_TX	SDMMC0_DATA_7	SDMMC1_DATA_7
GPIO44	UART3_RX	UART1_CTS	EFT2_ICAP0
GPIO45	UART3_TX	UART1_RTS	EFT2_ICAP1
GPIO46	I2C1_SDA	EFT0_OCMP0	EFT0_ICAP1
GPIO47	I2C1_SCL	EFT0_OCMP1	EFT0_ICAP0
GPIO48	EFT2_ICAP0	EFT2_OCMP0	EFT2_EXTCK
GPIO49	I2C1_SDA	FSMC_SMADQ_8	SDMMC1_CMDDIR
GPIO50	I2C1_SCL	FSMC_SMADQ_9	SDMMC1_DAT31_DIR
GPIO51	WDG_SW_RSTOUT	CLKOUT1	SDMMC1_DAT2_DIR
GPIO52	–	–	–
GPIO53	–	UART1_TX	WDG_SW_RSTOUT
GPIO54	–	UART1_RX	–
GPIO55	–	–	–
GPIO56	–	–	–
GPIO57	–	–	–
GPIO58	–	–	–
GPIO59	–	–	–
GPIO60	–	–	–
GPIO61	–	–	–
GPIO62	–	–	–
GPIO63	–	–	–
GPIO64	–	–	–
GPIO65	–	–	–
GPIO66	–	–	–

Table 2. Application GPIO Alternate function mapping (continued)

GPIO	ALT A	ALT B	ALT C
GPIO67	–	SPI1_TXD	UART1_RTS
GPIO68	–	SPI1_RXD	UART1_CTS
GPIO69	–	SPI1_SS	UART1_TXD
GPIO70	–	SPI1_SCK	UART1_RXD
GPIO71	–	I2C2_SCL	–
GPIO72	–	I2C2_SDA	–
GPIO73	–	–	–
GPIO74	–	–	–
GPIO75	–	–	–
GPIO76	–	–	–
GPIO77	–	–	–
GPIO78	–	–	–
GPIO79	–	–	–
GPIO80	–	–	–
GPIO81	–	–	–
GPIO82	–	–	–
GPIO83	–	–	–
GPIO84	–	–	–
GPIO85	–	FSMC_ADVn	–
GPIO86	–	FSMC_CS0n	–
GPIO87	–	SPI2_TXD	–
GPIO88	–	SPI2_RXD	–
GPIO89	–	SPI2_SS	–
GPIO90	–	SPI2_SCK	–
GPIO91	–	WDG_SW_RSTOUT	–
GPIO92	FSMC_SMADQ_7	SDMMC2_CMD	–
GPIO93	FSMC_SMADQ_6	SDMMC2_CLK	–
GPIO94	FSMC_SMADQ_5	SDMMC2_DATA_0	–
GPIO95	FSMC_SMADQ_4	SDMMC2_DATA_1	–
GPIO96	FSMC_SMADQ_3	SDMMC2_DATA_2	–
GPIO97	FSMC_SMADQ_2	SDMMC2_DATA_3	–
GPIO98	FSMC_SMADQ_1	SDMMC2_DATA_4	–
GPIO99	FSMC_SMADQ_0	SDMMC2_DATA_5	–
GPIO100	FSMC_WPn	SDMMC2_DATA_6	–

Table 2. Application GPIO Alternate function mapping (continued)

GPIO	ALT A	ALT B	ALT C
GPIO101	SQI_CE1n	SPI2_SS	–
GPIO102	FSMC_BUSYn	SDMMC2_DATA_7	–
GPIO103	FSMC_OEn	SDMMC2_FBCLK	–
GPIO104	FSMC_WEn	I2C2_SDA	–
GPIO105	FSMC_SMAD17/ALE	I2C2_SCL	–
GPIO106	FSMC_SMAD16/CLE	UART2_RX	–
GPIO107	FSMC_NAND_CS0n	UART2_TX	–
GPIO108	SQI_SIO3	SAI4_BCLK	FSMC_SMADQ_10
GPIO109	SQI_SIO2	SAI4_FS	FSMC_SMADQ_11
GPIO110	SQI_SIO1	SAI4_TX0	FSMC_SMADQ_12
GPIO111	SQI_SIO0	SAI4_TX1	FSMC_SMADQ_13
GPIO112	SQI_SCK	SAI4_RX0	FSMC_SMADQ_14
GPIO113	SQI_CE0n	SAI4_RX1	FSMC_SMADQ_15
GPIO114	I2C2_SDA	SDMMC0_DAT0_DIR	ETH_MDIO
GPIO115	I2C2_SCL	SDMMC0_DAT31_DIR	ETH_MDC
GPIO116	ETH_TXEN	SPI2_TXD	I2S2_TX
GPIO117	ETH_TX[0]	SPI2_RXD	I2S2_RX
GPIO118	ETH_TX[1]	SPI2_SS	I2S2_FS
GPIO119	ETH_RXDV_CRS	SPI2_SCK	I2S2_BCLK
GPIO120	ETH_RX[0]	–	–
GPIO121	ETH_RX[1]	–	–
GPIO122	ETH_RMII_CLK	ETH_MII_RX_CLK	–
GPIO123	ETH_TX[2]	UART2_RX	–
GPIO124	ETH_TX[3]	UART2_TX	–
GPIO125	ETH_RX[2]	–	–
GPIO126	ETH_RX[3]	UART3_RX	–
GPIO127	ETH_MII_TX_CLK	UART3_TX	–

2.11.2 Secure GPIO Alternate function mapping

Table 3. Secure GPIO Alternate function mapping

GPIO	ALT A	ALT B	ALT C
S_GPIO0	EFT3_ICAP0	EFT3_OCMP0	CAN1_RX
S_GPIO1	EFT3_ICAP1	EFT3_OCMP1	CAN1_TX
S_GPIO2	EFT4_ICAP0	SPI0_RXD	EFT4_EXTCK
S_GPIO3	EFT4_ICAP1	EFT4_OCMP1	CAN_2_RX
S_GPIO4	EFT3_OCMP0	SPI0_TXD	EFT3_EXTCK
S_GPIO5	EFT3_ICAP1	EFT4_OCMP0	EFT3_OCMP1
S_GPIO6	SPI0_TXD	EFT4_ICAP1	EFT4_EXTCK
S_GPIO7	SPI0_RXD	EFT4_OCMP1	CAN_2_TX
S_GPIO8	SPI0_SCK	–	–
S_GPIO9	SPI0_SS	–	–
S_GPIO10	I2C0_SDA	EFT4_ICAP0	–
S_GPIO11	I2C0_SCL	EFT4_OCMP0	–
S_GPIO12	UART0_RX	CAN_2_TX	–
S_GPIO13	UART0_TX	CAN_2_RX	–
S_GPIO14	UART0_CTS	EFT4_ICAP1	–
S_GPIO15	UART0_RTS	EFT4_OCMP1	–

2.11.3 Cortex- M3 GPIO Alternate function mapping

Table 4. Cortex- M3 GPIO Alternate function mapping

GPIO	ALT A	ALT B	ALT C
M3_GPIO0	WAKE0	–	–
M3_GPIO1	WAKE1	–	–
M3_GPIO2	WAKE2	–	–
M3_GPIO3	WAKE3	–	–
M3_GPIO4	WAKE4	–	–
M3_GPIO5	WAKE5	–	–
M3_GPIO6	WAKE6	–	–
M3_GPIO7	WAKE7	–	–
M3_GPIO8	CAN0_TX	–	–
M3_GPIO9	CAN0_RX	–	–
M3_GPIO10	UART0_RX	–	–
M3_GPIO11	UART0_RTS	USB1_DRVVBUS	–
M3_GPIO12	I2C0_SDA	–	–

Table 4. Cortex- M3 GPIO Alternate function mapping (continued)

GPIO	ALT A	ALT B	ALT C
M3_GPIO13	I2C0_SCL	–	DEBUGCFG
M3_GPIO14	UART0_TX	–	REMAP0
M3_GPIO15	UART0_CTS	CLKOUT0	REMAP1

2.12 Generic Interfaces

4x UARTS:

- Programmable baud rates up to 3 Mbps;
- Hardware Flow control;
- DMA capable.

3xI2C:

- Master/slave modes in multi-master environment;
- Multiple baud rates supported: 100/400/1000/3400 Kbits/s;
- DMA capable.

3xSSP/SPI ports supporting:

- Motorola SPI-compatible interface;
- Texas Instrument synchronous serial interface;
- National Semiconductor Microwire interface;
- Unidirectional interface;
- DMA capable.

2.13 Watchdog and timers

CortexA7 has:

- 2x MTU timers each providing access to four programmable 32-bit Free-Running decrementing Counters (FRCs);
- 1x Watchdog (WDT) unit that provides a way to recover from software crashes;
- 1x RTC counter clocked with 32KHz Oscillator.

CortexM3 has:

- 1x MTU timers providing access to four programmable 32-bit Free-Running decrementing Counters (FRCs);
- 1x Watchdog (WDT) unit that provides a way to recover from software crashes.

3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

3.1 LFBGA529 (19x19x1.7 mm) package information

Figure 2. LFBGA529 (19x19x1.7 mm) package outline

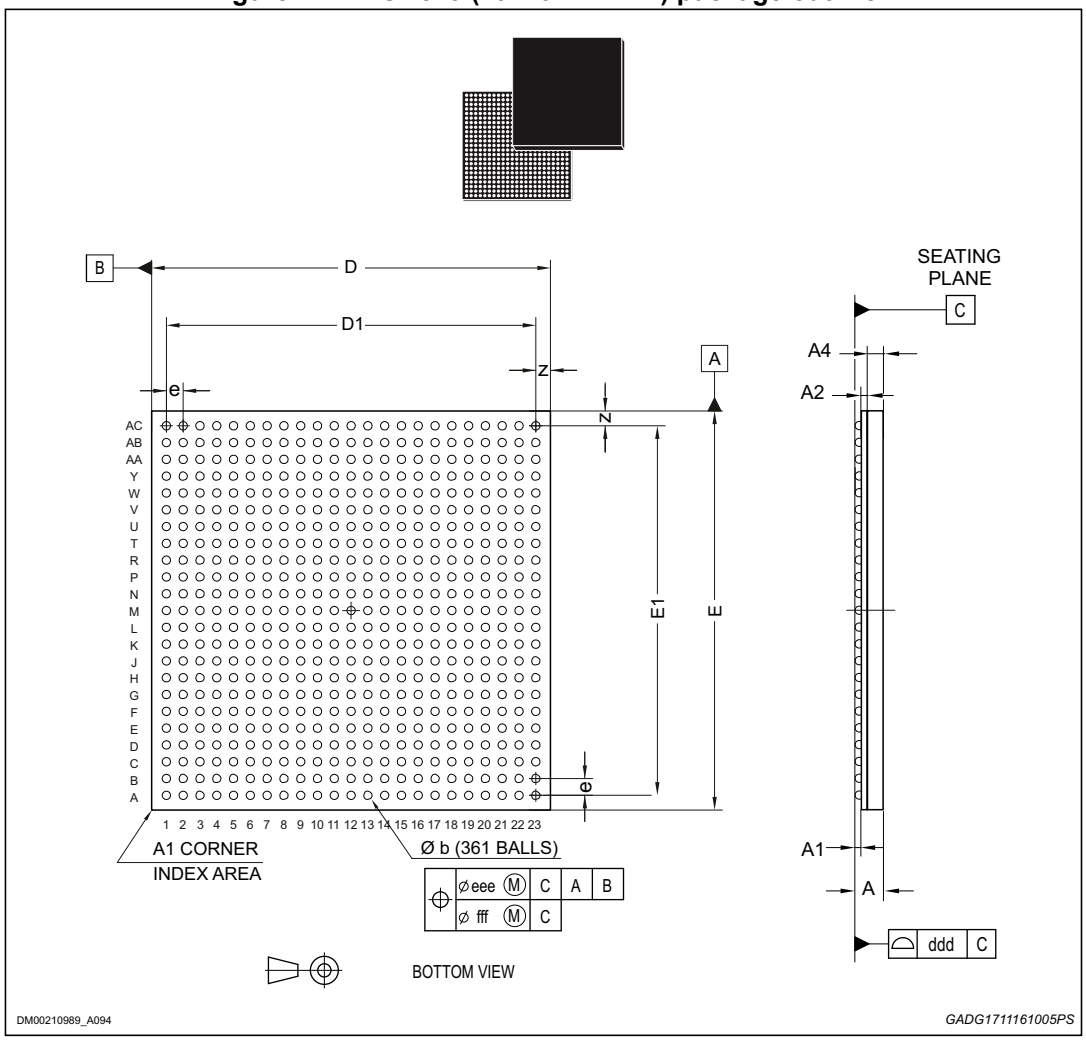


Table 5. LFBGA529 (19x19x1.7 mm) package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	–	–	1.7	–	–	0.0669
A1	0.25	–	–	0.0098	–	–
A2	–	0.28	–	–	0.0110	–
A4	–	–	0.8	–	–	0.0315
b	0.35	0.4	0.48	0.0138	0.0157	0.0189
D	18.85	19	19.15	0.7421	0.7480	0.7539
D1	–	17.6	–	–	0.6929	–
E	18.85	19	19.15	0.7421	0.7480	0.7539
E1	–	17.6	–	–	0.6929	–
e	–	0.8	–	–	0.0315	–
Z	–	0.7	–	–	0.0276	–
ddd	–	–	0.1	–	–	0.0039
eee	–	–	0.15	–	–	0.0059
fff	–	–	0.08	–	–	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

4 Revision history

Table 6. Document revision history

Date	Revision	Changes
19-Dec-2016	1	Initial release.
04-May-2018	2	Updated *Figure 1: Telematics box block diagram on page 5*.