STDES-8CHDOUTPT

Data brief

8-channel digital output L6364 IO-Link hub

Fully assembled board developed for performance evaluation only, not available for sale

Features

- Input DC voltage: 19-32 V_{DC} (IO-Link VBus)
- IO-Link to 8-channel digital output
- Digital output current limit: 0.7 A/ch
- Full isolation protection between IO-Link and digital output
- 4-pin M12 standard IO-Link connector
- 5-pin M12 standard digital output connector

Description

The STDES-8CHDOUTPT reference design embeds the L6364Q the IO-Link device transceiver, the low power STM32G071RBT6 main controller, and the ISO8200AQ isolated device for industrial loads driving.

The STDES-8CHDOUTPT is a turnkey solution ready for industrialization.

The ISO8200AQ lets you drive up to eight industrial loads simultaneously, at a current rating of 0.7 A per channel and an embedded 4 kV isolation.

A dedicated SWD 5-pin connector allows programming the microcontroller.

To communicate with an IO-Link master board, this STDES-8CHDOUTPT reference design requires a PC with an appropriated control GUI software. The IODD file for the STDES-8CHDOUTPT is available.

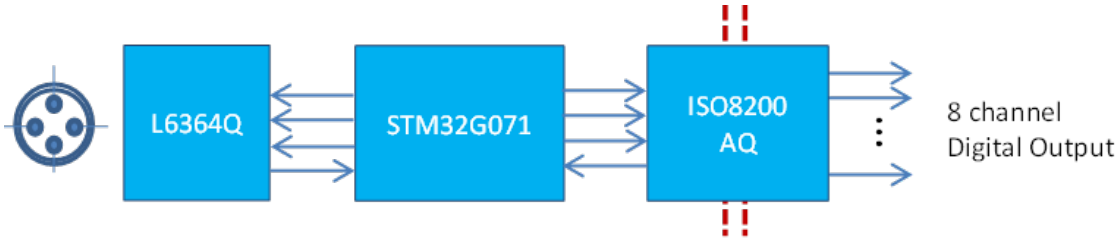
The STDES-8CHDOUTPT is a fully assembled kit developed for performance evaluation only, not available for sale.

Product summary	
8-channel digital output L6364 IO-Link hub	STDES-8CHDOUTPT
Mainstream Arm Cortex-M0+ MCU	STM32G071RBT6
Galvanic isolated octal high side smart power solid state relay with SPI interface	ISO8200AQ
Dual channel transceiver IC for SIO and IO-Link sensor applications in QFN package	L6364Q
1500 W, 23.1 V TVS in SMC	SM15T27AY
Applications	Factory Automation

1 Solution overview

The solution is based on a single STM32G071RBT6 MCU and an L6364Q transceiver. It uses the ISO8200AQ as the high-side load switcher to drive the 24 V high-side output loads.

Figure 1. STDES-8CHDOUTPT functional block diagram



2 Schematic diagrams

Figure 2. **STDES-8CHDOUTPT circuit schematic (1 of 3)**

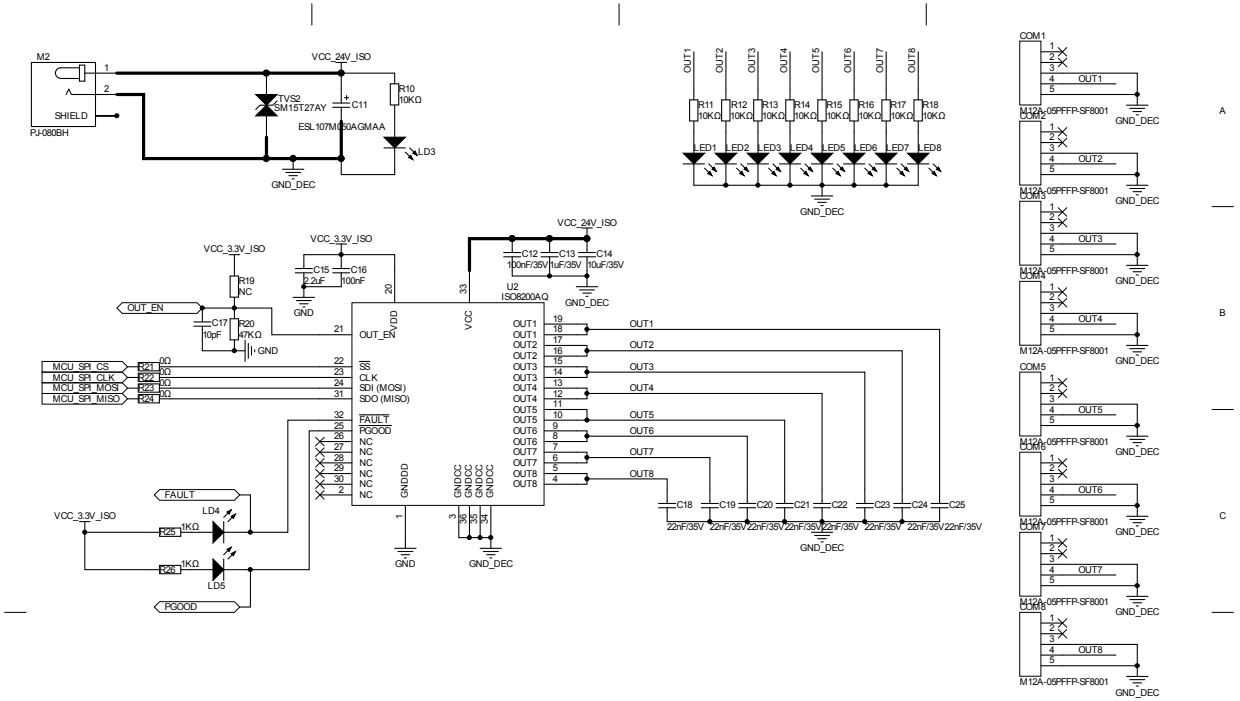


Figure 3. STDES-8CHDOUTPT circuit schematic (2 of 3)

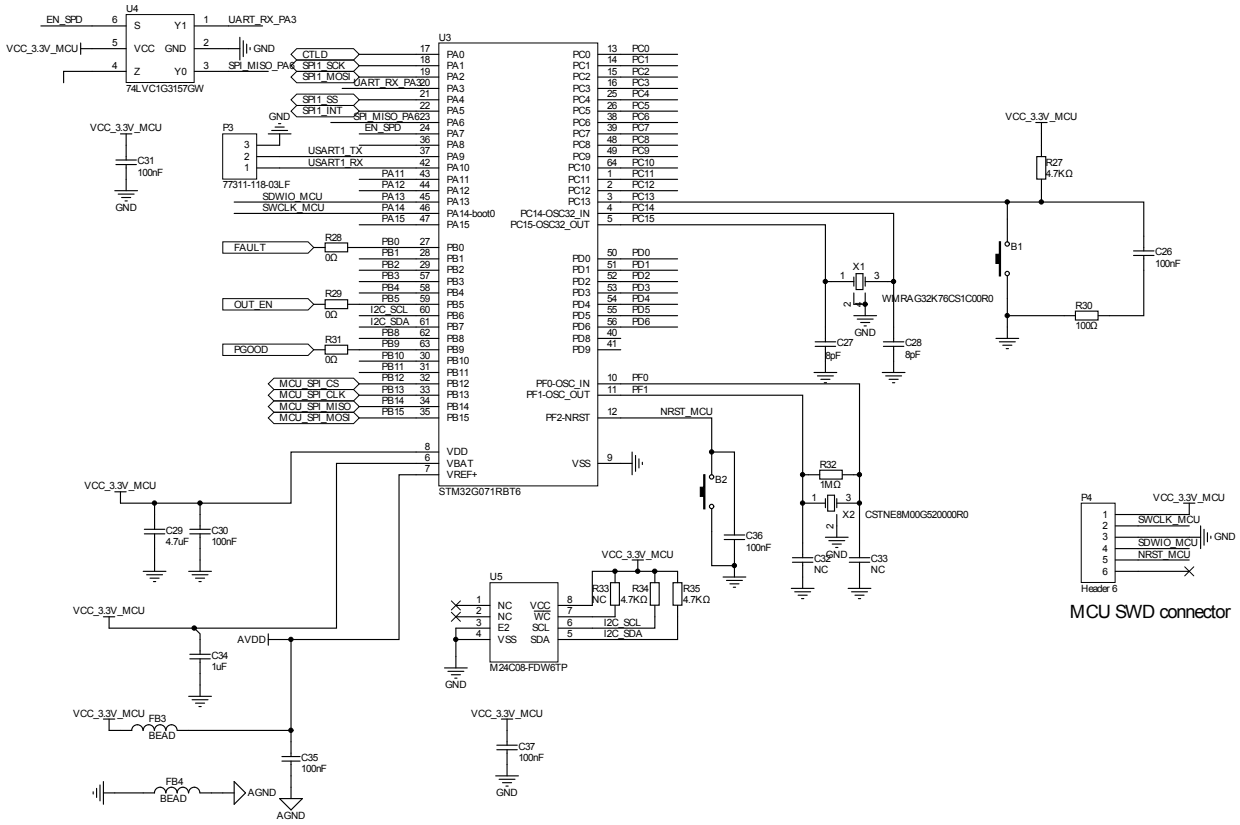
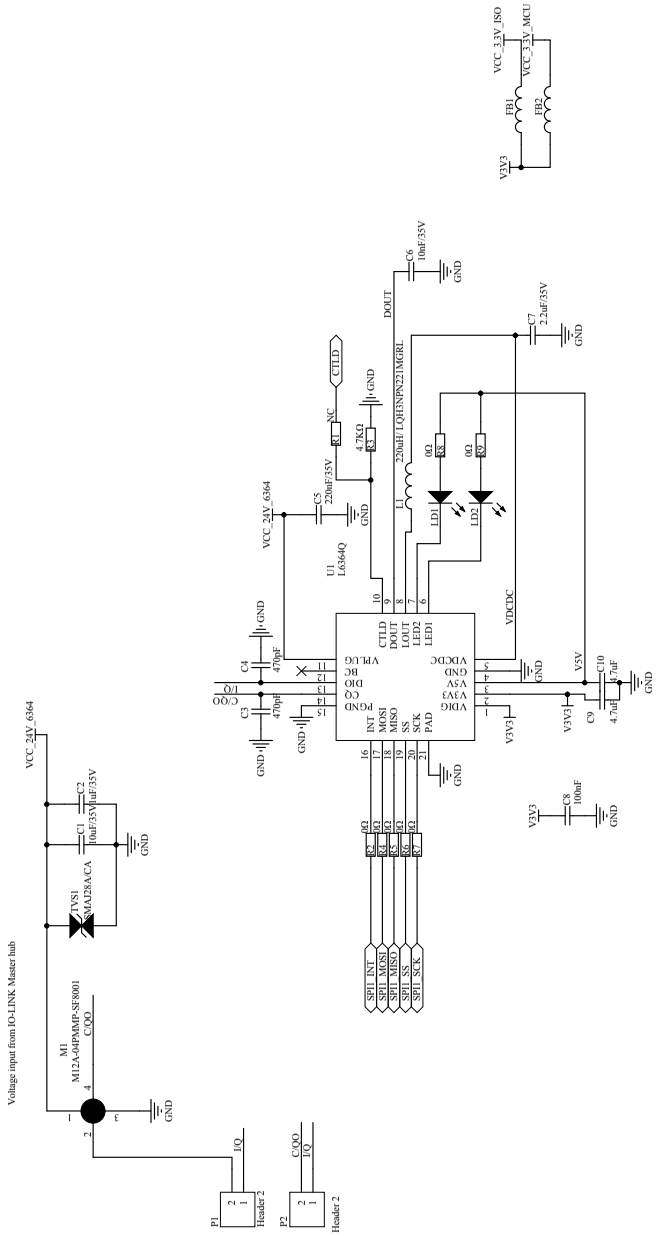


Figure 4. STDES-8CHDOUTPT circuit schematic (3 of 3)



Revision history

Table 1. **Document revision history**

Date	Revision	Changes
11-Oct-2022	1	Initial release.