STDES-8PH7TMG

Data brief

8-port IO-Link master with TMG stack

Fully assembled board developed for performance evaluation only, not available for sale

Product summary	
8-Port IO-Link master with TMG stack	STDES-8PH7TMG
High-performance and DSP with DP-FPU, Arm Cortex-M7 MCU with 2MBytes of Flash memory	STM32H743ZIT6
Low Voltage Unit for Gigabit Ethernet protection	SLVU2.8-4A1
IO-Link communication master transceiver IC	L6360
3 A step-down switching regulator	L7986A
256 Kbit Serial I2C Bus EEPROM	M24256-BRDW6TP
8 channel high side driver	VN808CM-E
Applications	Factory Automation

Features

- Input DC voltage: 24-36 V
- 8 IO-Link master ports
- ESD protected for IO-Link, USB, and power interface
- Connects the IO-Link master board to the PC through a USB interface
- IO-Link device diagnostic and failure alarm function
- STM32H743ZI main controller: high-performance, and DSP with DP-FPU, Arm Cortex-M7 MCU with 1 Mbyte of flash memory, 1MB RAM, 480 MHz CPU, L1 cache, external memory interface, JPEG codec, large set of peripherals
- 8 L6360 IO-Link master transceiver
- DC-DC converter
- On-board reverse polarity protection
- IO-Link master stack with IO-Link version 1.1.3
- SMI-TCP interface for tool communication
- Dual port Ethernet switch
- EEPROM interface for local data storage support
- SWD connector for debugging and programming capability
- Ready for PROFINET and EtherNet/IP gateways
- RoHS compliant

Description

The STDES-8PH7TMG is an 8-port IO-Link master board design. It is based on the STM32H743ZI, which is a high-performance MCU based on the high-performance Arm Cortex®-M0+ 32-bit RISC core and the IO-Link master PHY L6360. The L6360 is an IO-Link communication master transceiver IC.

The VN808CM-E is an octal channel high side driver that can be used to provide the V_{CC} to the L6360 or to the IO-Link device power supply.

The Ethernet IP function is implemented through an external Ethernet PHY KSZ8863, which has two PHY units and supports both 10BASE-T and 100BASE-TX.

A tool called IO-Link device tool V5.1–PE (by an ST partner, TMG) can be used to evaluate the 8-port IO-Link master function.

The Ethernet IP function is already supported as a high-level communication system. Further integrations, like PROFINET, are possible.

This STDES-8PH7TMG is a reference board designed with: the L6360 as IO-Link master transceiver, high performance: the STM32H743ZI as main controller and the L7986A as power supply.

The STDES-8PH7TMG uses the TMG stack and is ready for industrialization.

The use of SLVU2.8-4A1 as voltage suppressors, to protect components, which are connected to data and transmission lines against ESD.

This STDES-8PH7TMG works with an IO-Link device and control tool GUI software with the corresponding IODD file.

The STDES-8PH7TMG can connect with a PC through the Ethernet. It uses an M12 cable to be connected to an IO-Link device. This solution configures an IO-Link device through the TMG GUI software.

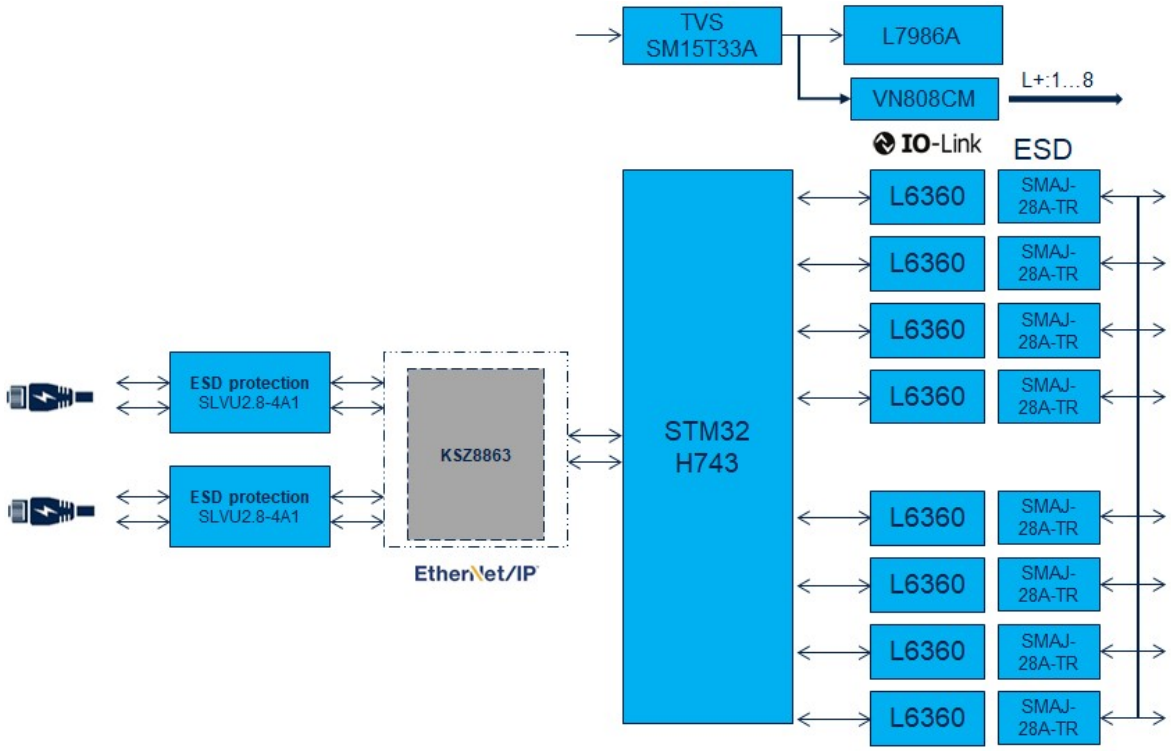
1 Solution overview

The solution is based on a single STM32H743ZI MCU and eight L6360 to implement the 8-port IO-Link master design. The integrated stack is from TMG.

The board can be used together with the IO-Link device tool V5.1 - PE (professional edition). The IO-Link device tool V5.1 is the most popular IO-Link engineering tool on the market. It is open to all IO-Link devices and supports the IO-Link masters from many manufacturers and communication systems. The necessary master device descriptions are available on www.st.com.

PROFINET and Ethernet/IP can be supported as higher-level communication systems. An evaluation license (30 days) is freely available. After the trial period, a license key is needed, which can be bound to a computer or a dongle. The license can be ordered from TMG TE.

Figure 1. STDES-8PH7TMG functional block diagram



2 Schematic diagrams

Figure 2. STDES-8PH7TMG circuit schematic (1 of 10)

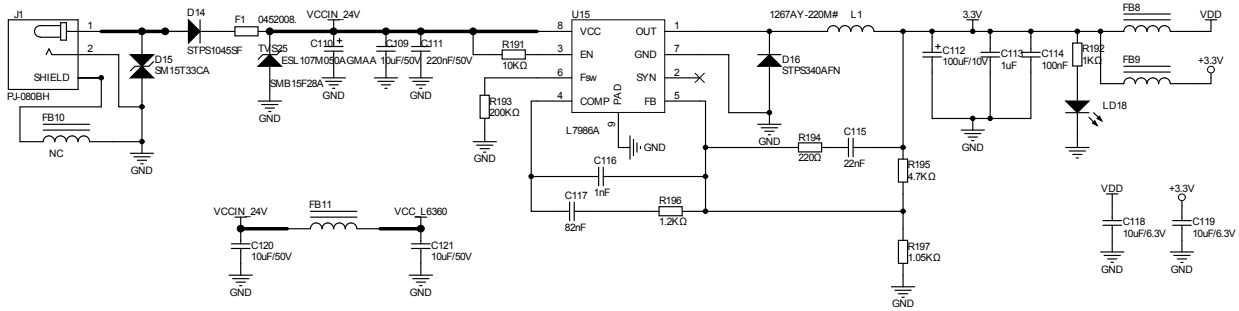


Figure 3. STDES-8PH7TMG circuit schematic (2 of 10)

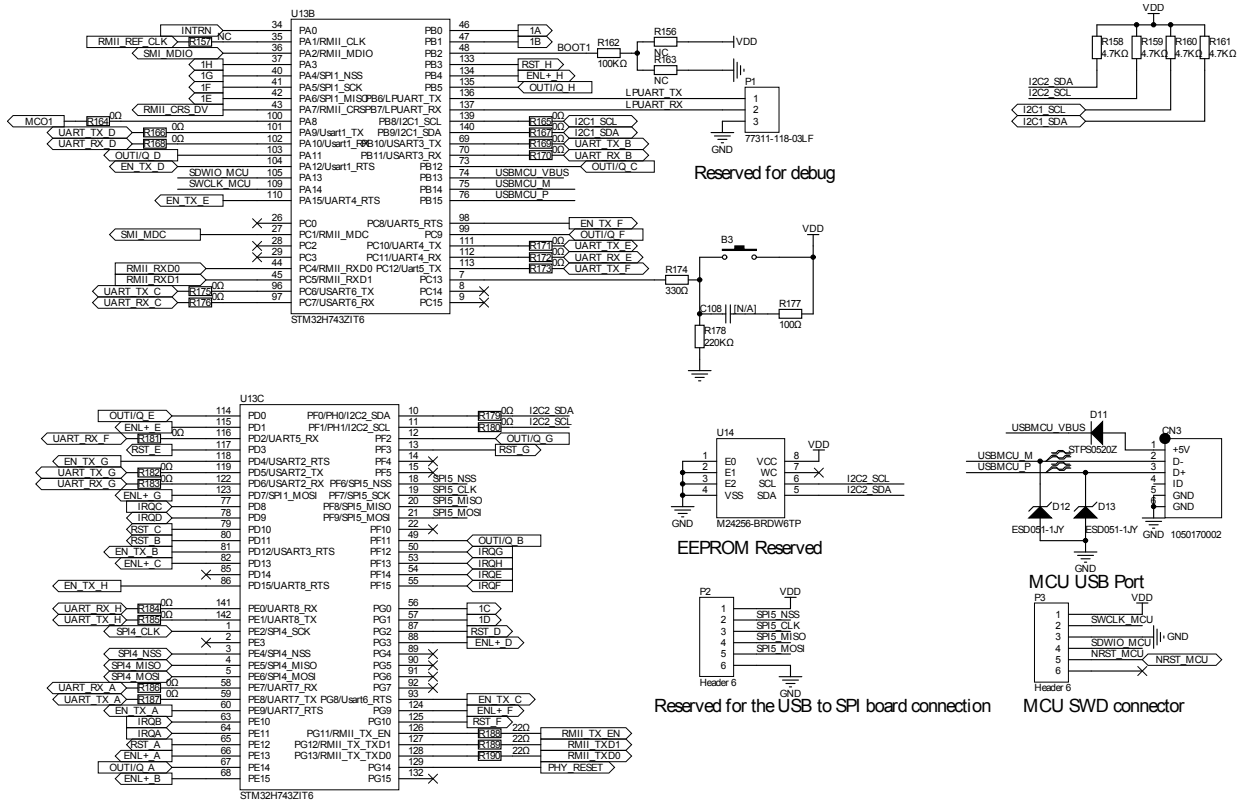


Figure 4. STDES-8PH7TMG circuit schematic (3 of 10)

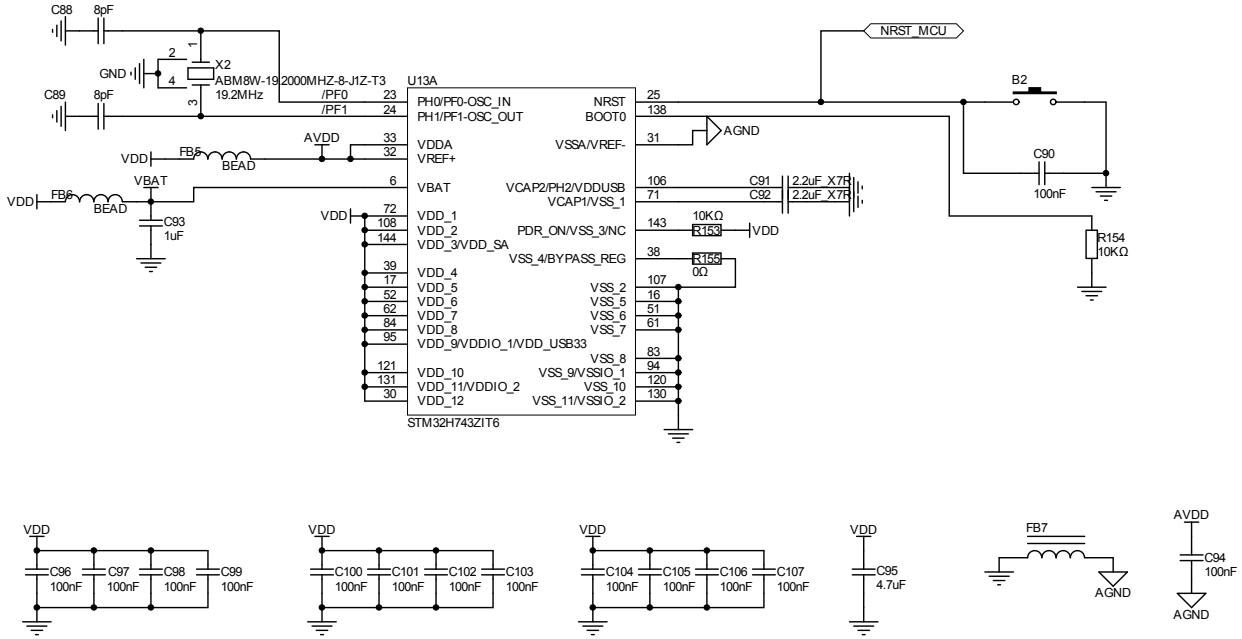


Figure 5. STDES-8PH7TMG circuit schematic (4 of 10)

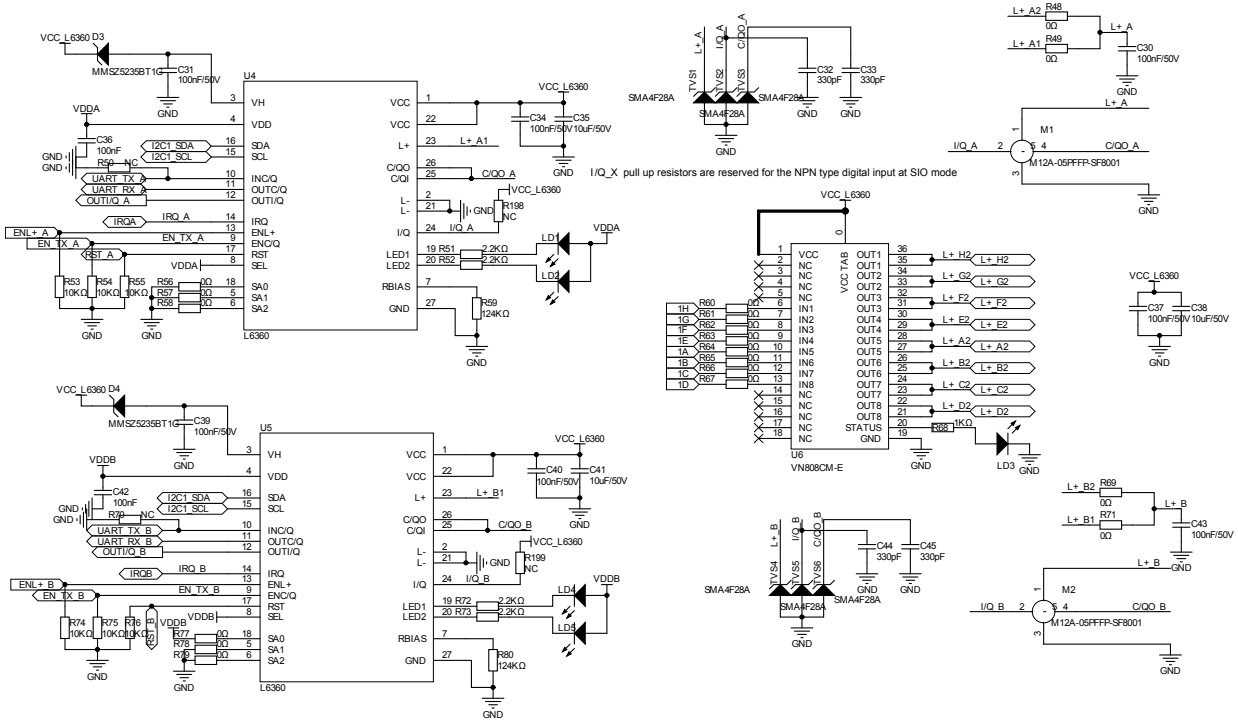


Figure 6. STDES-8PH7TMG circuit schematic (5 of 10)

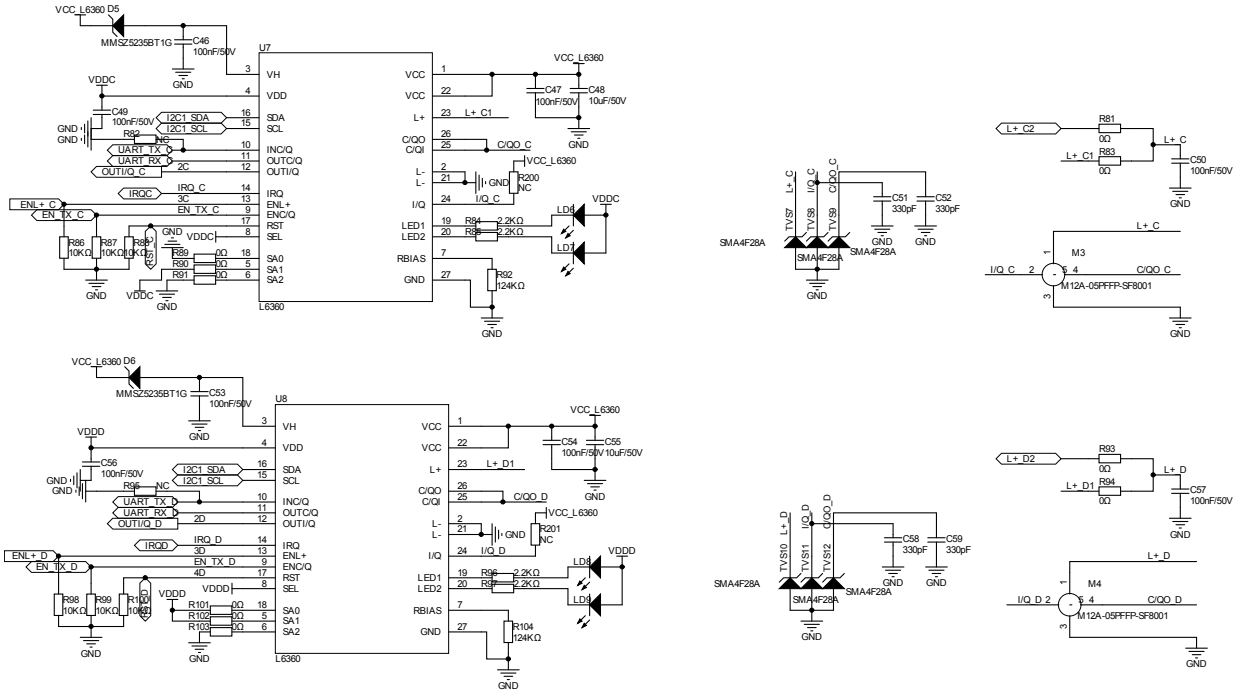


Figure 7. **STDES-8PH7TMG circuit schematic (6 of 10)**

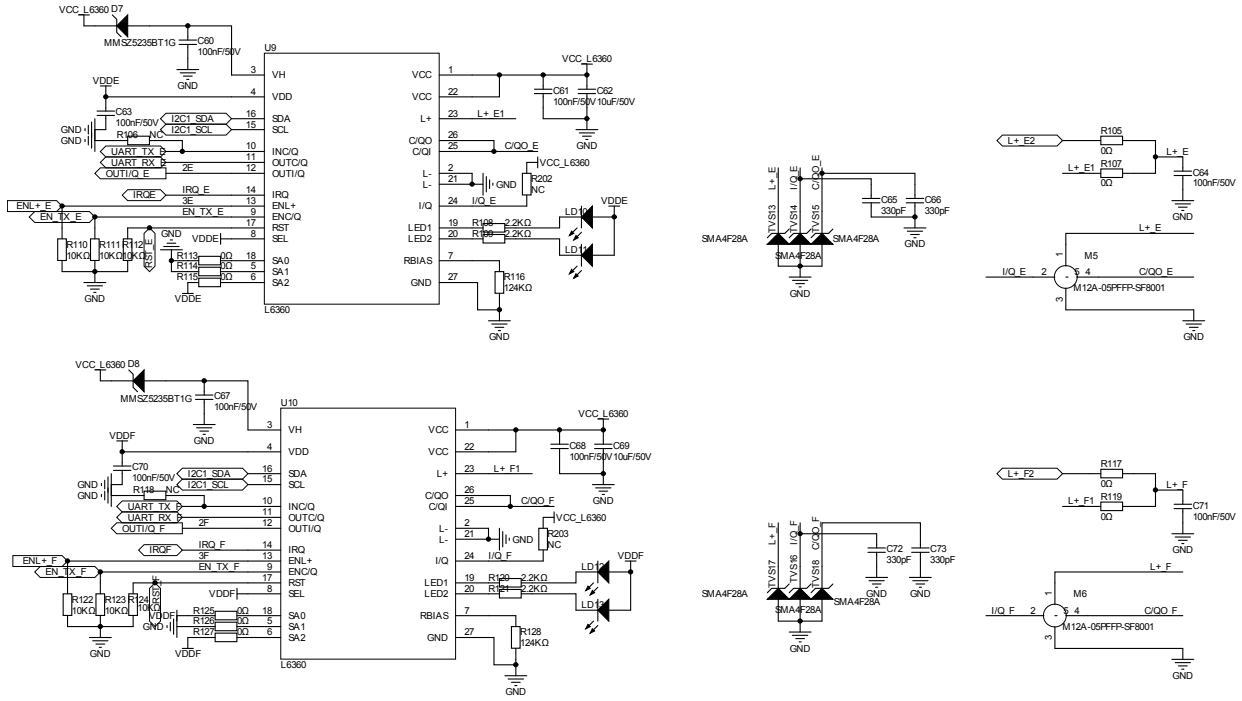


Figure 8. STDES-8PH7TMG circuit schematic (7 of 10)

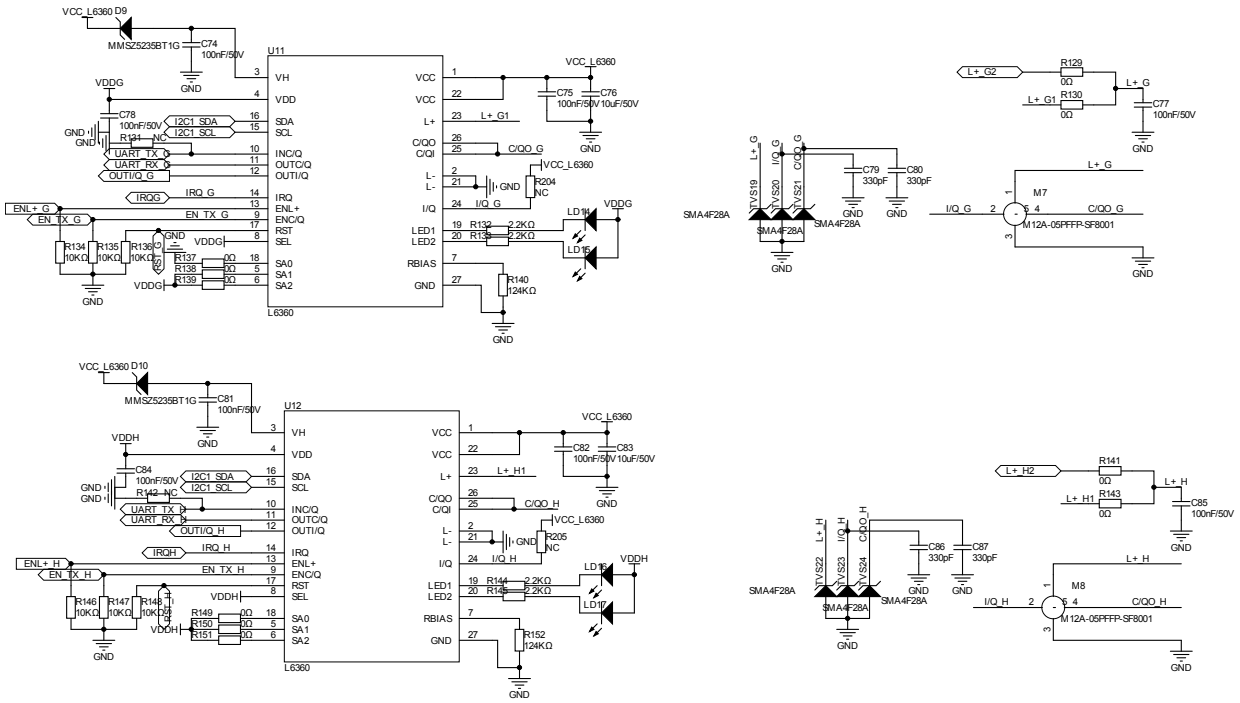


Figure 9. STDES-8PH7TMG circuit schematic (8 of 10)

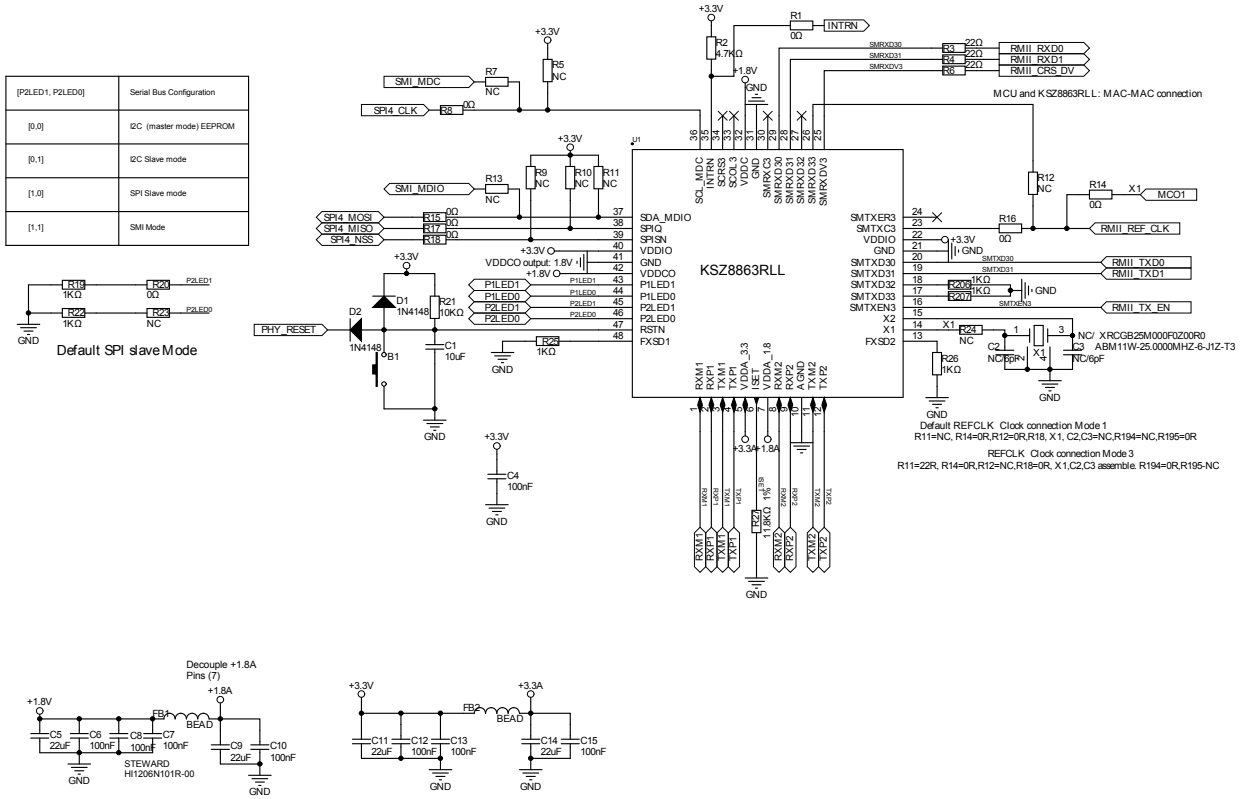


Figure 10. STDES-8PH7TMG circuit schematic (9 of 10)

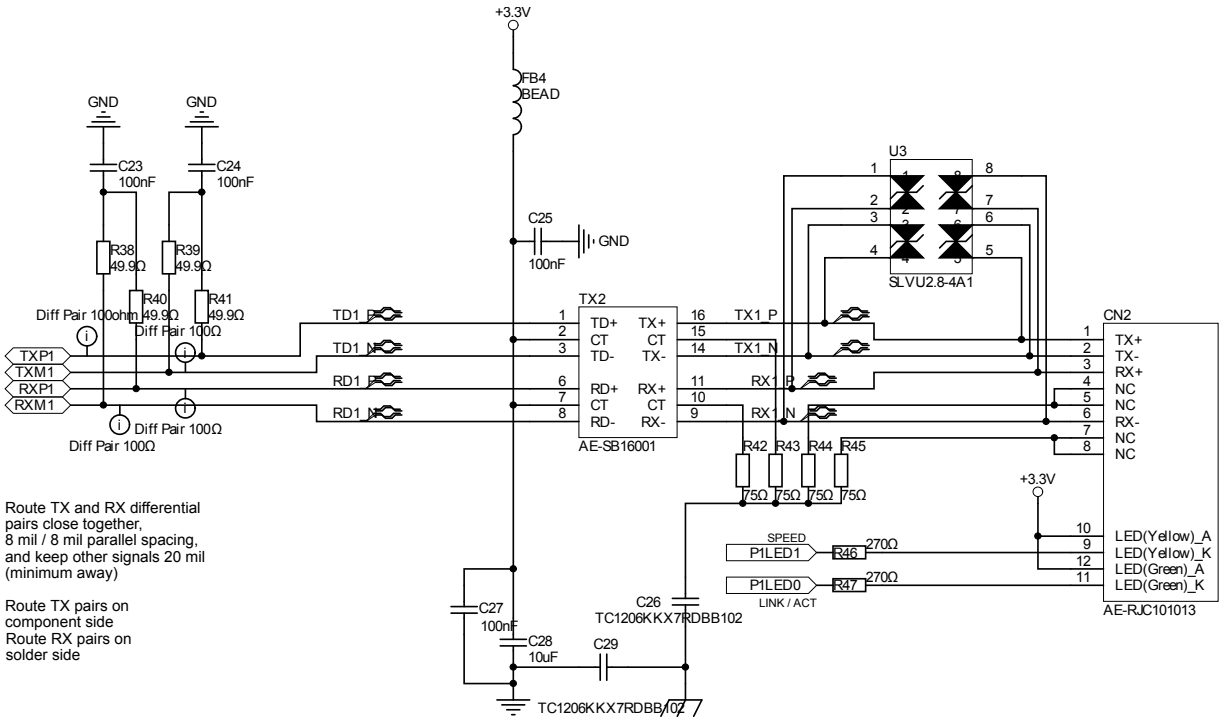
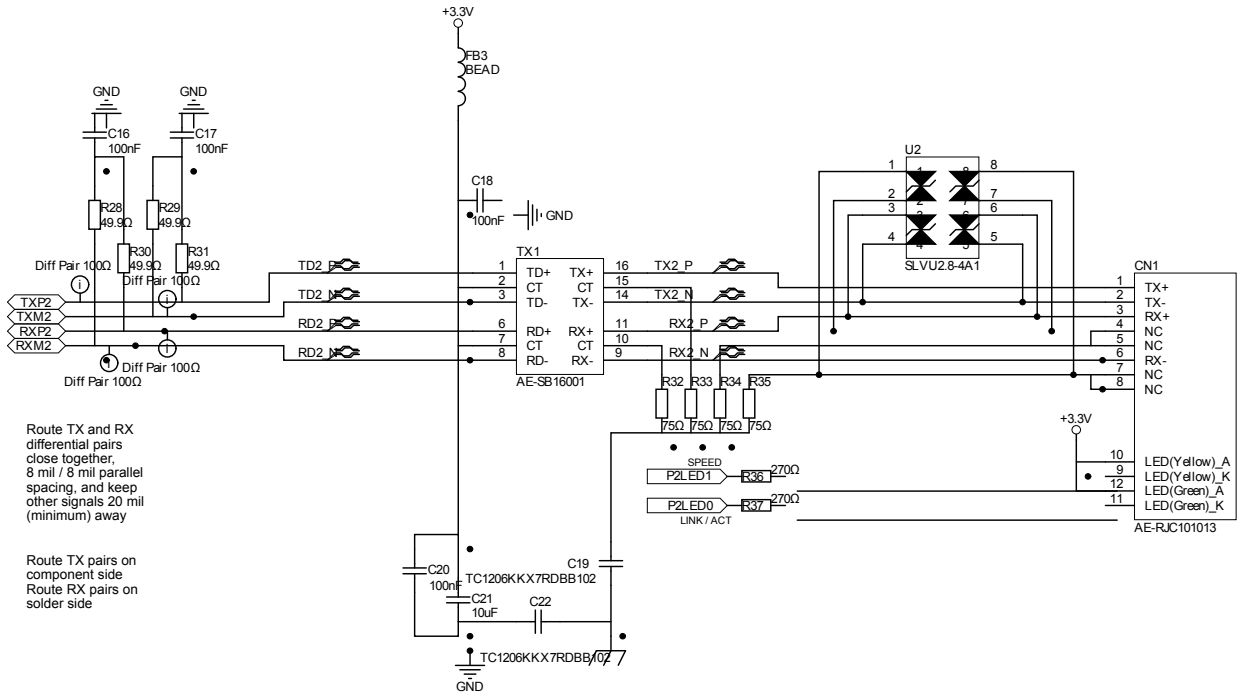


Figure 11. STDES-8PH7TMG circuit schematic (10 of 10)



Revision history

Table 1. **Document revision history**

Date	Revision	Changes
14-Nov-2022	1	Initial release.
18-May-2023	2	Updated Cover image, Product summary, Features, Description, Section 2 Schematic diagrams and Section 1 Solution overview.