STEVAL-TDR004V1

RF power amplifier demonstration board using two SD2933 N-channel enhancement-mode lateral MOSFETs

Features

- Excellent thermal stability
- Frequency: 1.6 - 54 MHz
- Supply voltage: 48 V
- Output power: 400 W (typ.)
- Input power 10 W max.
- Efficiency: 57 % - 76 %
- IMD at 300 WPEP < -26 dBc
- Load mismatch: 3:1 (all phases)

Description

The STEVAL-TDR004V1 demonstration board is an RF broadband power amplifier intended for linear or nonlinear operation over the 1.6 to 54 MHz band, using two SD2933 gold metallized N-channel MOS field-effect transistors. The temperature compensating biasing circuit supports class B and class AB operation.

STEVAL-TDR004V1 is designed in cooperation with Specific RF Devices (Germany).

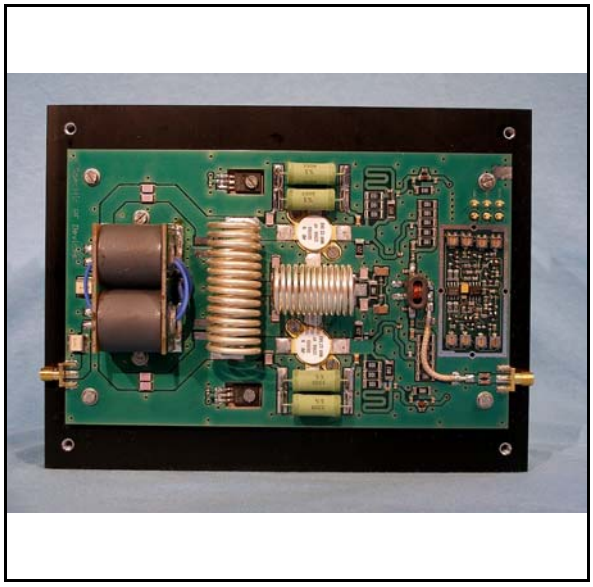


Table 1. Device summary

Order code
STEVAL-TDR004V1

Contents

1 Electrical data

1.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
P_{IN}	Input power	16	W
P_{OUT}	Output power	500	W
V_{DD} (1)	Drain supply voltage	50	V
V_{GG}	Gate biasing voltage	15	V
I_{DD}	Drain current	20	A
P_{DISS}	Power dissipation	400	W

1. V_{GG} from 9 to 15 V and P_{IN} < 16 W

2 Electrical characteristics

T_A = +25 ºC, V_{DD} = 48 V, I_{DQ} = 2 x 900 mA

Table 3. Electrical specification

Symbol	Test conditions	Min.	Typ.	Max.	Unit
Freq	Frequency range	1.6		54	MHz
P_{OUT}	P_{IN} = 10 W	300	400		W
Gain	P_{IN} = 10 W		16.2 ±0.6dB		dB
ND	P_{IN} = 10 W		57 - 76		%
H2	2^{ND} Harmonic @ P_{OUT} = 300 W		-26 / -49		dBc
H3	3^{RD} Harmonic @ P_{OUT} = 300 W		-13 / -58		dBc
VSWR	Load mismatch all phases @ P_{OUT} = 300 W			3:1	

3 Typical performance

Figure 1. Output power and efficiency vs. frequency

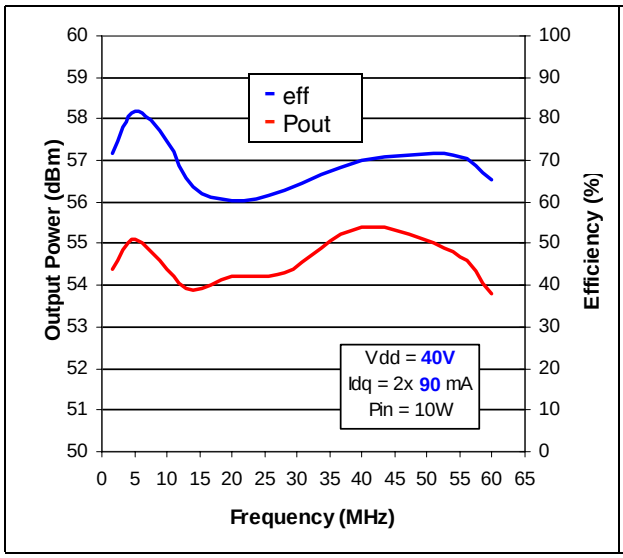


Figure 2. Output power and efficiency vs. frequency

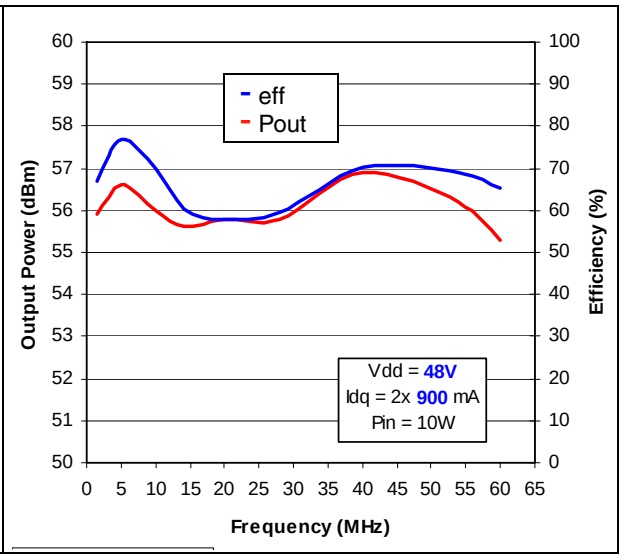


Figure 3. IMD vs. frequency

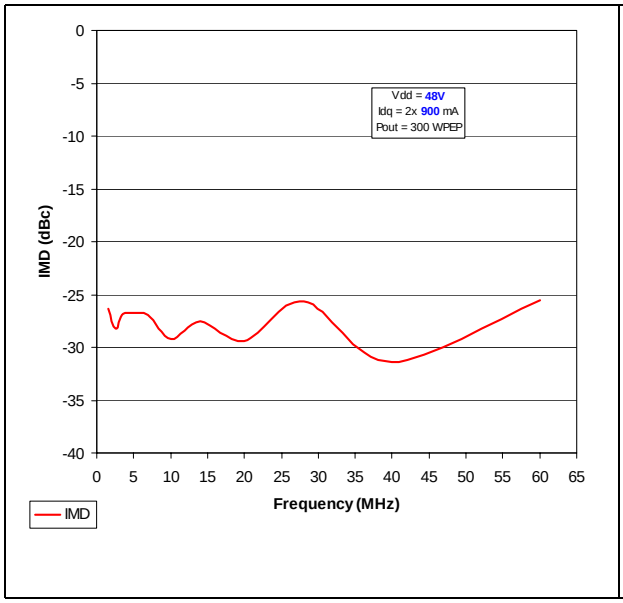


Figure 4. Output power vs. drain voltage

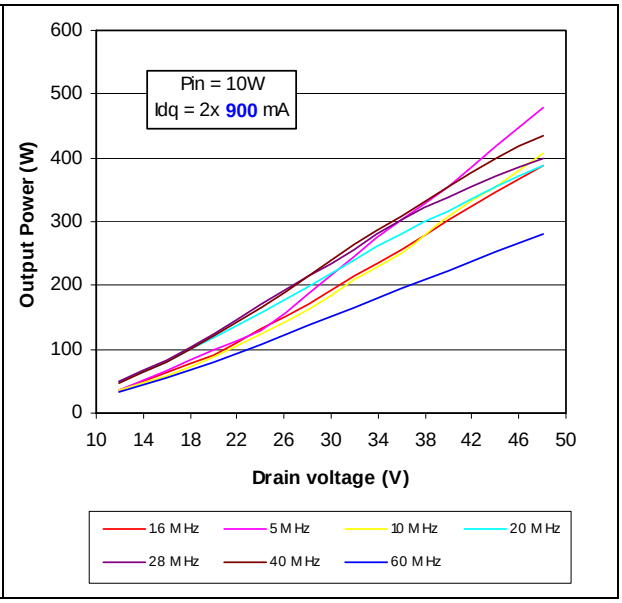
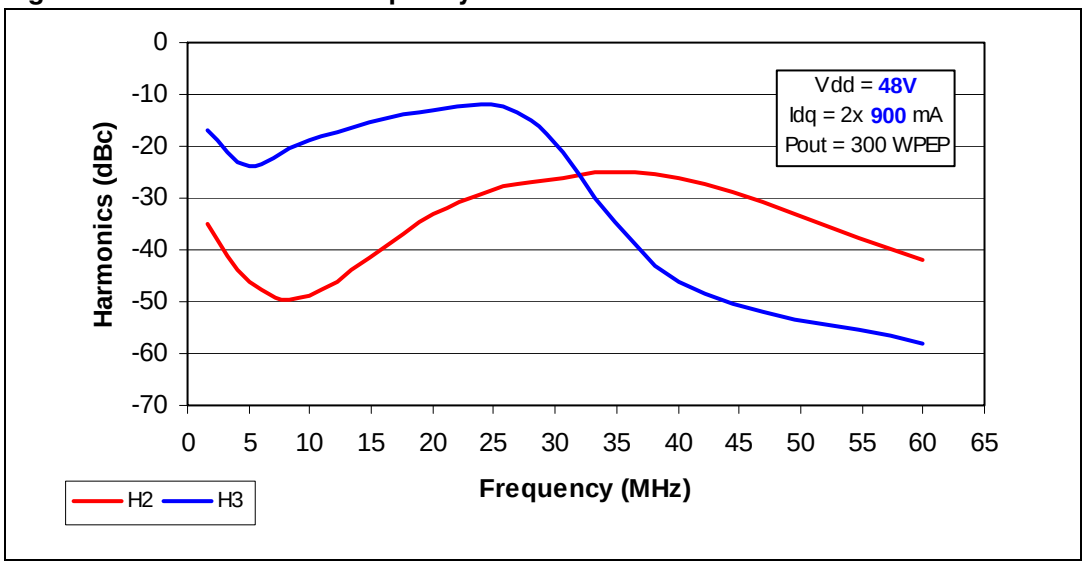


Figure 5. Harmonics vs. frequency



4 STEVAL-TDR004V1 amplifier photos

Figure 6. Top view

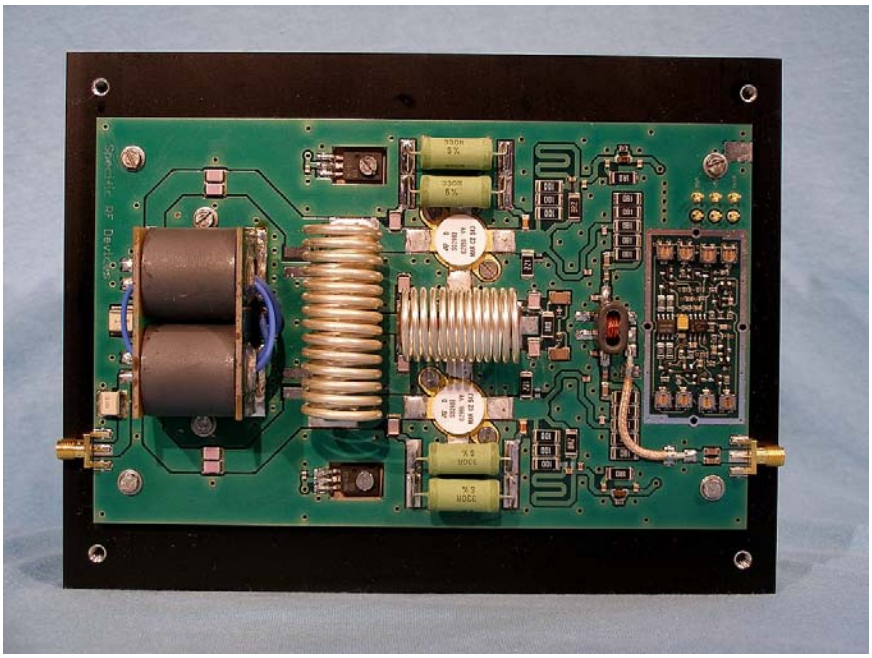
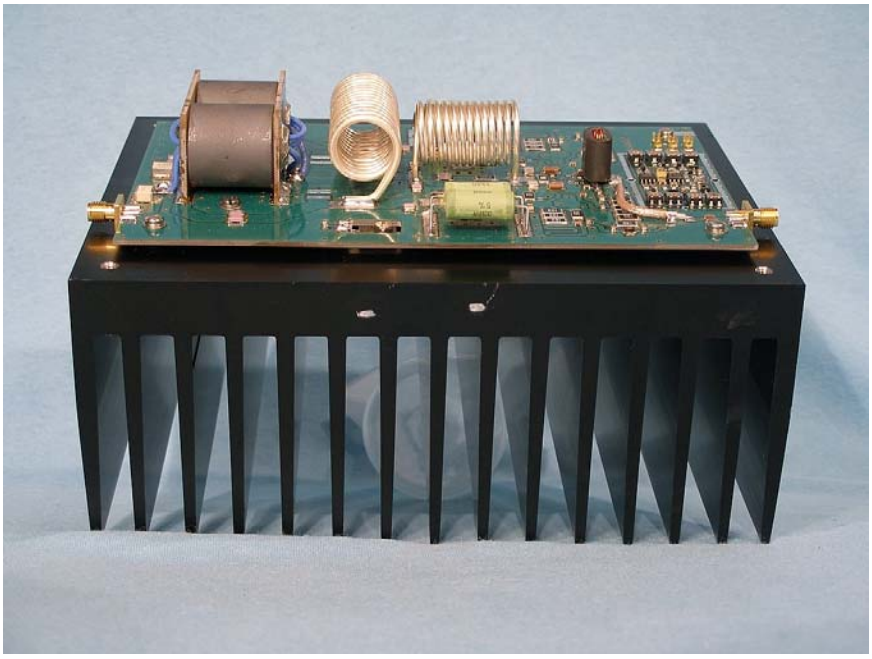


Figure 7. Side view



5 STEVAL-TDR004V1 class of operation

- class B: a low bias point with ~100 mA per transistor
- class AB: a higher bias point with ~ 900 mA per transistor

To select a bias point, the STEVAL-TDR004V1 features a “BIAS” control port.

- The bias point is 2 x 100 mA if “BIAS” is left open. In this case a DC voltage of ~5 V is present
- The bias point is 2 x 900 mA if “BIAS” is connected to ground.

"PA_ON" control port / ON-OFF bias current

- To switch on the biasing circuit, connect “PA_ON” to ground.
- To switch off the biasing circuit, leave “PA_ON” open.

6 SD2933 mounting recommendations

6.1 Mounting recommendations

- Ensure the holes in the heat sinks are free from burrs
- The minimum depth of tapped holes in heat sinks is 6 mm
- Use 4-40 UNC-2A cheese-head screws with a flat washer to more evenly distribute the joint pressure
- The minimum flatness of the mounting area is 0.02 mm
- Mounting area roughness should be less than 0.5 µm (micro)
- Avoid, as much as possible, the use of flux or flux solutions, as they can penetrate even hermetically sealed ceramic-capped transistors. Tin and wash the printed circuit board BEFORE mounting the power transistors, then solder the transistor leads without using flux
- Transistor leads may be tinned by dipping them full-length into a solder bath at a temperature of about 230 °C. No flux should be used during tinning
- Recommended heat sink compounds: WPSII (silicon-free) from Austerlitz Electronics, 340 from Dow Corning, etc.

6.2 Mounting sequence

- Apply a thin layer of evenly distributed heat sink compound to the flange
- Position the device with flat washers in place
- Tighten the screws until finger tight (0.05 Nm)
- Further tighten the screws until the specified torque is reached
- For M174, M177 & M244 package types, torque should be a minimum of 0.6 Nm, and a maximum of 0.75 Nm.

Table 4. DMOS packages - list of materials

Package type	Description	Flange	Leadframe	Ceramic insulator	Plating		Torque (Nm)	
					Leads	Flange	Min	Max
M174	0.500 DIA 4L NON HERM W/FLANGE	Cu	ALLOY 42 (Fe58 / Ni42)	BeO (99.5% min)	Au (100 µ min) over Ni (100 µ min / 350 µ max)	Ni(100 µ min) + Pd (10 µ min)	0.6	0.75
M174 (Moly disk)	0.500 DIA 4L NON HERM W/FLANGE (MOLY DISK)	Cu-Mo-Cu	ALLOY 42 (Fe58 / Ni42)	BeO (99.5% min)	Au (100 µ min) over Ni (100 µ min / 350 µ max)	Ni(100 µ min) + Pd (10 µ min)	0.6	0.75
M177	0.550 DIA 4L NON HERM W/FLANGE	Cu-Mo-Cu	ALLOY 42 (Fe58 / Ni42)	BeO (99.5% min)	Au (60 µ min) over Ni (100 µ min / 350 µ max)	Au (100 µ min) over Ni (100 µ min / 350 µ max)	0.6	0.75
M244	2x 0.400x0.425 WIDE 2L LAP N/H FLANGE	W (85%) - Cu (15%)	ALLOY 42 (Fe58 / Ni42)	BeO(99.5 % min)	Au (60 µ min) over Ni (100 µ min / 350 µ max)	Au (60 µ min) over Ni (100 µ min / 350 µ max)	0.6	0.75

7 Revision history

Table 5. Document revision history

Date	Revision	Changes
27-Aug-2008	1	Initial release.
18-Mar-2010	2	Updated description on cover page.

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