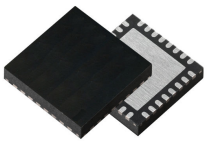
STM32WL3Rxx

Data brief

32-bit MCU Arm® Cortex®-M0+ 2(G)FSK, 4(G)FSK, ASK, D-BPSK, up to 128KB flash, up to 16KB SRAM



VFQFPN32 5x5 mm

Product status	
Reference	**Type**
STM32WL3RK8	32 pins, 64 KB flash
STM32WL3RKB	32 pins, 128 KB flash

Features

- Includes ST state-of-the-art patented technology
- Ultra-low power sub-1GHz wireless system-on-chip
- Programmable MCU:
  - Core: Arm® Cortex®-M0+ 32-bit, running up to 64 MHz
  - Program memory: 64-Kbyte / 128-Kbyte flash memory
  - Data memory: 8-Kbyte / 16-Kbyte SRAM (full retention down to ultra deep stop)
  - Additional storage: 1-Kbyte OTP (user data)
- Radio
  - Frequency bands: 276 - 319 MHz, 413-479 MHz, 826 - 958 MHz
  - Modulation schemes:
    - 2(G)FSK, 2(G)MSK, 4(G)FSK
    - OOK, ASK
    - D-BPSK
    - DSSS (direct sequence spread spectrum)
    - I/Q channels data access
    - Compatible with proprietary and standardized wireless protocols (wM-Bus, Sigfox, Mioty, KNX-RF, IEEE 802.15.4g, others)
  - Air data rate from 0.1 to 600 kbit/s
  - Programmable TX power:
    - 276 - 319 MHz up to 14 dBm
    - 413 - 479 MHz up to 20 dBm
    - 826 - 958 MHz up to 20 dBm
  - RX sensitivity @ 1% BER:
    - -122 dBm @ 1.2 kbits/s 315 MHz 2(G)FSK
    - -132 dBm @ 300 kbit/s 433 MHz OOK
    - -131 dBm @ 300 kbit/s 868 MHz 2(G)FSK
    - -112 dBm @ 38.4 kbit/s 868 MHz 2(G)FSK
  - Suitable for worldwide certifications:
    - Europe: ETSI EN 300 220, category 1 compliant, ETSI EN 303 131
    - US: FCC part 15 and part 90
    - Japan: ARIB STD T67, T108
  - Fully-configurable hardware sequencer for autonomous radio operations (Sniff mode, Frequency hopping, Low Duty Cycle mode, Listen before talk)

- Ultra-low power architecture
  - Dynamic current consumption: 14 µA/MHz
  - Shutdown mode with 6 wakeup pins: 14 nA
  - UltraDeepstop mode: 418 nA (at 25 °C), 1.2 µA (at 85 °C) with RAM0 (16 Kbyte) retained
    - 6 wakeup pins
    - The following functions are not supported in UltraDeepstop mode: MR_SUBGHz, LPUART, RTC, IWDG, DAC
    - No internal wakeup capabilities support in this power mode
  - Deepstop mode: 1.123 µA at (at 25 °C), 4.176 (at 85 °C) with:
    - RAM0 (16 Kbyte)
    - IWDG
    - RTC with LSE
  - SoC consumption: 1.3 mA current in WFI conditions (direct HSE mode)
  - Radio only consumption:
    - 4 mA in RX
    - 8 mA in TX @ +10 dBm
    - 78 mA in TX @ +20 dBm
  - Consumption: 1.3 mA current in WFI conditions (direct HSE mode)
  - Wakeup capability from both Deepstop and Shutdown modes
- Peripherals and analog front-end
  - 12-bit ADC: up to 1 Msample/s with 8 single ended channels (or 4 differentials)
  - Battery voltage monitoring with low-level detection
  - Temperature monitoring
- Communication interfaces
  - Up to 18 GPIOs (VFQFPN32), all with retention capability
  - 1x USART. Supports of LIN, Smartcard Protocol, IrDA, SIR ENDEC specifications, and modem operations (CTS/RTS)
  - 1x LPUART (available also in low-power mode), with wakeup capability
  - 1 x SPI with I2S interface multiplexed
  - 1x I2C (SMBus/PMBus)
  - 1x DMA 8 channels controller, supporting ADC, SPIs, I2Cs, USART, LPUART, timers, AES
- Clock sources and timers
  - Flexible clocking scheme, featuring:
    - 64 MHz (HSI or PLL)
    - Fail-safe 48 MHz crystal oscillator (HSE), with integrated trimming capacitors
    - 32 kHz crystal oscillator (LSE)
    - Integrated low-power 32 kHz RC (LSI)
  - 1x 16-bits, four channels general purpose timer
  - 1x 16-bits, two channels general purpose timer
  - 1x RTC
  - 1x independent watchdog
  - Radio timer with wakeup capability
- Security
  - Secure bootloader with SWD disabling
  - AES-128 co-processor and 16-bit TRNG
  - Embedded UART bootloader with selectable write and read-out protection

- Operating range and reset
  - Ultra-low-power power-on-reset (POR) and power-down-reset (PDR)
  - Programmable voltage detector (PVD)
  - Supply voltage: from 1.7 to 3.6 V
  - Temperature range: -40 ºC to 105 ºC
- All packages are ECOPACK2 compliant

Applications

- Remote control
- Asset tracking
- Wireless sensors
- Industrial monitoring and control
- Smart home and alarm systems
- Building automation

1 Introduction

This document provides the ordering information and mechanical device characteristics of the STM32WL3Rxx microcontrollers, based on Arm® core.

This document must be read in conjunction with the STM32WL3Rxx reference manual (RM0551).

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32WL3Rxx errata sheet (ES0660).

For information on the Arm® Cortex®-M0+ core, refer to the Cortex®-M0+ technical reference manual, available from the www.arm.com website.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

1.1 Glossary

Table 1. **Definition of terms**

Acronym	Description
AES	Advanced encryption standard hardware accelerator
AHB	Advanced high-performance bus
APB	Advanced peripheral bus
BOR	Brown out reset
CHF	Channel filter
CRC	Cyclic redundancy check
DMAMUX	Direct memory access multiplexer
ETSI	European telecommunications standards institute
GFSK	Gaussian frequency shift keying
HSE	High speed external clock oscillator
HSI	High speed Internal clock oscillator
IRQ	Interrupt request
LDO	Low drop output
LPWAN	Low-power wide-area network
LSE	Low-speed external clock oscillator
LSI	Low-speed internal clock oscillator
OTP	One time programmable
PDR	Power down reset
POR	Power on reset
PVD	Programmable voltage detector
PWR	Power controller
SMPS	Switch mode power supply
SPI	Serial peripheral interface (communication standard)
SWD	Single wire debug
SYSCFG	System configuration
TIM	Timer
VREF	Voltage reference
WFI	Wait for instruction (Arm instruction entering low power mode)
IWDG	Watchdog

2 Description

The STM32WL3Rxx is a high performance ultra-low power wireless application processor, intended for RF wireless applications in the sub-1 GHz band. It is designed to operate in both the license-free ISM and SRD frequency bands such as 433, 868, and 915 MHz.

It adopts a single-core architecture embedding an Arm® 32-bit Cortex®-M0+ CPU that can operate up to 64 MHz. It integrates high-speed and flexible memory types: up to 128 Kbyte flash memory, and up to 16 Kbyte RAM, one-time programmable (OTP) memory area of 1 Kbyte.

The STM32WL3Rxx embeds a wide set of peripherals, 12-bit, 8 channel ADC, RTC, IWDG, general purpose timers, AES-128, RNG, CRC, communication interfaces such as USART, SPI, and I2C. Moreover, the security features enable secure boot with USART/SWD block (write protection) and sensitive information storage in flash (read-out protection).

Direct data transfer between memory and peripherals and from memory-to-memory is supported by seven DMA channels with fully-flexible channel mapping by the DMAMUX peripheral.

It can be configured to support standalone or network processor applications. In the first configuration, the STM32WL3Rxx operates as single device in the application for managing both the application code and proprietary sub-1 GHz protocol stacks.

It operates in the -40 to +105 °C temperature range from a 1.7 V to 3.6 V power supply. A comprehensive set of power-saving modes enables the design of low-power applications.

The integrated highly efficient SMPS step-down converter together with the state transition speed between low-power and active states minimize in every condition the average current consumption enabling the STM32WL3Rxx to be the wireless application processor most suited for battery-operated applications.

The STM32WL3Rxx comes in a VFQFPN32 package supporting up to 18 I/Os.

Figure 1. Block diagram

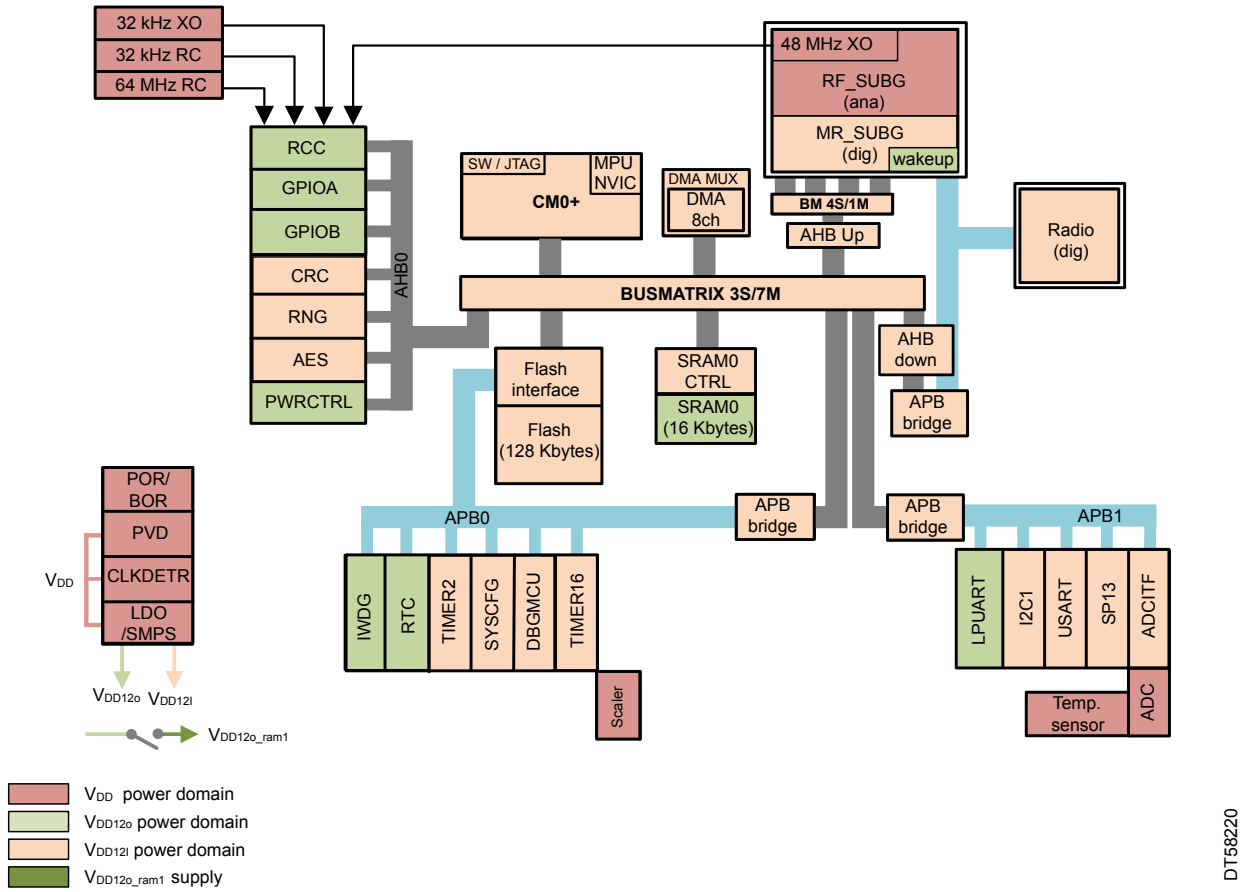


Table 2. Device features and peripheral counts

Feature		STM32WL3RKB	STM32WL3RK8
Memory	Flash memory (Kbytes)	64	128
	SRAM (Kbytes)	16	8
RF front-end	RX	Yes	Yes
	TX	Yes	Yes
ADC	12-bit	1	1
Communication interfaces	CRC	Yes	Yes
	DEBUG	Yes	Yes
	DMA1	Yes	Yes
	GPIOA	Yes	Yes
	GPIOB	Yes	Yes
	I2C1	Yes	Yes
	LPUART1	Yes	Yes
	SPI3 (with I2S multiplexed)	1	1
	USART1	Yes	Yes
System and clock controllers	RCC	Yes	Yes
	RTC	1	1
Timers	TIM2	16-bits, 4 channel general- purpose	
	TIM16	16-bits, 2 channel general- purpose	
Watchdog	IWDG	1	1
Sub-1 GHz RADIO	433 MHz/868 MHz/915 MHz	Y	Y
Security	AES	1	1
	RNG	1	1
Temperature sensor	TEMP SENSOR	Yes	Yes
SMPS		Yes	Yes
Battery voltage monitoring with low-level detection		Yes	Yes
Voltage range		1.7 - 3.6 V	1.7 - 3.6 V
Temperature range		-40 to +85 °C	-40 to +85 °C
CM0+ max speed		64 MHz	64 MHz
Packages	VFQFPN32	Yes	Yes

3 Functional overview

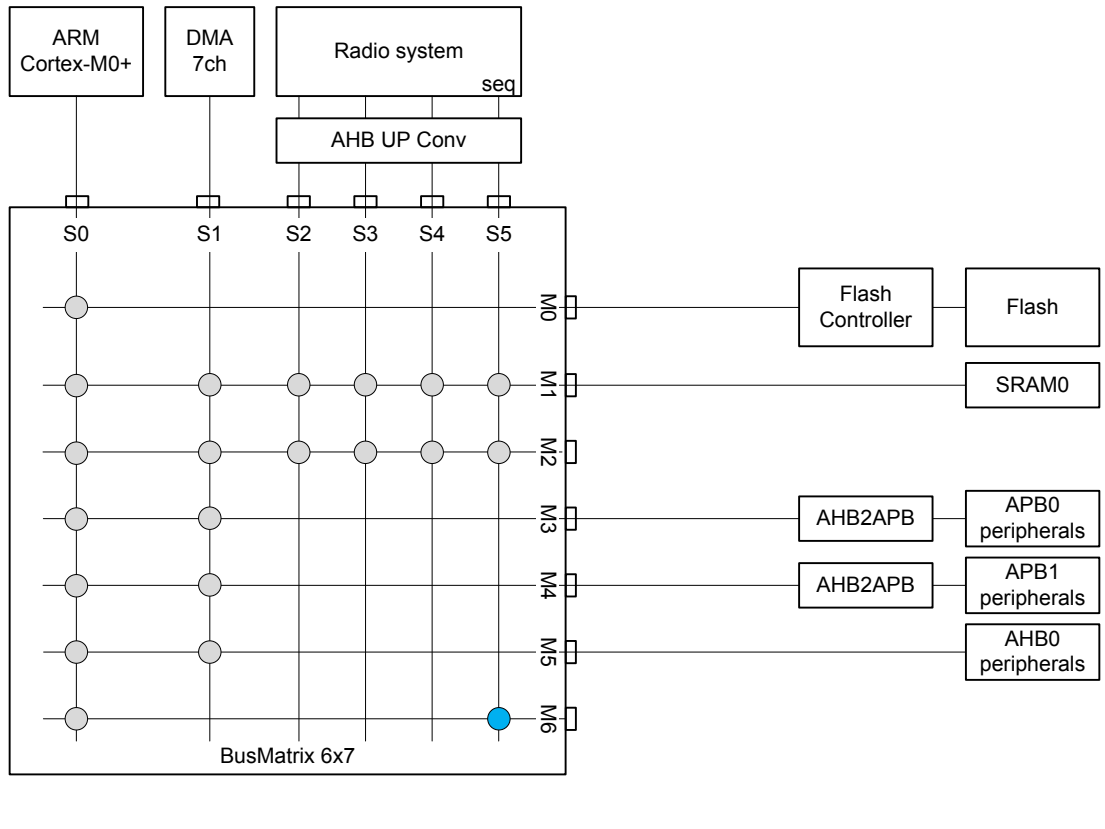
3.1 Architecture

The devices embed a sub-GHz RF subsystem that interfaces with a generic microcontroller subsystem using an Arm Cortex®-M0+ core. The main system consists of a 32-bit multilayer AHB bus-matrix interconnect:

- Three masters:
  - CPU (Cortex -M0+) core S-bus
  - DMA1
  - Sub-1 GHz radio subsystem
- Seven slaves:
  - Internal flash memory on CPU (Cortex®-M0+) S bus
  - Internal SRAM0 (16 Kbytes)
  - APB0 peripherals (through an AHB to APB bridge)
  - APB1 peripherals (through an AHB to APB bridge)
  - AHB0 peripherals
  - AHBRF including AHB to APB bridge and Radio peripherals (connected to APB2)

The bus matrix provides access from a master to a slave, enabling concurrent access and efficient operation even when several high-speed peripherals work simultaneously. This architecture is shown in Figure 2.

Figure 2. STM32WL3Rxx system architecture



The system consists of a Cortex®-M0+ “Radio protocol and application” processor with its radio sub-system. There is a single flash memory to be used by the CPU for both sub-1 GHz protocols and application management. The peripherals are located on the different system buses (AHB, APB0, APB1, APB2 for the radio system). There are 2 SRAM banks, a SRAM0 always power supplied and SRAM1 that can be programmed to be always on or switchable.

3.2 Arm Cortex-M0+ core with MPU

The STM32WL3Rxx contains an Arm Cortex-M0+ microcontroller core. The Cortex-M0+ provides a low-cost platform that meets the needs of CPU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts. The Cortex-M0+ can run from 1 MHz up to 64 MHz. The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier. The interrupts are handled by the Cortex-M0+ nested vector interrupt controller (NVIC). The NVIC controls specific Cortex-M0+ interrupts as well as the STM32WL3Rxx peripheral interrupts. With its embedded Arm core, the STM32WL3Rxx family is compatible with all Arm tools and software.

3.3 Memories

3.3.1 Embedded flash memory

The flash controller implements the erase and program flash memory operation. The flash controller also implements the read and write protection.

The flash memory features are:

- Memory organization:
  - 1 bank of 128 Kbytes
  - Page size: 2 Kbytes
- 32-bit wide data read/write
- Page erase (2 Kbytes) and mass erase

Flash controller features:

- flash memory read operations
- flash memory write operations: single data write, or 4x32-bits burst write
- flash memory erase operations
- page write protection mechanism (by 4 segments of variable sizes from 1 to 127 pages)

Option-byte loader hardware mechanism reserved for ST analog trimming bits.

3.3.2 Embedded SRAM

The STM32WL3Rxx integrates a total of 16 Kbytes of embedded SRAM.

3.3.3 Embedded OTP

The one-time-programmable (OTP) is a memory of 1 Kbyte dedicated for user data. The user can protect the OTP data area by writing the last word at address 0x1000 1BFC and by performing a system reset. This operation freezes the OTP memory from further unwanted write operations.

3.3.4 Memory protection unit (MPU)

The MPU is used to manage accesses to memory to prevent one task from accidentally corrupting the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas. The MPU is especially helpful for applications where critical or certified code must be protected against the behavior of other tasks.

3.4 RF subsystem

The STM32WL3Rxx embeds an ultra-low-power radio supporting Sub-1GHz operation.

It integrates a high performance ultra-low power Sub-1GHz transceiver supporting different modulation schemes: 2(G)FSK, 4(G)FSK, OOK and ASK and air data rate programmable from 0.1 to 300 kbit/s for 2-GFSK and up to 600 kbit/s for 4-GFSK.

The STM32WL3Rxx RF output power can be programmed to deliver up to +20 dBm, in TX+TXHP mode, enabling long communication ranges. Up to +16 dBm in TXHP mode or up to +10 dBm in TX modes, exploiting the extremely optimized architecture for ultra-low-current consumption and battery-operated system.

The STM32WL3Rxx receiver offers best in class sensitivity performance together with extremely low current consumption.

3.4.1 RF front-end

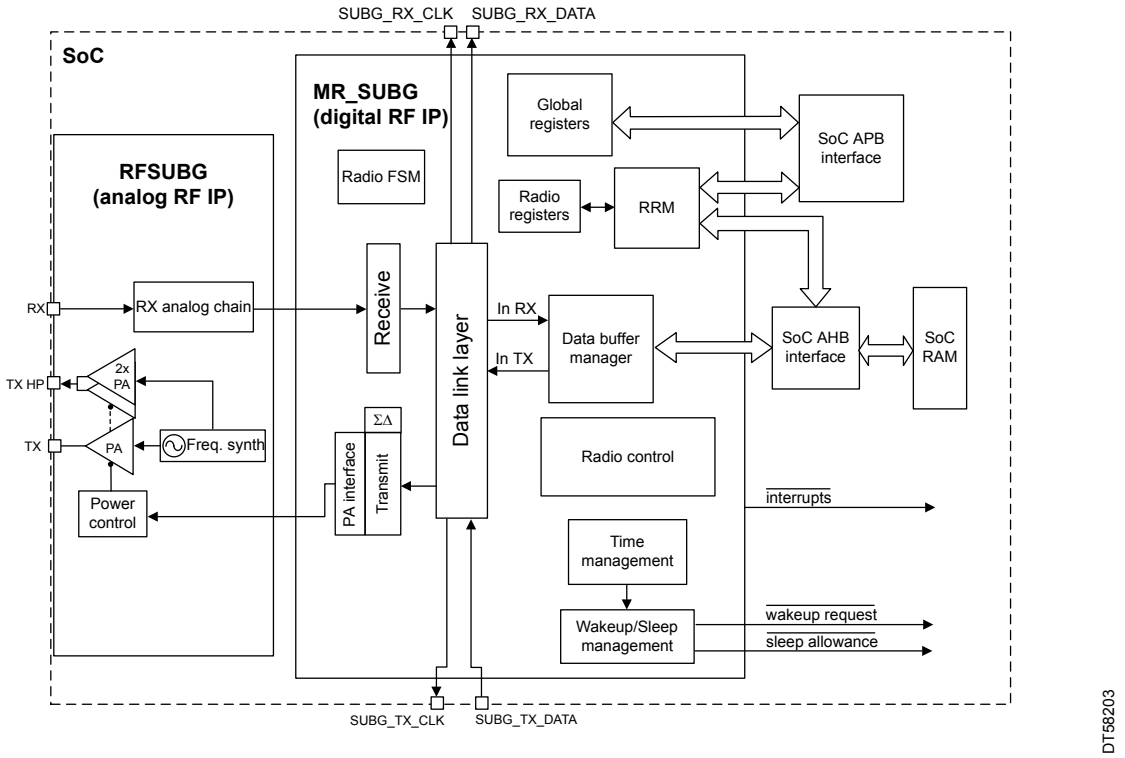
The RF front-end is based on a direct modulation of the carrier in TX and used a low IF architecture in RX mode.

In transmit mode, three different topologies, with dedicated BOM configuration on the board, address operations in different output power range according to the selection of TX and TX_HP.

Moreover, the output power is user selectable through the dedicated programmable register. A linearized, smoothed analog control offers a clean power ramp-up.

In receive mode, the automatic gain control (AGC) can reduce the chain gain at both RF and IF locations, for optimized interferer rejections. Thanks to the use of complex filtering and highly accurate I/Q architecture, high sensitivity and excellent linearity can be achieved.

Figure 3. Sub-1GHz IP block diagram



3.4.2 TX and RX event alert

The STM32WL3Rxx is provided with the TX_SEQUENCE and RX_SEQUENCE signals which alert, respectively, transmission and reception activities.

A signal can be enabled for TX and RX on two pins, through alternate functions:

- TX_SEQUENCE is available on PA10 (AF2) or PB14 (AF2)
- RX_SEQUENCE is available on PA8 (AF2) or PA11 (AF2)

The signal is high when radio is in TX (or RX), low otherwise.

The signals can be used to control external antenna switching and support coexistence with other wireless technologies.

Note: The RF_ACTIVITY signal is used to notify if there is an ongoing RF operation (either TX or RX). It is a logical OR between the RX_SEQUENCE and TX_SEQUENCE.

3.5 Power supply management

3.5.1 SMPS step-down converter

The device integrates a step-down converter to improve low power performance when the V_{DD} (also referred to as V_{DDIO}) voltage is high enough.

The SMPS output voltage can be programmed from 1.2 V to 2.4 V with a granularity of 100 mV. The SMPS output voltage can be controlled by the PWRC_CR5.SMPSLVL[3:0] register.

The relation between the SMPSLVL and the V_{out} of the SMPS is given by Table 3:

Table 3. SMPS output voltage

SMPSLV	V_{out}	Min. V_{DD}
0	1.2 V	1.95 V
1	1.2 V	1.95 V
2	1.2 V	1.95 V
3	1.3 V	1.95 V
4	1.4 V	2.0 V
5	1.5 V	2.0 V
6	1.6 V	2.15 V
7	1.7 V	2.2 V
8	1.8 V	2.3 V
9	1.9 V	2.45 V
10	2.0 V	2.6 V
11	2.1 V	2.7 V
12	2.2 V	2.8 V
13	2.3 V	2.8 V
14	2.4 V	2.9 V
15	2.4 V	2.9 V

It is internally clocked at 4 MHz or 8 MHz. It can be clocked at a frequency in-between 4 MHz and 8 MHz by means of the KRM feature. In this case the SMPS can be clocked at system clock divided by 8 to 16 by unitary steps. This feature is useful to avoid that the channel to be received is at a frequency that is an integer multiple of the SMPS clock.

The device can operate without the internal SMPS either by using a dedicated hardware setting, or by using the bypass-on-the-fly (BOF) feature. The bypass-on-the-fly permits internal connection of the SMPS output to the battery via a current-limited switch (Static mode), or bypass of the SMPS by the use of an internal regulator (dynamic). In both modes the SMPS is off while the bypass-on-the-fly is operating, and a programmable current limitation is provided. The Static mode connects the SMPS output to the battery after the first start-up of the STM32WL3Rxx, and the connection is maintained until a reset occurs. In this case, the transmission is limited to +14 dBm. The dynamic mode bypasses the SMPS with a regulator. For instance, this can be done dynamically to use the SMPS during transmission and to bypass the SMPS via a regulator during reception.

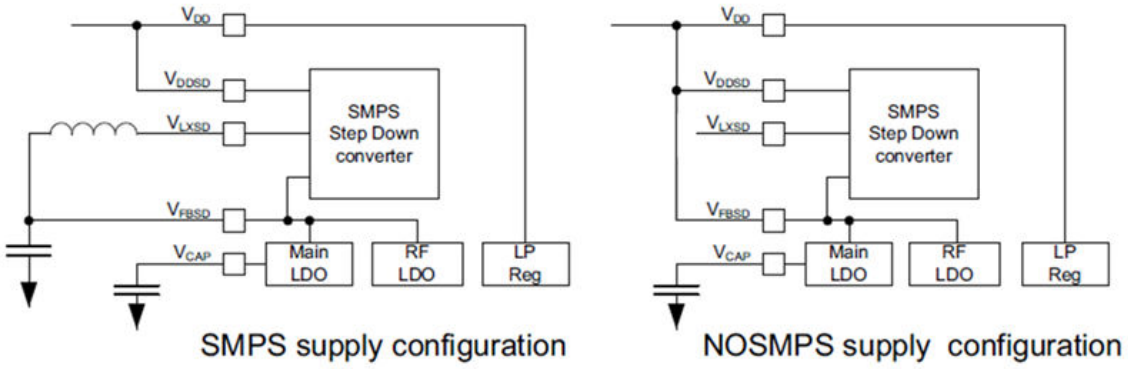
The SMPS has the following possible configurations:

- SMPS_ON
  - The VFBSD pin of the SMPS outputs a regulated voltage (from 1.2 V to 2.4 V)
  - The SMPS needs a clock.
- No SMPS
  - VFBSD pin must be connected or to an external supply or to VDD
  - VLXSD pin must be floating
  - The SMPS does not need a clock

- STATIC BYPASS ON THE FLY
  - The VFBSD pin is internally connected to VDDSD via a switch, with a maximum current of 40 mA
  - The SMPS does not need a clock and is disabled
- DYNAMIC BYPASS ON THE FLY
  - The VFBSD pin internally connected to the output of a programmable voltage regulator, with a maximum current of 40 mA.
  - The SMPS doesn't need a clock and is disabled

Except for the configuration SMPS OFF, an L/C BOM must be present on the board and connected to the VFBSD pad.

Figure 4. Power supply configuration



3.5.2 SMPS bypass on-the-fly (BOF)

Bypass on-the-fly (BOF) is a feature that allows the SMPS to be bypassed. This can be done directly with a power switch (static bypass mode), or via an LDO (dynamic bypass mode).

In case extra radio sensitivity is needed, the user can switch to dynamic bypass mode before entering radio receiver mode. In this way the SPSM is OFF. When BOF is done in static bypass mode, the SMPS is disabled and the SMPS output is connected to the battery via an internal switch. In this case both Deepstop and Run mode operations can be chosen.

When BOF is done in dynamic bypass mode, the SMPS is disabled and the LDO is enabled. The LDO is connected between the battery and the VFBSD pin and its output voltage is programmable like the SMPS.

A current limitation is implemented in both static and dynamic bypass modes.

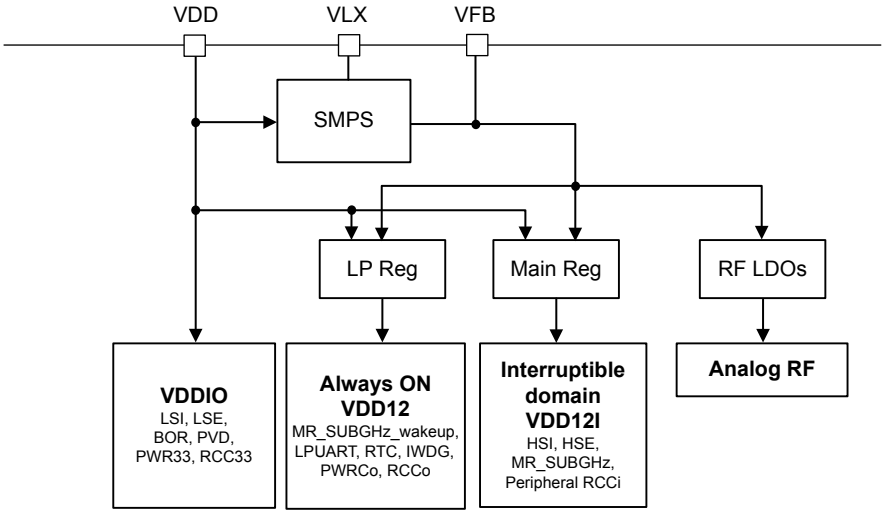
3.5.3 Linear voltage regulators

The digital power supplies are provided by different regulators:

- Main LDO (MLDO):
  - Provides 1.2 V from a 1.4 to 3.6 V input voltage
  - Supplies both VDD12i and VDD12o when the device is active
  - Is disabled during the low power mode (Deepstop)
- Low-power LDO (LPREG):
  - Stays enabled during both active and low power phases
  - Provides 1.0 V or 1.2 V voltage selectable by software
  - Not connected to the digital domain when the device is active
  - Connected to the VDD12o domain during low power mode (Deepstop)
- Dedicated LDO (RFLDO) to provide a 1.2 V to the analog RF block

The embedded SMPS step-down converter is inserted between the external power and the LDOs.

Figure 5. Power-supply domains overview



3.5.4 Power voltage supervisor

The STM32WL3Rxx device embeds several power voltage monitoring:

- Power On reset (POR) / Power Down reset (PDR) / Brown-Out reset (BOR)
- BORH monitoring
- Power voltage detector (PVD)

3.6 Operating modes

The STM32WL3Rxx supports three main operating modes:

- Run mode
- Deepstop mode
- UltraDeepstop mode
- Shutdown mode

The transition from one mode to another one is managed through a PMU state machine.

3.6.1 Run mode

In Run mode, the STM32WL3Rxx is fully operational.

In Run mode:

- both regulators (MLDO and LPREG) are enabled
- the MLDO provides the power supply for both VDD12i and VDD12o
- the system clock and the bus clock are running
- the CPU core and the radio can be used
- the power consumption may be reduced by gating the clock of the unused peripherals

3.6.2 Deepstop mode

Deepstop is an STM32WL3Rxx power mode that allows restart from a saved context environment, and the application to resume running at wake up.

The conditions to enter Deepstop mode are:

- The radio (MR_SUBG) is sleeping (no radio activity)
- The CPU is sleeping (WFI with SLEEPDEEP bit activated)
- No unmasked wake-up sources are active (including those from a previous wakeup sequence for which the software did not clear the associated flag after wakeup) the PWRC_CR1.LPMS bit is equal to 0.
- The system is clocked on RC64MPLL (HSI or PLL locked mode)
- Reset PWRC_CR5.GPIORET bit when PWRC_DBGR.DEEPSTOP2 bit is set, otherwise set PWRC_CR5.GPIORET bit
- If SMPS clock variable rate multiplier is enabled RCC_KRMR.KRMEN=1, in order to guarantee a good SMPS startup at next wakeup, its mandatory to put RCC_CFGR.SMPSDIV=0.

In Deepstop mode:

- The system and the bus clocks are stopped as the RC64MPLL block is OFF
- the VDD12i power domain is switched off
- the VDDI2o power domain is ON and supplied by the LPREG which regulated voltage is:
  - 1.2 V if the bit PWRC_CR2.LPREG_FORCE_VH=1
  - 1.0 V in all the other cases

The current regulation status of the LPREG is reported by the PWRC_CR2.LPREG_VH_STATUS bit:

- the RAM0 bank is kept in retention
- the other RAM banks are in retention or not, depending on software choice in PWRC_CR2 register
- the slow clock can be running or stopped, depending on the software configuration present before Deepstop entry:
  - ON or OFF
  - LSE or LSI source
- The RTC, IWDG, and LPUART stay active (if enabled and one slow clock source is ON).
- The MR_SUBG wakeup block including its timer stay active (if enabled and one slow clock source is ON).
- The configurations of all the I/Os are latched before entering Deepstop mode:
  - AF configuration is latched only for the I/Os on which at least one pin of a peripheral that can be active in Deepstop mode (RTC, IWDG, and LPUART) is mapped
  - I/O analog switch configurations are retained for the I/Os on which at least one analog pin of a peripheral that can be active in Deepstop mode is mapped
  - All the I/Os that can be outputs driving either a static low or high level, and also some IOs with the slow clock information, LCO, or RTC_OUT.

A version of the Deepstop mode called DEEPSTOP2 has been implemented to emulate the Deepstop mode without losing the debugger connection and breakpoints nor watchpoints.

- This variant can be selected by setting the PWRC_DBGR.DEEPSTOP2 bit.
- In this case, the Deepstop mode sequence (entry and exit) is done without shutting down the VDD12i power domain.

Possible wake-up sources are:

- The radio block is able to generate two events to wake up the system through its embedded wake-up timer running on low speed clock:
  - SUBG RFIP wakeup time is reached

- the RTC is able to generate a wakeup event
- the LPUART is able to generate a wakeup event
- the IWDG is able to generate a reset event
- all I/Os are able to wake up the system.

At wakeup, the hardware resources located in the VDD12i power domain are reset, the CPU reboots. The reason for wakeup is visible in a PWRC register.

3.6.3 UltraDeepstop mode

UltraDeepStop mode is the least power consuming mode, with the ability to retain crucial information in RAM.

The entry conditions for UltraDeepStop mode are the same as those needed to enter Shutdown mode, except that the PWRC_PDCRA.UDS bit must be equal to 1 (the PWRC_DBGR.DEEPSTOP2 bit must be kept at 0).

In UltraDeepStop mode:

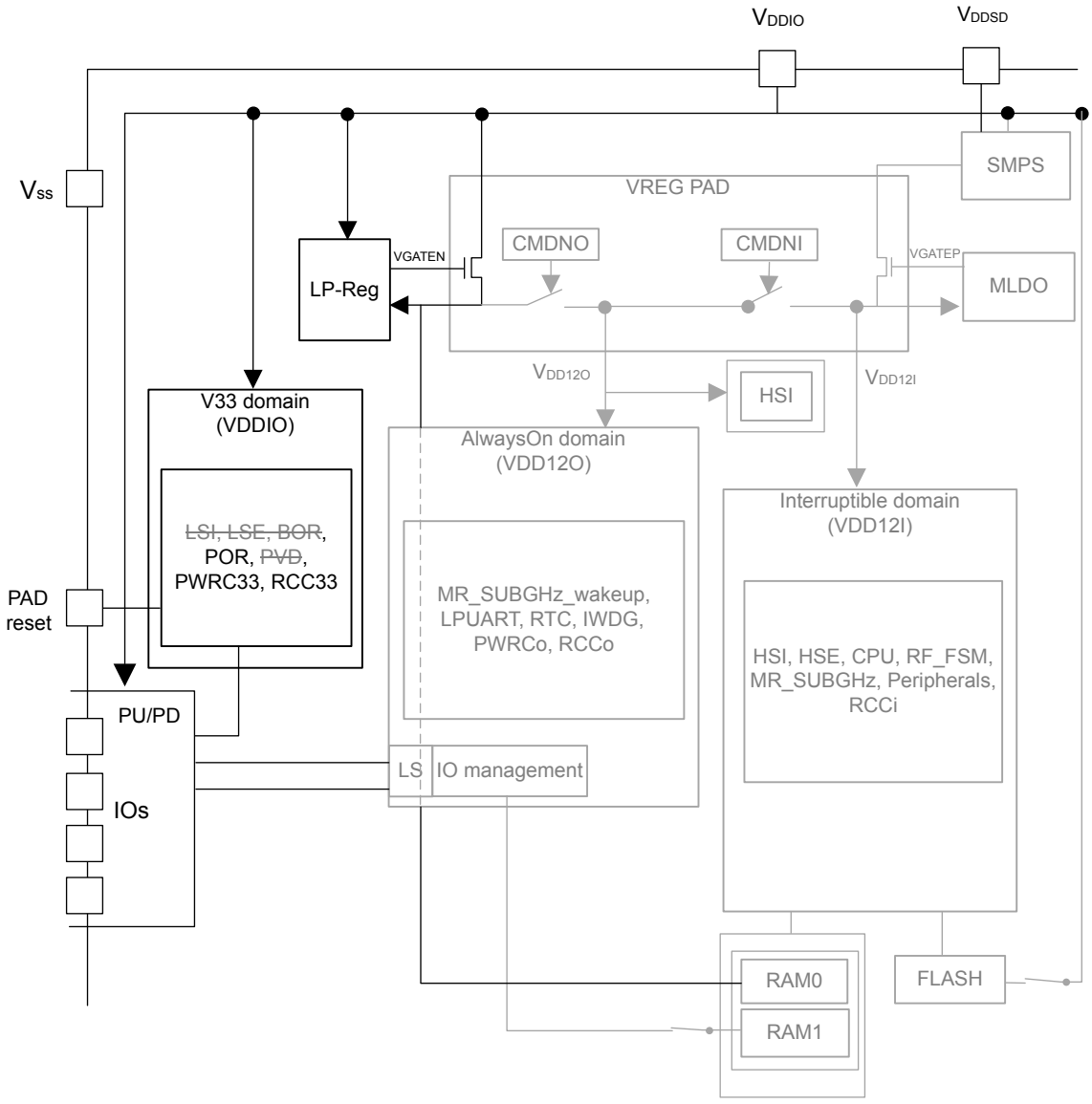
- The system is powered down as SMPS regulator is OFF (both VDD12i and VDD12o power domains are OFF)
- The LP regulator is left ON with a drive capability of 1.0 V only
- The VDDIO power domain is ON
- All clocks are OFF (system and slow clock tree) as RC64MPLL, LSI and LSE are OFF
- If PWRC_CR1.APC = 1, the I/O pull-ups and pull-downs are controlled by PWRC_PUCRx/PWRC_PDCRx during UltraDeepStop mode
- The only wakeup sources are a low pulse on the RSTN pin, or a configurable pulse or level on the PB0/PA0/PA7/PA8/PA9/PA11 pins through the Shutdown I/O wakeup enable register (PWRC_SDWN_WUEN), and the Shutdown I/O wakeup polarity register (PWRC_SDWN_WUPOL)

An UltraDeepStop exit is similar to a board POR startup, but the RAM0 content is kept throughout the low power period. The associated reset reason is the PORRSTF flag or EWUF flag (see V33 reset status register (RCC_CSR) for reset reason flag details, or Shutdown I/O wakeup flag register (PWRC_SDWN_WUF) for the PB0/PA0/PA7/PA8/PA9/PA11 wakeup flag).

The BOR feature can be enabled or disabled during UltraDeepStop through the PWRC_CR1.ENSDNBOR bit.

Figure 6 shows the regulators and SMPS configuration in UltraDeepStop mode, configured with the BOR reset disabled.

Figure 6. Power regulator and SMPS configuration in UltraDeepstop mode



3.6.4 Shutdown mode

The Shutdown mode is the least power consuming mode. The conditions to enter Shutdown mode are the same conditions needed to enter Deepstop mode except that the PWRC_CR1.LPMS bit must be equal to 1. (PWRC_DBGR.DEEPSTOP2 bit must be maintained equal to 0).

In Shutdown mode, the STM32WL3Rxx is in ultra-low power consumption: all voltage regulators, clocks and the RF interface are not powered. The STM32WL3Rxx can enter shutdown mode by internal software sequence. There are two ways to exit shutdown mode: by asserting and de-asserting the RSTN pin or by six GPIOs. The wake-up function is associated to PB0, PA0, PA7, PA8, PA9, and PA11.

In Shutdown mode:

- The system is powered down as both the regulators are OFF
- The V_{DDIO} power domain is ON
- All the clocks are OFF, LSI and LSE are OFF
- The I/O pull-ups and pull-downs can be controlled during Shutdown mode, depending on the software configuration
- The wake-up sources below are available through a low pulse on the RSTN pin or six GPIOs.
  - The 6 Wakeup GPIOs can be enabled by a single bit that enables all the wake-up GPIOs at the same time (PWRC_SDWN_WUPOL.WUEN).
  - The 6 Wakeup GPIOs share the same flag register PWRC_SDWN_WUF.WUF.
  - All Wakeup GPIOs (but PB0) not support Schmitt trigger feature.
  - The polarity control of wake-up pins shares the same polarity setting bit, PWRC_SDWN_WUF.WUPOL.

The exit from Shutdown is like a POR start up. The BOR feature can be enabled or disabled during Shutdown.

3.7 Reset management

The STM32WL3Rxx offers two resets:

- PORESETn: this reset is provided by the APMU analog power management unit block and corresponds to a POR or BOR root cause. It is linked to power voltage ramp-up or ramp-down. This reset impacts all resources of the STM32WL3Rxx device.
  Exit from Shutdown mode is equivalent to a POR/BOR and thus generates a PORESETn.
- The PADRESETn (system reset): this reset is built through several sources:
  - PORESETn
  - Reset due to the watchdog The STM32WL3Rxx embeds a watchdog timer, which may be used to recover from software crashes.
  - Reset due to CPU lockup. The Cortex-M0+ generates a lockup to indicate the core is in the lock-up state resulting from an unrecoverable exception. The lock-up reset is masked if a debugger is connected to the Cortex-M0+.
  - Software system reset. The system reset request is generated by the debug circuitry of the Cortex-M0+. The debugger sets the SYSRESETREQ bit of the application interrupt and reset control register (AIRCR). This system reset request through the AIRCR can also be done by the embedded software (into the hardfault handler for instance).
  - Reset from the NRSTn external pin The NRSTn pin toggles to inform that a reset has occurred.

The PADRESETn resets all resources of the STM32WL3Rxx, except:

- debug features
- flash controller key management
- RTC timer
- power controller unit
- part of the RCC registers

The pulse generator guarantees a minimum reset pulse duration of 20 µs for each internal reset source. In case of reset from the RSTN external pad, the reset pulse is generated when the pad is asserted low.

3.8 Clock management

Three different clock sources may be used to drive the system clock (CLK_SYS) of the STM32WL3Rxx (see Figure 7. Fast clock tree generation):

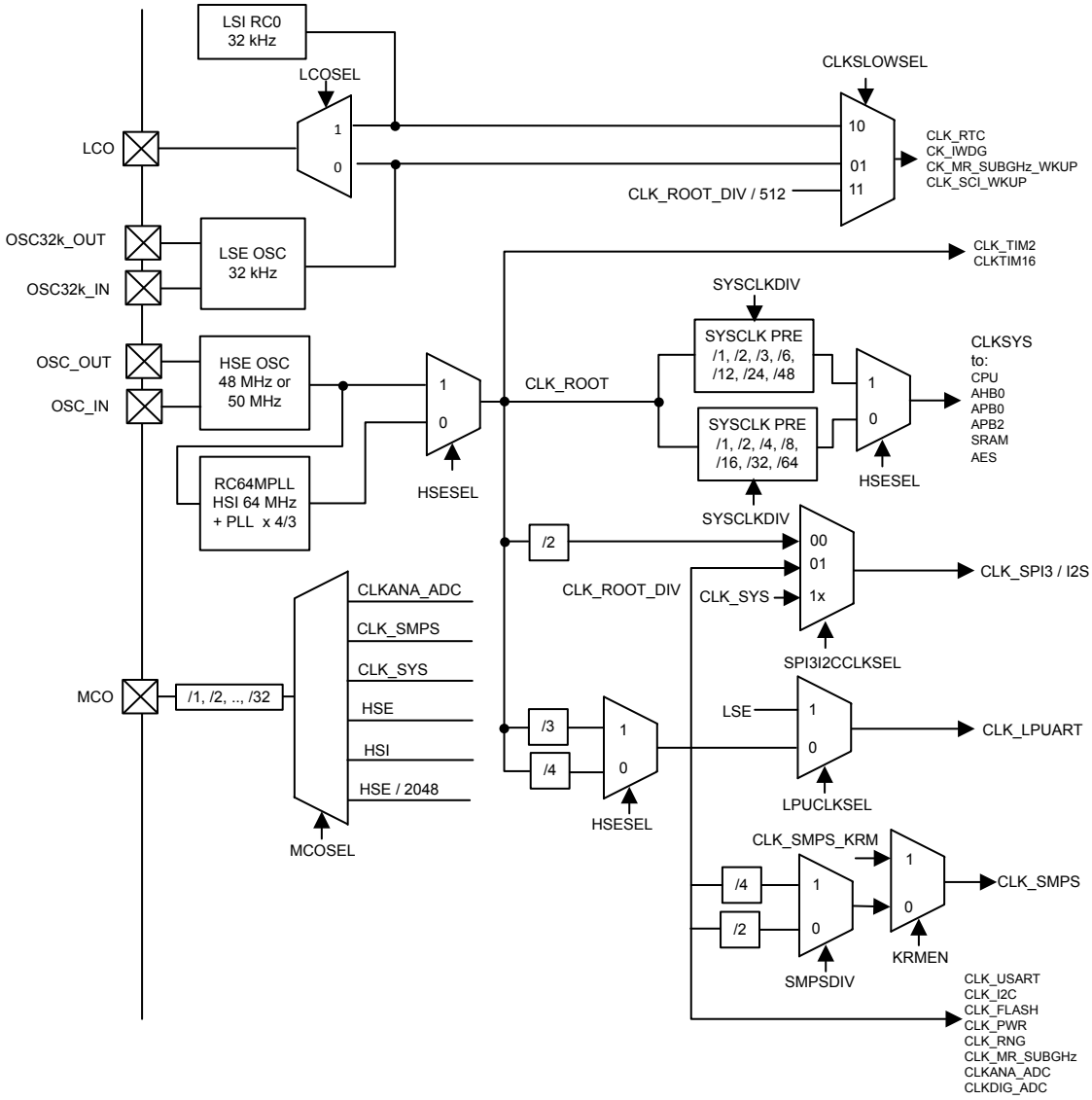
- HSI: high speed internal 64 MHz RC oscillator
- PLL64M: 64 MHz PLL clock based on HSE 48 MHz
- HSE (High Speed External):
  - high speed 48 MHz external crystal
    or
  - provided by a single ended 48 MHz input instead of a crystal

The STM32WL3Rxx has also a slow frequency clock tree used by some peripherals (RTC, watchdog, LPUART, and MR_SUBG radio timer). Three different clock sources can be used for this slow clock tree:

- LSI: low speed low drift internal RC with a fixed frequency between 24 kHz and 49 kHz depending on the sample. It is called the 32 kHz clock within this document for simplicity.
- LSE:
  - 32.768 kHz low speed external crystal.
    or
  - provided by a single-ended 32.768 kHz input instead of a crystal
- The CLOCK_ROOT_DIV/512 (see Figure 7): In this case, the slow clock is not available in Deepstop mode and it must not be used for peripherals working in Deepstop mode.

Figure 7 provides an overview of the fast clock tree in the STM32WL3Rxx.

Figure 7. Fast clock tree generation



3.8.1 System clock details

The HSI and the PLL64M clocks are provided by the same analog block which can synthesize:

- a non-accurate clock (target is 1% typical) when no external XO provides an input clock to this block
- an accurate clock when the external XO provides the 48 MHz and once its internal PLL is locked.

The use of PLL64M or HSE as clock source is mandatory for sub-1 GHz radio operations (because a high accuracy clock is needed).

This fast clock source is used to generate all the fast clocks of the device through dividers as shown in Figure 7. After reset, the CLK_SYS is divided by four to provide a 16 MHz to the whole system (CPU, DMA, memories, and peripherals). Then the software can program another system clock frequency (CLK_SYS) in the following way using the RCC_CFGR.CLKSYSDIV bits:

- 000: CLK_SYS is CLK_ROOT
- 001: CLK_SYS is CLK_ROOT/2
- 010: CLK_SYS is CLK_ROOT/4 (HSESEL = 0) or CLK_ROOT/3 (HSESEL = 1)
- 011: CLK_SYS is CLK_ROOT/8 (HSESEL = 0) or CLK_ROOT/6 (HSESEL = 1) (forbidden when radio is in use)
- 100: CLK_SYS is CLK_ROOT/16 (HSESEL = 0) or CLK_ROOT/12 (HSESEL = 1) (forbidden when radio is in use)
- 101: CLK_SYS is CLK_ROOT/32 (HSESEL = 0) or CLK_ROOT/24 (HSESEL = 1) (forbidden when radio is in use)
- 110: CLK_SYS is CLK_ROOT/64 (HSESEL = 0) or CLK_ROOT/48 (HSESEL = 1) (forbidden when radio is in use)

Forbidden configuration means that the “in use” feature cannot work if the system clock runs at this frequency.

Special care must be taken when programming the CLK_SYS as some constraints need to be respected:

CLK_SYS frequency must be greater or equal to CLK_MR_SUBGHz.

3.9 Boot mode

Following CPU boot, the application software can modify the memory map at address 0x0000 0000. This modification is performed by programming the REMAP bit in the flash controller. The following memory can be remapped:

- main flash memory SRAM0 memory

The STM32WL3Rxx SOC has a pre-programmed bootloader supporting USART protocol with automatic baud rate detection. The main features of the embedded bootloader are:

- auto baud rate detection up to 1 Mbps
- flash mass erase, section erase
- flash programming
- flash readout protection enable/disable

The pre-programmed bootloader is an application, which is stored in the STM32WL3Rxx internal ROM at manufacturing time by STMicroelectronics. This application allows upgrading the device flash memory with a user application using a serial communication channel (USART).

The bootloader is activated by hardware by forcing PA10 high during hardware reset, otherwise, application residing in flash memory is launched.

STMicroelectronics provides a boot loader executed after each CPU reboot. This boot loader has its own documentation.

3.10 General purpose inputs/outputs (GPIO)

Each general-purpose I/O port has four 32-bit configuration registers, two 32-bit data registers, and a 32-bit set/reset register. In addition, all GPIOs have a 32-bit locking register and two 32-bit alternate function selection registers.

Each of the GPIO pins can be configured by software:

- Output states: push-pull or open drain with pull-up/down
- Output data from output data register or peripheral (alternate function output)
- Speed selection for each I/O
- Input states: floating, pull-up/down, analog
- Input data to input data register or peripheral (alternate function input)
- Bit set and reset register for bitwise write access
- Locking mechanism provided to freeze the I/O port configurations
- Analog function
- Alternate function selection registers
- Fast toggle capable of changing every clock cycle
- Highly flexible pin multiplexing allows the use of I/O pins as GPIOs or as one of several peripheral functions.

3.11 Direct memory access (DMA)

Direct memory access (DMA) provides high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps CPU resources free for other operations. The implemented DMA has an arbiter for handling the priority between DMA requests. The DMA main features are as follows:

- Eight independently configurable channels (requests)
- Each of the eight channels is connected to dedicated hardware DMA requests, software trigger is also supported on each channel. This configuration is done by software
- Priorities between requests from channels of the DMA are software programmable (4 levels consisting of very high, high, medium, low) or hardware in case of equality (request 1 has priority over request 2, and so on.)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size
- Support for circular buffer management
- event flags (DMA Half Transfer, DMA Transfer Complete and DMA Transfer Error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer (SRAM0/SRAM1)
- Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to SRAMs, APB0 and APB1 peripherals as source and destination
- Programmable number of data to be transferred: up to 65536

3.12 Nested vectored interrupt controller (NVIC)

The interrupts are handled by the Cortex-M0+ Nested Vector Interrupt Controller (NVIC). The NVIC controls specific Cortex-M0+ interrupts (address 0x00 to 0x3C) as well as 32 user interrupts (address 0x40 to 0xBC). In the STM32WL3Rxx device, the user interrupts have been connected to the interrupt signals of the different peripherals (GPIO, flash controller, timer, USART, and so on). These interrupts can be controlled using the ISER, ICER, ISPR and ICOR registers (see “Cortex-M0+ Devices Generic User Guide”).

3.13 Advanced encryption standard hardware accelerator (AES)

The AES hardware accelerator can be used to both encrypt and decrypt data using the AES algorithm. It is a fully compliant implementation of the advanced encryption standard (AES) as defined by Federal Information Processing Standards Publication (FIPS PUB 197, 2001 November 26). Multiple key sizes and chaining modes are supported: ECB, CBC, CTR for key sizes of 128 bits The AES is a 32-bit AHB peripheral. It supports DMA single transfers for incoming and outgoing data (two DMA channels required). The AES IP provides hardware acceleration to AES crypto algorithm packaged in STM32WL3Rxx crypto library (excluding key length of 192-bit).

The main features of the AES are:

- NIST FIPS publication 197, Advanced Encryption Standard (AES) compliant implementation
- 128-bit data block processing
- Support for cipher keys length of 128-bit
- Encryption and decryption with multiple chaining modes: – Electronic Code Book (ECB) – Cipher Block Chaining (CBC) – Counter Mode (CTR)
- 51 clock cycles for processing one 128-bit block of data with a 128-bit key in ECB mode
- Integrated key scheduler with its key derivation stage (ECB or CBC decryption only)
- 32-bit AHB interface for register accesses, supporting complete 32- bit word access only. (AHB sequential accesses are not supported).
- 128-bit registers for storing initialization vectors (4× 32-bit)
- 1x32-bit INPUT buffer and 1x32-bit OUTPUT buffer
- Automatic data flow control with support of direct memory access (DMA) using two channels (one for incoming data, one for processed data). Single transfers only.
- Data swapping logic to support 1-bit, 8-bit, 16-bit or 32-bit data
- Possibility for software to suspend a message if the IP needs to process another message with a higher priority (context swapping)

3.14 True random number generator (RNG)

The RNG is a random number generator based on a continuous analog noise that provides a 16-bit value to the host when read.

3.15 Cyclic redundancy check (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator with polynomial value and size. Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the flash memory integrity. The CRC calculation unit helps to compute a signature of the software during runtime, which can later be compared with a reference signature generated at link-time, and which can be stored at a given memory location.

3.16 General purpose timers

The STM32WL3Rxx embeds one general purpose timer (TIM2) supporting up to 4 independent channels, one general purpose timer (TIM16) supporting one single channel and one complementary.

3.16.1 General Purpose timer (TIM2)

The general purpose 16-bit timer (TIM2) consists of a 16-bit auto-reload counter driven by a programmable prescaler.

It may be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (output compare, PWM). Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler on the timer input clock which is at 32MHz.

The TIM2 main features are:

- 16-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler allowing division (also “on the fly”) the counter clock frequency either by any factor between 1 and 65536
- Up to 4 independent channels for:
  - input capture
  - output compare
  - PWM generation (edge and center-aligned mode)
  - one-pulse mode output
- Synchronization circuit to control the timer with external signals and to interconnect several timers together
- Repetition counter to update the timer registers only after a given number of cycles of the counter
- Interrupt/DMA generation on the following events:
  - update: counter overflow/underflow, counter initialization (by software or internal/external trigger)
  - input capture
  - output comparison
  - trigger event (counter start, stop, initialization or count by internal/external trigger)
- Supports incremental (quadrature) encoder for positioning purposes
- Trigger input for external clock or cycle-by-cycle current management
- The counter can be frozen in debug mode

3.16.2 General purpose timer (TIM16)

The TIM16 timer consists of a 16-bit auto-reload counter driven by a programmable prescaler. It may be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion).

Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the RCC clock controller prescaler.

The main TIM16 features are:

- 16-bit auto-reload upcounter
- 16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535
- One channel for:
  - input capture
  - output comparison
  - PWM generation (edge-aligned mode)
  - one-pulse mode output
  - trigger event (counter start, stop, initialization or count by internal/external trigger)
- Complementary output with programmable dead-time
- Synchronization circuit to control the timer with external signals and to interconnect several timers together
- Repetition counter to update the timer registers only after a given number of cycles of the counter
- Break input to put the timer’s output signals in the reset state or a known state

- Interrupt/DMA generation on the following events:
  - update: counter overflow
  - input capture
  - output comparison
  - break input (interrupt request)
- The counter can be frozen in debug mode.

3.17 Independent watchdog (IWDG)

The STM32WL3Rxx integrates an embedded watchdog peripheral which offers a combination of high safety level, timing accuracy and flexibility of use. The independent watchdog peripheral serves to detect and resolve malfunctions due to software failure, and to trigger system reset when the counter reaches a given timeout value.

The independent watchdog (IWDG) is clocked by its own dedicated low-speed clock (LSI) and thus stays active even if the main clock fails.

The IWDG is best suited to applications which require the watchdog to run as a totally independent process outside the main application but have lower timing accuracy constraints. The counter can be frozen in debug mode.

3.18 Real-time clock (RTC)

The STM32WL3Rxx integrates a real-time clock (RTC). It is an independent BCD timer/counter. The RTC provides a time of day/clock/calendar with programmable alarm interrupt. RTC includes also a periodic programmable wake-up flag with interrupt capability. The RTC provides an automatic wake-up to manage all low power modes.

Two 32-bit registers contain seconds, minutes, hours (12- or 24-hour format), day (day of week), date (day of month), month, and year, expressed in binary coded decimal format (BCD). The sub-second value is also available in binary format. Compensations for 28-, 29- (leap year), 30-, and 31-day months are performed automatically. Daylight saving time compensation can also be performed. Additional 32-bit registers contain the programmable alarm sub seconds, seconds, minutes, hours, day, and date.

One anti-tamper detection pin with programmable filter is available. A timestamp feature can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, by a tamper event, or by a switch to Deepstop mode.

A digital calibration circuit is available to compensate for quartz crystal inaccuracy. After power-on reset, all RTC registers are protected against possible parasitic write accesses. As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, low power mode or under system reset).

The RTC contains 5 backup registers which are supplied through a switch that takes power either from the VDD12I supply (when present) or from the VDD12O pin.

The backup registers are 32-bit registers used to store 20 bytes of user application data when VDD12I power is not present. They are not reset by a system or power reset, or when the device wakes up from Deepstop mode.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes. The counter can be frozen in debug mode.

3.19 Inter-integrated circuit interface (I2C)

The I2C (inter-integrated circuit) bus interface handles communications between the microcontroller and the serial I2C bus. It provides multi master capability, and controls all I2C bus-specific sequencing, protocol, arbitration, and timing. It supports Standard-mode (Sm), Fast-mode (Fm) and Fast-mode Plus (Fm+).

It is also SMBus (system management bus) and PMBus (power management bus) compatible.

DMA can be used to reduce CPU overload. The counter can be frozen in debug mode.

3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32WL3Rxx embeds a universal synchronous asynchronous receiver transmitter (USART) that offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. The USART offers a very wide range of baud rates using a fractional baud rate generator.

It supports synchronous one-way communication and half-duplex single wire communication. It also supports the local interconnection network (LIN), SmartCard Protocol and IrDA (infrared data association) SIR ENDEC specifications, and modem operations (CTS/RTS). It also supports multiprocessor communications.

High speed data communication is possible by using the DMA (direct memory access) for multibuffer configuration.

The USART main features are:

- Full-duplex asynchronous communication
- NRZ standard format (mark/space)
- Configurable oversampling method by 16 or 8 to give flexibility between speed and clock tolerance
- Baud rate generator systems
- Two internal FIFOs for transmit and receive data, that can be enabled/disabled by software. FIFOs come with status flags for FIFOs states.
- A common programmable transmit and receive baud rate of up to 2 Mbit/s with the clock frequency at 16 MHz and oversampling is by 8.
- Dual clock domain with a dedicated kernel clock allowing baud rate programming independent from the PCLK reprogramming.
- Auto baud rate detection
- Programmable data word length (7 or 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Synchronous master/slave mode and clock output/input for synchronous communications
- SPI slave transmission underrun error flag Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Communication control/error detection flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Interrupt sources with flags
- Multiprocessor communications
- Wake up from mute mode (by idle line detection or address mark detection)

3.21 Low-power universal asynchronous receiver transmitter (LPUART)

The low power universal asynchronous receiver transmitted (LPUART) is an UART which allows bidirectional UART communications with a limited power consumption. Only 32.768 kHz LSE clock is required to allow UART communications up to 9600 baud/s. Higher baud rates can be reached when the LPUART is clocked by clock sources different from the LSE clock.

Even when the microcontroller is in stop mode, the LPUART can wait for an incoming UART frame while having an extremely low energy consumption. The LPUART includes all necessary hardware support to make asynchronous serial communications possible with minimum power consumption.

It supports half-duplex single wire communications and modem operations (CTS/RTS). It also supports multiprocessor communications.

DMA (direct memory access) can be used for data transmission/reception.

The main features are:

- Full-duplex asynchronous communications
- NRZ standard format (mark/space)
- Programmable baud rate
- From 300 baud/s to 9600 baud/s using a 32.768 kHz clock source
- Higher baud rates can be achieved by suing a higher frequency clock source
- Two internal FIFOs for transmit and receive data, that can be enabled/disabled by software. FIFOs come with status flags for FIFOs states.
- Dual clock domain allowing:
  - UART functionality and wakeup from stop mode
  - convenient baud rate programming independent from the PCLK reprogramming
- Programmable data word length (7 or 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Transfer detection flags:
  - receive buffer full
  - transmit buffer empty
  - busy and end-of-transmission flags
- Parity control:
  - transmits parity bit
  - checks parity of received data byte
- Four error detection flags:
  - overrun error
  - noise detection
  - frame error
  - parity error
- Interrupt sources with flags
- Multiprocessor communications: the LPUART enters mute mode if the address does not match
- Wakeup from mute mode (by idle line detection or address mark detection)

3.22 Serial peripheral interface (SPI/I2S)

The STM32WL3Rxx embeds a serial peripheral interface (SPI3). The SPI3 supports the I2S protocol in addition to SPI features.

SPI or I2S mode is selectable by software. SPI Motorola mode is selected by default after a device reset.

The SPI interfaces allow communication at up to 32 Mbit/s in both master and slave modes.

The serial peripheral interface (SPI) protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices. The interface can be configured as master, and in this case it provides the communication clock (SCK) to the external slave device. The interface is also capable of operating in multimaster configuration.

The Inter-IC sound (I2S) protocol is also a synchronous serial communication interface. It can operate in slave or master mode with full duplex and half-duplex communication. It can address four different audio standards including the Philips I2S standard, the MSB- and LSB-justified standards and the PCM standard.

The main SPI features are:

- Master or slave operation
- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- 4-bit to 16-bit data size selection
- Multimaster mode capability
- 8 master mode baud rate prescalers up to fPCLK/2
- Slave mode frequency up to fPCLK/2
- NSS management by hardware or software for both master and slave: dynamic change of master/slave operations
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Dedicated transmission and reception flags with interrupt capability
- SPI bus busy status flag
- SPI Motorola support
- Hardware CRC feature for reliable communication:
  - CRC value can be transmitted as last byte in Tx mode
  - automatic CRC error checking for last received byte
- Master mode fault, overrun flags with interrupt capability
- CRC error flag
- Two 32-bit embedded Rx and Tx FIFOs with DMA capability
- SPI TI mode support
- DMA capability for transmission and reception (16-bit wide)

The main I2S features are:

- Half-duplex communication (only transmitter or receiver)
- Master or slave operations
- 8-bit programmable linear prescaler to reach accurate audio sample frequencies (from 8 kHz to 192 kHz)
- Data format may be 16-bit, 24-bit or 32-bit
- Packet frame is fixed to 16-bit (16-bit data frame) or 32-bit (16-bit, 24-bit, 32-bit data frame) by audio channel
- Programmable clock polarity (steady state)
- Underrun flag in slave transmission mode, overrun flag in reception mode (master and slave) and Frame Error Flag in reception and transmitter mode (slave only)
- 16-bit register for transmission and reception with one data register for both channel sides

- Supported I2S protocols:
  - I2S Philips standard
  - MSB-Justified standard (left-justified)
  - LSB-Justified standard (right-justified)
  - PCM standard (with short and long frame synchronization on 16-bit channel frame or 16-bit data frame extended to 32-bit channel frame)
- Data direction is always MSB first
- DMA capability for transmission and reception (16-bit wide)
- Master clock can be output to drive an external audio component. Ratio is fixed at 256 × FS (where FS is the audio sampling frequency)

3.23 Analog digital converter (ADC)

The STM32WL3Rxx SOC embeds a 12-bit ADC. The ADC consists in a 12-bit successive approximation analog-to-digital converter (SAR) with 2 x 8 multiplexed channels allowing measurements of up to eight external sources and up to three internal sources.

The main ADC features are:

- Conversion frequency is up to 1 Msample/s
- Three input voltage ranges are supported (0 to 1.2 V, 0 to 2.4 V, 0 to 3.6 V)
- Up to eight analog single ended channels or four analog differential inputs or a mix of both.
- Temperature sensor conversion.
- Battery level conversion up to 3.6 V
- ADC mode conversion only available, programmable in continuous or single mode
- ADC Down Sampler for multi-purpose applications to improve analog performance while off-loading the CPU (ratio adjustable from 1 to 128)
- A watchdog feature to inform when data is outside thresholds
- DMA capability
- Interrupt sources with flags

3.23.1 Temperature sensor

The temperature sensor can be used to measure the junction temperature (T_j) of the device. The temperature sensor is internally connected to the ADC input channels which are used to convert the sensor output voltage to a digital value. To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

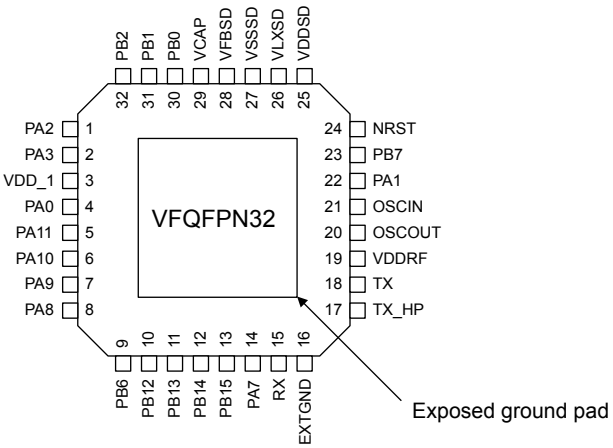
3.24 Debug support (DBG)

The STM32WL3Rxx embeds an Arm serial wire debug (SWD) interface that enables interactive debugging and programming of the device. The interface is composed of only two pins: SWDIO and SWCLK. The enhanced debugging features for developers allow up to 4 breakpoints and up to 2 watchpoints.

4 Pinouts and pin descriptions

The STM32WL3Rxx comes in a VQFPN32 package offering 18 GPIOs.

Figure 8. Pinout top view (QFN32 package - 5 mm x 5 mm)



DT58216V1

Note: All PAx and PBx type pins can wake up the circuit.

Table 4. Pin description

Pin number	Pin Name (function after reset)	Pin type	Alternate functions	Additional functions
1	PA2	I/O	SWDIO, USART1_CK, TIM16_CH1, I2S3_MCK, TIM2_CH1	ADC_VINM2
2	PA3	I/O	SWCLK, USART1_RTS_DE, TIM16_CH1N, SPI3_SCK/I2S3_CK, TIM2_CH2	ADC_VINP2
3	VDD_1	S	-	1.7 to 3.6 V battery voltage input
4	PA0	I/O	I2C1_SCL, USART1_CTS, TIM2_CH3	WKUP12
5	PA11	I/O	MCO, RX_SEQUENCE, SPI3_MOSI/I2S3_SD, SUBG_TX_CLOCK	WKUP11
6	PA10	I/O	LPUART1_CTS, TX_SEQUENCE, I2S3_MCK, SUBG_TX_DATA	LCO
7	PA9	I/O	USART1_TX, RTC_OUT, SPI3_NSS/I2S3_WS, TIM2_CH4	WKUP9
8	PA8	I/O	RTC_OUT/RTC_TAMP1/RTC_TS, USART1_RX, RX_SEQUENCE, SPI3_MISO, TIM2_CH3	WKUP8
9	PB6	I/O	I2C1_SCL, LPUART1_TX, SPI3_SCK/I2S3_CK, TIM2_CH3	-
10	PB12	I/O	USART1_RTS_DE, LPUART1_CTS, LCO, TIM2_CH3	RCC_OSC32_OUT
11	PB13	I/O	TIM2_CH4	RCC_OSC32_IN
12	PB14	I/O	I2C1_SMBA, USART1_RX, TX_SEQUENCE, MCO, TIM2_ETR	PVD_IN
13	PB15	I/O	USART1_TX	-
14	PA7	I/O	LPUART1_RTS_DE, TIM2_CH2	WKUP7
15[1]	RX	I/RF	-	RF RX port
16	EXTGND	S	-	-
17	TX_HP	O/RF	-	RF TX port
18	TX	O/RF	-	RF TX port
19	VDDRF	S	-	1.7 to 3.6 V battery voltage input
20	OSCOUT	I/O	-	48 MHz crystal
21	OSCIN	I/O	-	48 MHz crystal
22	PA1	I/O	I2C1_SDA, USART1_TX, TIM16_BRK, TIM2_CH4	-
23	PB7	I/O	I2C1_SDA, LPUART1_RX, RF_ACTIVITY, SPI3_MOSI/ I2S3_SD, TIM2_ETR	-
24	NRST	RSTS	-	Reset pin
25	VDDSD	S	-	1.7 to 3.6 V battery voltage input SMPS input
26	VLXSD	S	-	SMPS LX pin
27	VSSSD	S	-	SMPS Ground

Pin number	Pin Name (function after reset)	Pin type	Alternate functions	Additional functions
28	VFBSD	S	-	SMPS output
29	VCAP	S	-	1.2 V digital core
30	PB0	I/O	USART1_RX, LPUART1_RTS_DE, TIM16_CH1, ANTENNA_SWITCH	ADC_VINM1, WKUP0
31	PB1	I/O	USART1_CK, SWDIO, TIM16_CH1N, SUBG_RX_DATA	ADC_VINP1
32	PB2	I/O	USART1_RTS_DE, SWCLK, TIM16_BRK, SUBG_RX_CLOCK	ADC_VINM0
Exposed pad	GND	S	-	Ground

1. *For part numbers with transmitter only, pin 15 is not connected and must left floating.*

Table 5. Alternate function port A

Port		AF0	AF1	AF2	AF3	AF4	AF5
		I2C1/ SYS_AF/RTC/ USART	SYS_AF/ USART/ LPUART	SYS_AF/ TIM2	SYS_AF/ SPI3	SYS_AF/ TIM2	SYS_AF/ Single-wire debug
Port A	PA0	I2C1_SCL	USART1_CTS	-	-	TIM2_CH3	-
	PA1	I2C1_SDA	USART1_TX	TIM16_BRK	-	TIM2_CH4	-
	PA2	SWDIO	USART1_CK	TIM16_CH1	I2S3_MCK	TIM2_CH1	SWDIO
	PA3	SWCLK	USART1_RTS_DE	TIM16_CH1N	SPI3_SCK/ I2S3_CK	TIM2_CH2	SWCLK
	PA7	-	LPUART1_RTS_DE	-	-	TIM2_CH2	-
	PA8	RTC_OUT/ RTC_TAMP1/ RTC_TS	USART1_RX	RX_SEQUENCE	SPI3_MISO	TIM2_CH3	-
	PA9	-	USART1_TX	RTC_OUT	SPI3_NSS/ I2S3_WS	TIM2_CH4	-
	PA10	-	LPUART1_CTS	TX_SEQUENCE	I2S3_MCK	SUBG_TX_DATA	-
	PA11	MCO	-	RX_SEQUENCE	SPI3_MOSI/ I2S3_SD	SUBG_TX_CLOCK	-

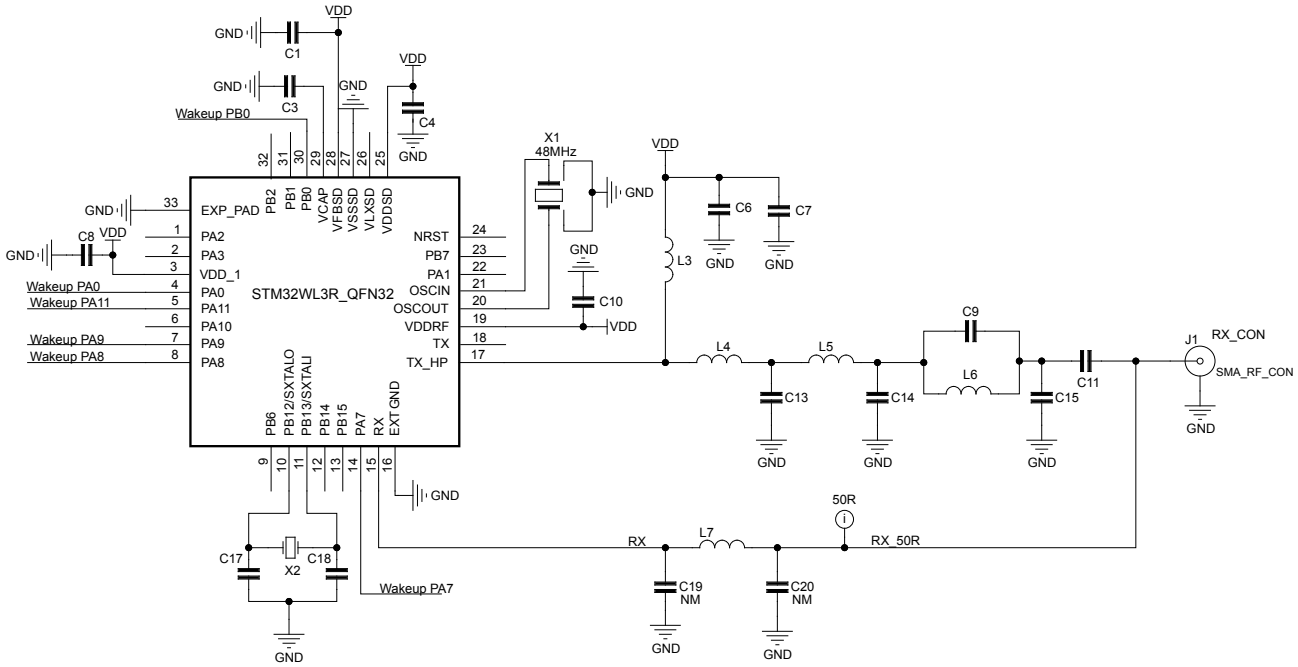
Table 6. **Alternate function port B**

Port		AF0	AF1	AF2	AF3	AF4	AF5
		I2C1/ SYS_AF/RTC/ USART	SYS_AF/ USART/ LPUART	SYS_AF/ TIM16	SYS_AF/ SPI3	SYS_AF/ TIM2	SYS_AF/
Port B	PB0	USART1_RX	LPUART1_RTS_DE	TIM16_CH1	-	ANTENNA_SWITCH	-
	PB1	USART1_CK	SWDIO	TIM16_CH1N	-	SUBG_RX_DATA	-
	PB2	USART1_RTS_DE	SWCLK	TIM16_BRK	-	SUBG_RX_CLOCK	-
	PB6	I2C1_SCL	LPUART1_TX	-	SPI3_SCK/ I2S3_CK	TIM2_CH3	-
	PB7	I2C1_SDA	LPUART1_RX	RF_ACTIVITY	SPI3_MOSI/ I2S3_SD	TIM2_ETR	-
	PB12	USART1_RTS_DE	LPUART1_CTS	LCO	-	TIM2_CH3	-
	PB13	-	-	-	-	TIM2_CH4	-
	PB14	I2C1_SMBA	USART1_RX	TX_SEQUENCE	MCO	TIM2_ETR	-
	PB15	-	USART1_TX	-	-	-	-

5 Application circuits

The schematics below are purely indicative.

Figure 9. STM32WL3Rxx application circuit without SMPS



DT58217

Figure 10. STM32WL3Rxx application circuit with SMPS

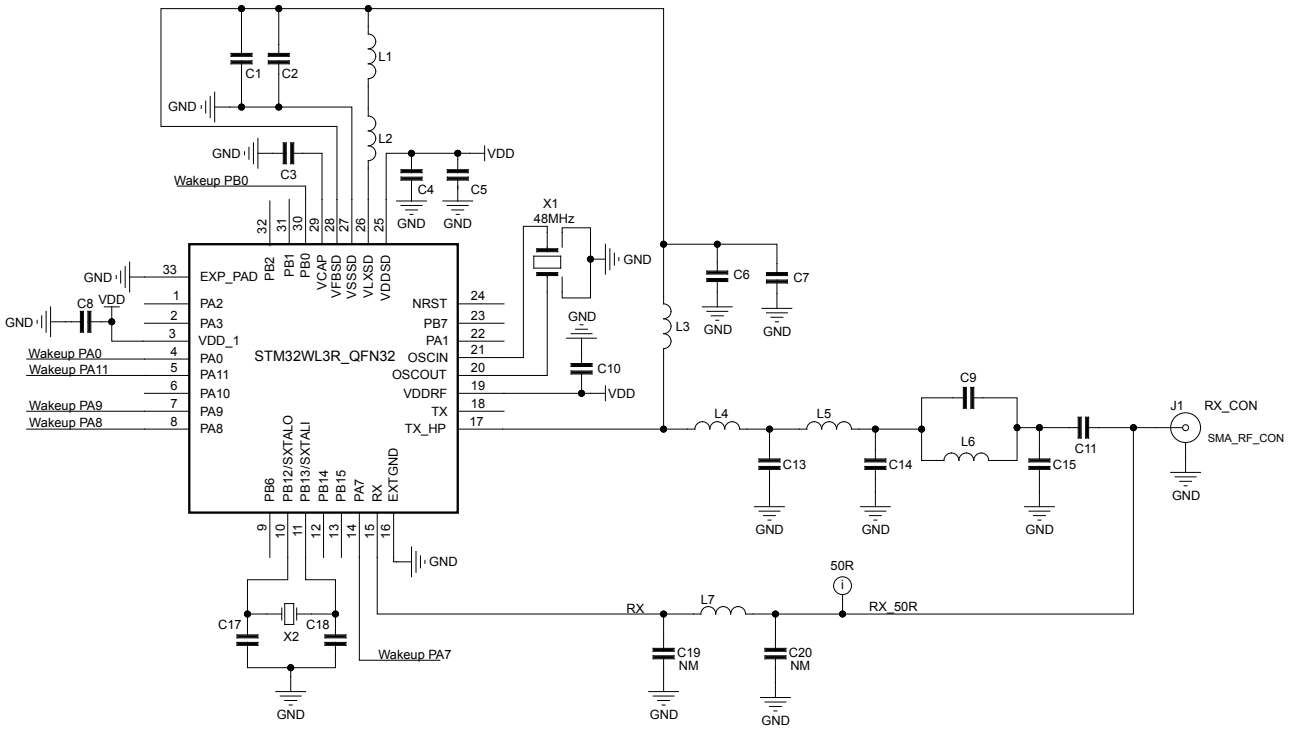


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Table 7. Application circuit external components

Components	Description
C8	Decoupling capacitor for VDD_1
C10	Decoupling capacitor for VDDRF
C3	Decoupling capacitor for VCAP
C4, C5	Decoupling capacitor for VDDSD. Input capacitors for internal DCDC converter
C1, C2	Output capacitors for internal DCDC converter
L1	Power inductor for DCDC converter.
L2	SMPS noise filter
C6, C7	Decoupling capacitor for PA VDD pin
C17, C18	32.768 kHz crystal loading capacitors
L3	RF choke inductor
L7, C19, C20	Filter/matching for RX path
L4, C13, L5, C14	Filter/matching for TX path
C9, L6, C15	Notch filter and low pass filter
C11	DC blocking capacitor
X1	48 MHz crystal

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK2 packages, depending on their level of environmental compliance. ECOPACK2 specifications, grade definitions, and product status are available at: www.st.com. ECOPACK2 is an ST trademark.

6.1 Device marking

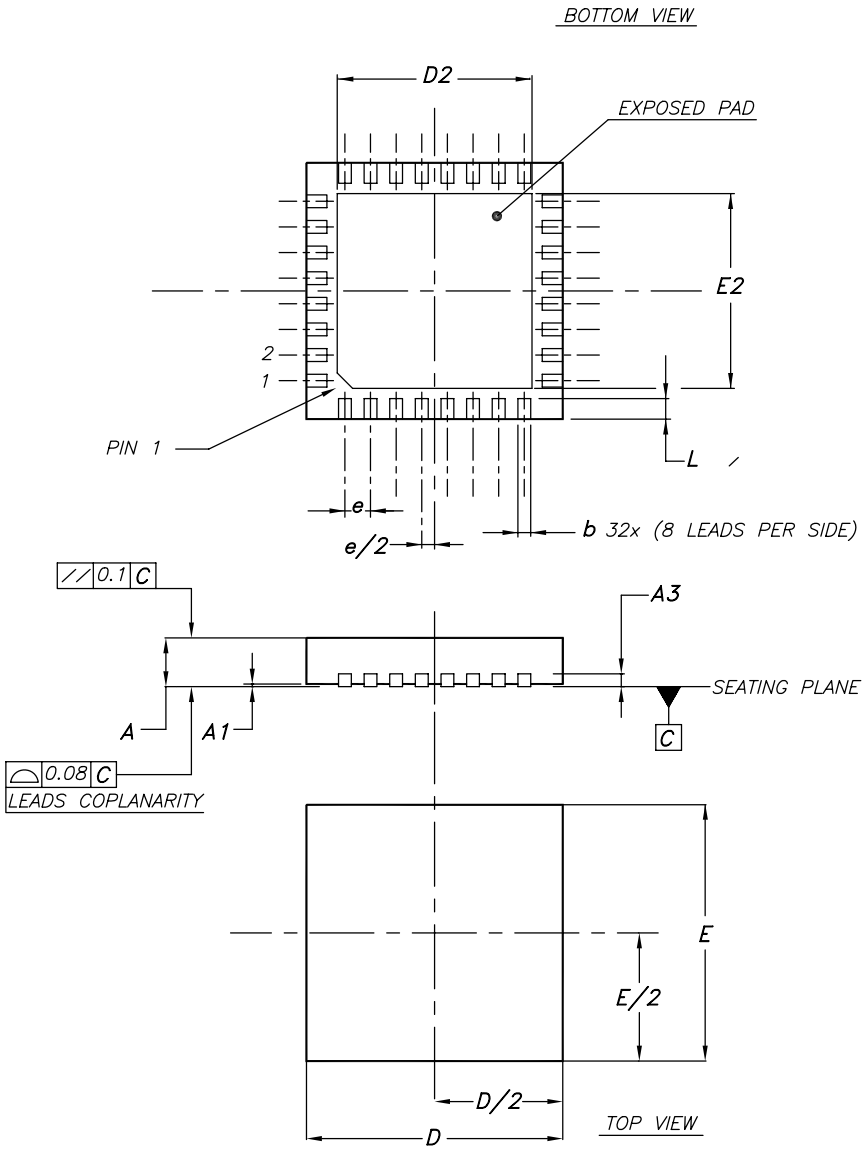
Refer to technical note “Reference device marking schematics for STM32 microcontrollers and microprocessors” (TN1433) available on http://www.st.com, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.2 VFQFPN32 package information (42)

This VFQFPN is a 32 lead, 5 x 5 mm, 0.50 mm pitch, very fine pitch quad flat no lead package.

Figure 11. VFQFPN32 - Outline



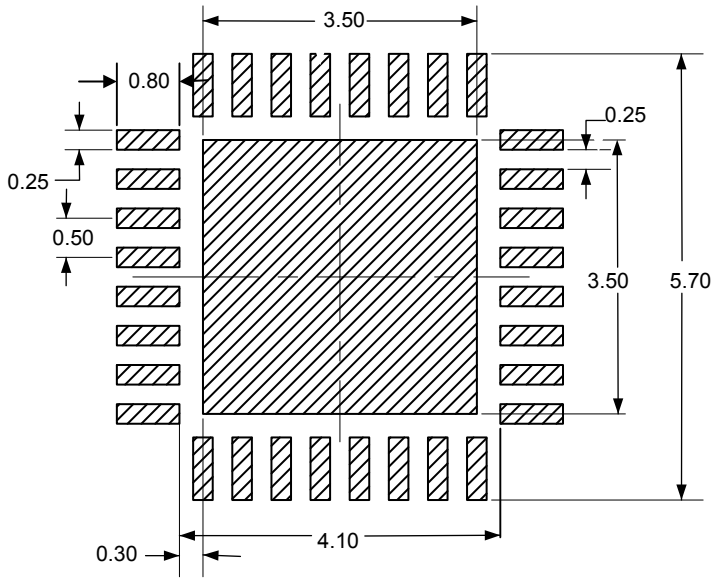
1. *Drawing is not to scale.*

Table 8. VFQFPN32 - Mechanical data

Symbol	Millimetres			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	-	0.02	0.05	-	0.0008	0.0020
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
D	4.85	5.00	5.15	0.1909	0.1969	0.2028
E	4.85	5.00	5.15	0.1909	0.1969	0.2028
D2	3.65	-	3.95	0.1437	-	0.1555
E2	3.65	-	3.95	0.1437	-	0.1555
e	-	0.50	-	-	0.0197	-
L	0.30	0.40	0.50	0.0118	0.0157	0.0197

1. *Values in inches are converted from mm and rounded to 3 decimal digits.*

Figure 12. VFQFPN32 - Footprint example



7 Ordering information

Table 9. Ordering information scheme

Example: STM32 WL 3R K 8 V 6 TR

Device family

STM32 = Arm-based 32-bit microcontroller

Product type

WL = wireless long-range

Device subfamily

3R = Cortex-M0+ Remote control line

Pin count

K = 32

Memory configuration

8 = 64 Kbyte flash/8 Kbyte RAM

B = 128 Kbyte flash/16 Kbyte RAM

Package(1)

V = VFQFPN

Temperature range

6 = -40 °C up to +85 °C

7 = -40 °C up to +105 °C

Frequency band options

No character = 276 - 319 MHz, 413-479 MHz and 868-958 MHz

X = Transmitter only

Packing

TR = tape and reel

1. *ECOPACK2 (RoHS compliant and free of brominated, chlorinated and antimony oxide flame retardants).*

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Revision history

Table 10. **Document revision history**

Date	Version	Changes
14-Nov-2025	1	Initial release.

Contents

List of tables

List of figures

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