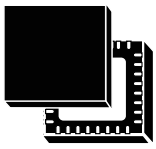
STSAFE-V100-Qi

Data brief

Automotive authentication device for Wireless Qi charging



UFQFPN32 WF (5 × 5 × 0.55 mm)

Features

Automotive feature

- AEC-Q100 qualified

Certification, compliancy, and authentication features

- WPC compliancy with QI1.3 and QI2.0 authentication process
- Asymmetric cryptography :
  - Elliptic curve digital signature algorithm (*ECDSA*) with *SHA*-256 for digital signature generation and verification
- Hardware Common Criteria EAL6+ certification:
  - Common criteria compliance

Hardware features

- Highly reliable flash memory technology
- Operating temperature range (automotive grade 2): −40 °C to 105 °C
- Electrostatic discharge (ESD) protection up to 4 kV (HBM)
- 1.8 V or 3.3 V supply voltage range
- *SPI* support at up to 48 MHz
- *I²C* support at up to 1 MHz
- Common criteria EAL 6+

1 Description

The STSAFE-V products offer a broad portfolio of secure automotive solutions. Our family STSAFE-V100-Qi is a dedicated solution for *WPC* QI charging.

It includes a dedicated solution for *WPC* (wireless power consortium) QI wireless charging in Vehicle. STSAFE-V100-Qi is compliant with *WPC* 1.3.x and 2.0 authentication protocol.

The STSAFE-V100 family provides services to protect the confidentiality, integrity and authenticity of information and devices.

The STSAFE-V100-Qi operates in the –40 °C to 105 °C automotive temperature range.

The STSAFE-V100-Qi devices are qualified for AEC Q100 automotive applications and are offered UFQFPN32 wettable flanks and TSSOP20 packages.

The TSSOP20 package is proposed as an option at this stage.

The STSAFE-V100-Qi devices are offered in Ecopack2 packages.

2 Pin and signal description

2.1 UFQFPN32 pin and signal description

The figure below gives the pinout of the UFQFPN32 package in which the devices are delivered. Table 1 describes the associated signals.

Figure 1. UFQFPN32 pinout

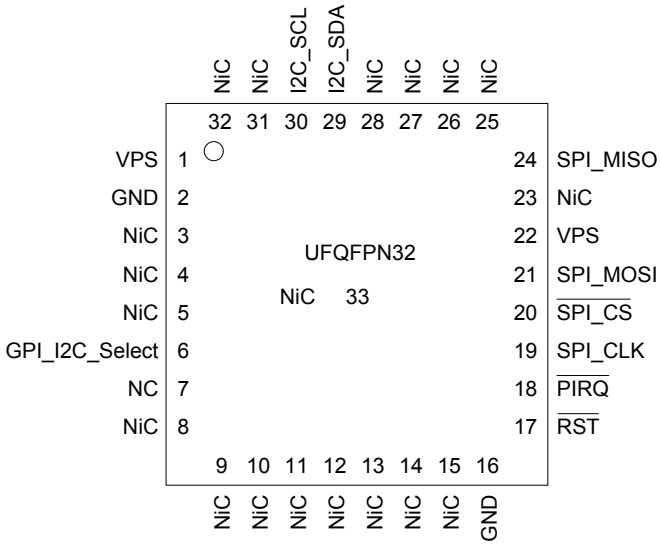


Table 1. UFQFPN32 descriptions

Signal	Type	Description
VPS	Input	**Power supply**. This pin must be connected to 1.8 V or 3.3 V DC power rail supplied by the motherboard.
GND	Input	**Ground**, has to be connected to the main motherboard ground.
$\overline{\text{RST}}$	Input	**Reset**, active low, used to re-initialize the device. Must not be unconnected. External pull-up resistor required if it cannot be driven.
SPI_MISO	Output	***SPI* master input, slave output** (output from slave)
SPI_MOSI	Input	***SPI* master output, slave input** (output from master)
SPI_CLK	Input	***SPI* serial clock** (output from master)
$\overline{\text{SPI\_CS}}$	Input	***SPI* chip (or slave) select**, internal pull-up (active low; output from master)
$\overline{\text{PIRQ}}$	Output	**IRQ**, active low, open drain, used by the device to generate an interrupt
NC	Input	Must not be connected
GPI_I2C_Select	Input	This pin must be connected to an external pull-down resistor to activate the *I²C* protocol during product boot time. It can remain unconnected for the *SPI* protocol. This pin is internal pull-up by default and becomes internal floating after *I²C* activation.
NiC	-	**Not internally connected**: not connected to the die. May be left unconnected but no impact on device if connected.
I2C_SDA	Input/output	**Bidirectional *I²C* serial data** (open drain without a weak pull-up resistor)
I2C_SCL	Input	**Input *I²C* serial clock** (open drain without a weak pull-up resistor)

Note: The UFQFPN32 package has a central pad (PIN33) on the bottom, which is not connected to the die. This pin does not impact the STSAFE-V100-Qi, be it connected or not.

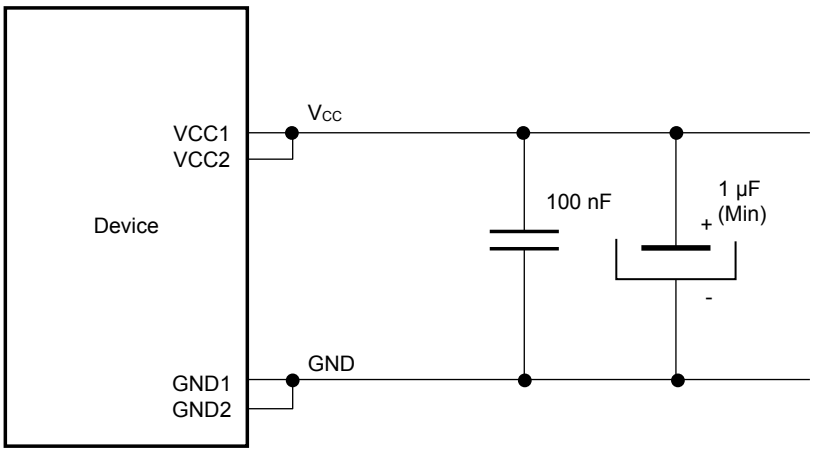
3 Electrical integration guidance

This section gives some guidance on how to integrate the STSAFE-V100-Qi device in an application.

3.1 Recommended power supply filtering

The power supply of the device should be filtered using the circuit shown in the figure below.

Figure 2. Recommended filtering capacitors on V_{CC}



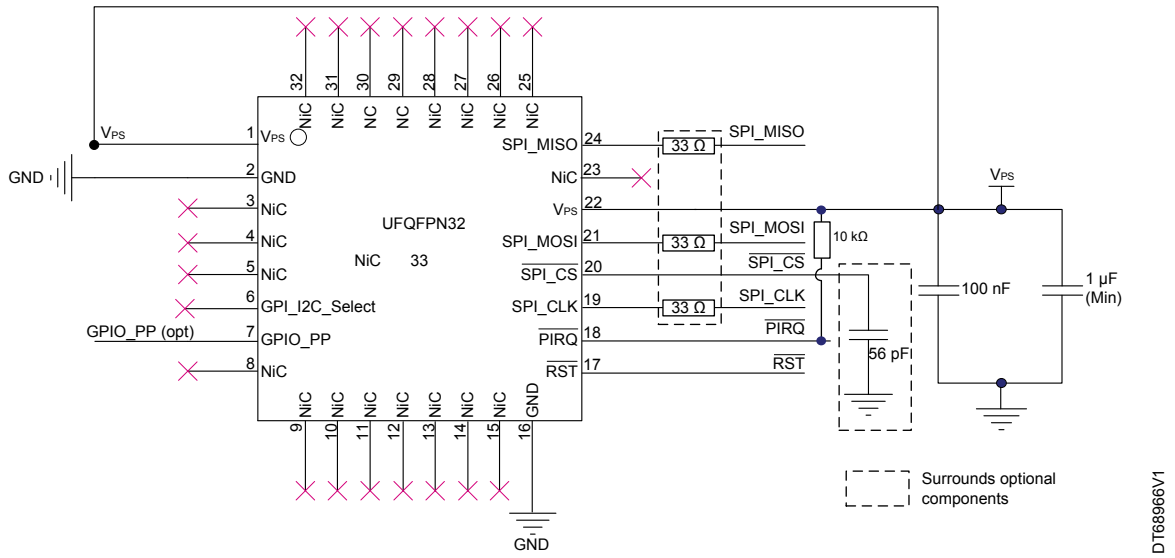
3.2 $\overline{\text{SPI\_CS}}$ optional filtering

Recommendation for SPI_CS integration: It is mandatory that SPI_CLK is at the low logic level when the falling edge occurs on the SPI_CS signal. An external capacitance of 56 pF is recommended on SPI_CS for that purpose. This capacitor might not be required depending on the intrinsic line capacitance, the SPI bus frequency, or both.

3.3 Device integration for SPI communication

The figure below shows the typical hardware implementation of the STSAFE-V100-Qi device for *SPI* communication.

Figure 3. Typical hardware implementation for SPI communication (UFQFPN32 package)



Note: The use of a low-value resistor (typically 33 Ω) on SPI_MISO, SPI_MOSI and SPI_CLK can be recommended for line adaptation when the signals are affected by parasite spikes. Its use is mandatory to avoid disturbance of the ramp-up and ramp-down signals.

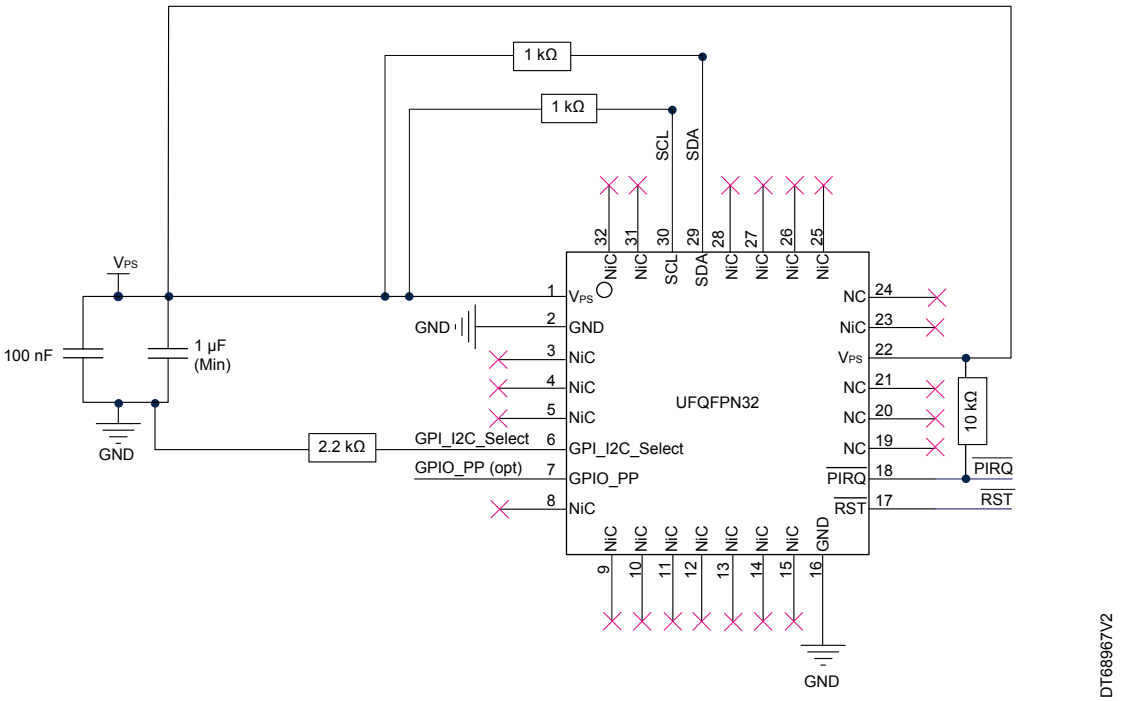
Note: The capacitor on $\overline{SPI\_CS}$ is optional (see Section 3.2 $\overline{SPI\_CS}$ optional filtering).

Note: The pull-up resistor on the PIRQ line is mandatory to optimize the power consumption in standby mode.

3.4 Device integration for I²C communication

The figure below shows the typical hardware implementation of the STSAFE-V100-Qi device for *I²C* communication.

Figure 4. Typical hardware implementation for *I²C* communication (UFQFPN32 package)



Note: The pull-up resistor on the $\overline{PIRQ}$ line is mandatory to optimize the power consumption in standby mode.

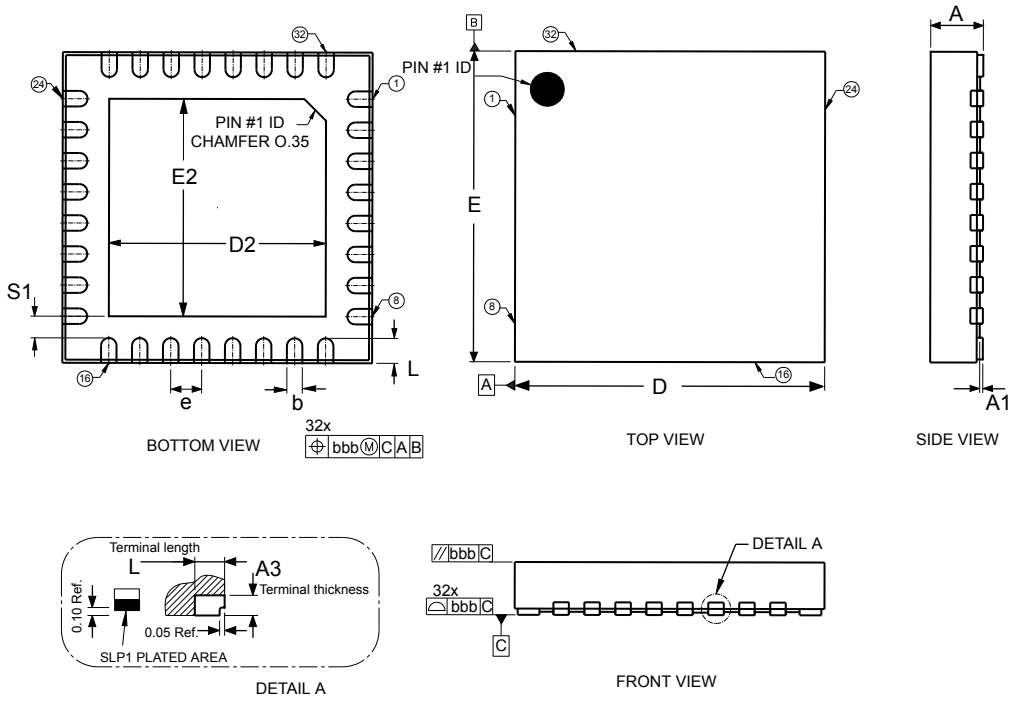
4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 UFQFPN32 package information (B0EY)

This UFQFPN is a 32 lead wettable flank, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package.

Figure 5. UFQFPN32 - Outline



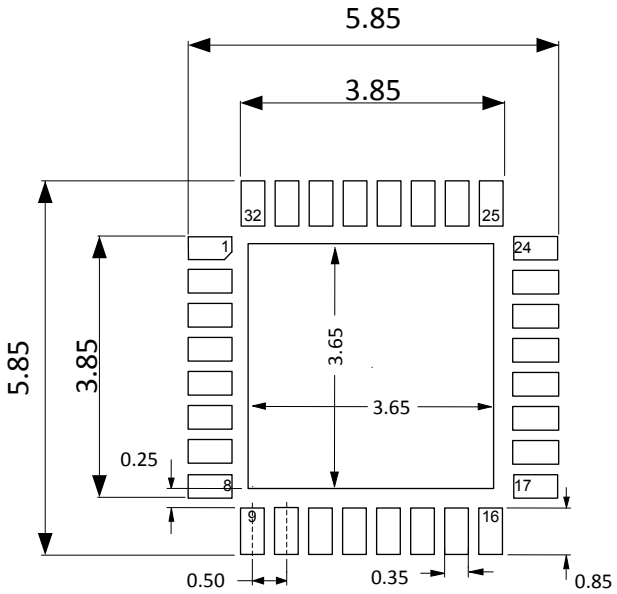
1. *Drawing is not to scale.*
2. *Coplanarity applies to the exposed pad as well as the terminal.*

Table 2. UFQFPN32 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.55	0.65	0.0197	0.0217	0.0256
A1	-	0.05	-	-	0.0020	-
A3		0.152 ref.			0.0060 ref.	
L	0.30	0.40	0.50	0.0118	0.0157	0.0196
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
D		5.00 BSC			0.1968 BSC	
E		5.00 BSC			0.1968 BSC	
e		0.50 BSC			0.0197 BSC	
D2	3.50	3.65	3.80	0.1377	0.1437	0.1496
E2	3.50	3.65	3.80	0.1377	0.1437	0.1496
S1		0.30 ref.			0.0118 ref.	
N[2]			32			
bbb	-	0.10	-	-	0.0039	-
ccc	-	0.10	-	-	0.0039	-
eee	-	0.08	-	-	0.0031	-

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *Total number of terminals.*

Figure 6. UFQFPN32 - PCB footprint example



1. *Dimensions are expressed in millimetres.*
2. *Pin 1 is identified in the PCB footprint example. The location of this pin must be identified using the customer manufacturing process.*

5 Delivery packing

5.1 UFQFPN32 - tape and reel delivery packing

Surface-mount packages can be supplied with tape and reel packing. The reels have a 13" typical diameter.

Reels are in plastic, either anti-static or conductive, with a black conductive cavity tape. The cover tape is transparent anti-static or conductive.

The devices are positioned in the cavities with the identifying pin (normally Pin “1”) on the same side as the sprocket holes in the tape.

The STMicroelectronics tape and reel specifications are compliant with the EIA 481-A standard specification.

Table 3. UFQFPN32 - packages on tape and reel

Package	Description	Tape width	Tape pitch	Reel diameter	Quantity per reel
UFQFPN32	Very thin fine pitch quad flat pack no-lead package	12 mm	8 mm	13 in.	3000

Figure 7. UFQFPN32 - reel diagram

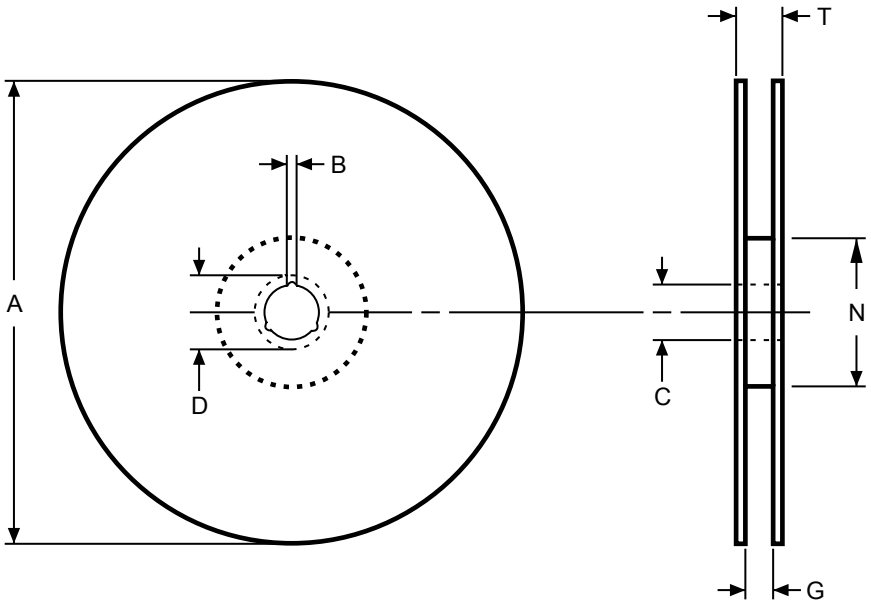
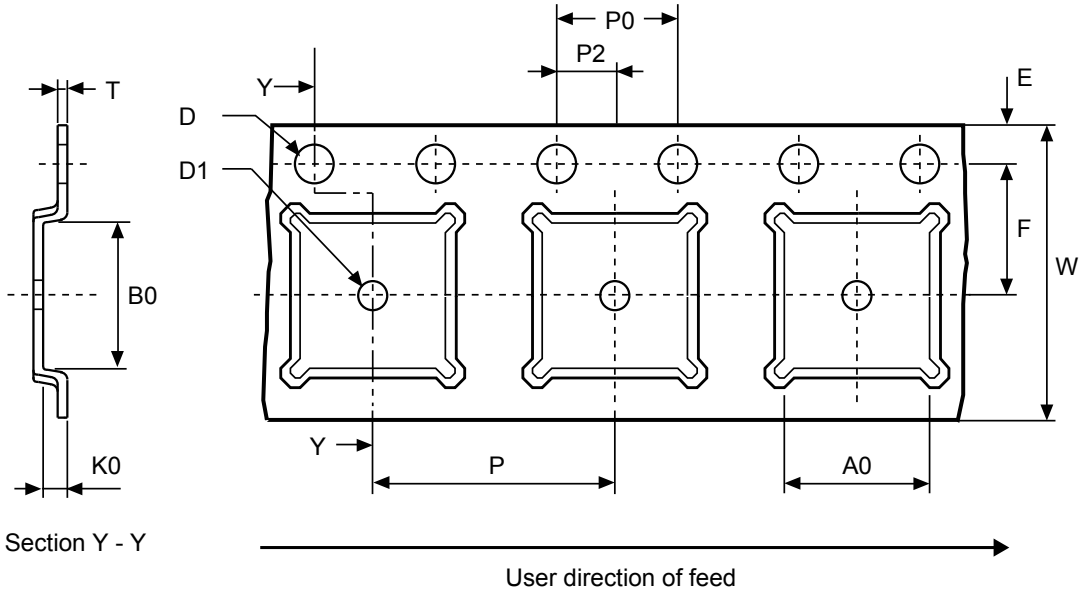


Table 4. UFQFPN32 - reel dimensions

Reel size	Tape width	A Max.	B Min.	C	D Min.	G Max.	N Min.	T Max.	Unit
13”	16	330	1.5	13 ±0.2	20.2	16.4 +2/–0	100	22.4	mm
	12					12.6		18.4	

Figure 8. UFQFPN32 - Embossed carrier tape



1. *Drawing is not to scale.*

Figure 9. UFQFPN32 - Chip orientation in the embossed carrier tape

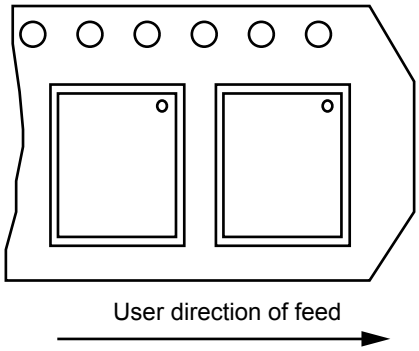


Table 5. UFQFPN32 - Carrier tape dimensions

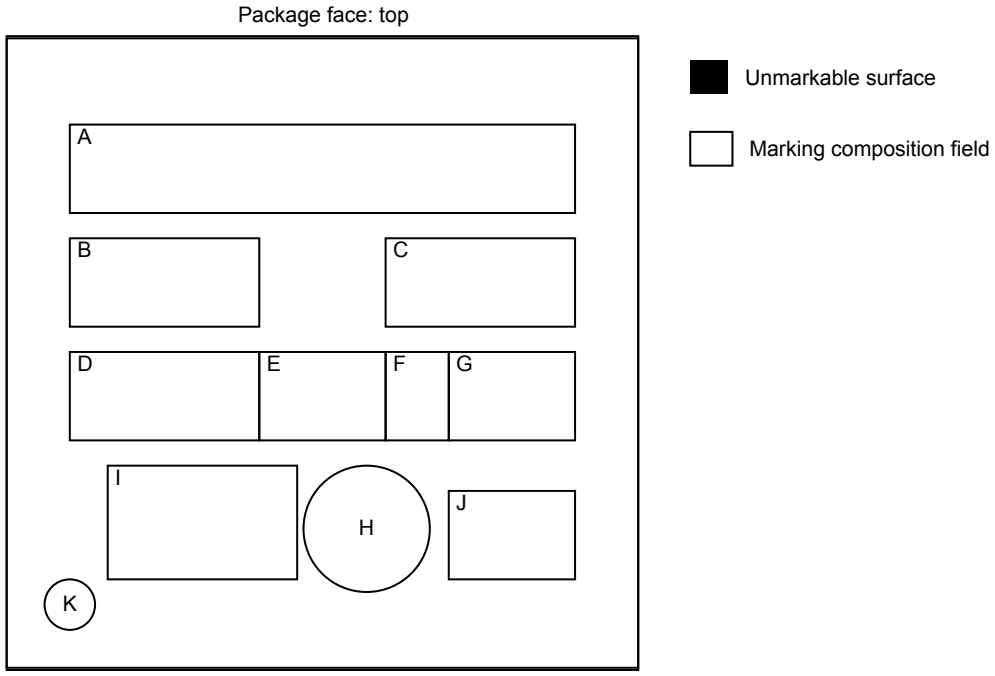
Package	A0	B0	K0	D1 Min.	P	P2	D	P0	E	F	W	T Max.	Unit
UFQFPN 5×5	5.3 ±0.1	5.3 ±0.1	0.75 ±0.1	1.5	8 ±0.1	2 ±0.05	1.55 ±0.05	4 ±0.1	1.75 ±0.1	5.5 ±0.1	12 ±0.3	0.3 ±0.05	mm

6 Package marking information

6.1 UFQFPN32 package marking information

Parts marked as E or ES (for engineering sample) are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Figure 10. UFQFPN32 standard marking example



Legend:

A: Marking area – 8 digits

B: Marking area – 3 digits

C: BE sequence (LLL)

D: Country of origin (3 characters allowed (max.))

E: Assembly plant (PP)

F: Assembly year (Y)

G: Assembly week (WW)

H: Second level interconnect

I: Standard STMicroelectronics logo

J: Diffusion traceability plant (WX)

K: Dot(1)

1. *The dot on the back side indicates the pin 1 location.*

7 Ordering information

Table 6. **Ordering information**

Ordering code	Package	Profil type	Factory firmware version	Supported interfaces
STSAFV10QI3WBTE1	UFQFPN32 WF	0	10.02	I²C or SPI
STSAFV10QI3WBTE2	UFQFPN32 WF	0	10.257	

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
21-Jul-2023	1	Initial release.
29-Sep-2023	2	Added: Ordering information Updated: • Section Features • Section Cover image • Section 1 Description • Section 2.1 UFQFPN32 pin and signal description – Table 1. UFQFPN32 descriptions • Section 3 Electrical integration guidance • Section 3.1 Recommended power supply filtering • Figure 3. Typical hardware implementation for SPI communication (UFQFPN32 package) • Section 5.1 UFQFPN32 - tape and reel delivery packing

Glossary

AES Advanced encryption standard

CA Certification Authority

CC Common Criteria

DRBG Deterministic random bit generator

EC Elliptic curve

ECC Elliptic curve cryptography

ECDAA Elliptic curve direct anonymous attestation (algorithm)

ECDSA Elliptic curve digital signature algorithm

EK Endorsement key

ESD Electrostatic discharge

GPIO General purpose input/output

HBM Human body model

HMAC Hash-based message authentication code or keyed-hash message authentication code

I²C Inter-integrated circuit

NIST National Institute of Standards and Technology

NV Nonvolatile

PKCS Public key cryptographic standards

RNG Random number generator

RSA Public-key cryptosystem (created by Ron Rivest, Adi Shamir and Leonard Adleman)

RSAES Rivest Shamir Adelman encryption/decryption scheme

RSASSA Rivest Shamir Adelman signature scheme with appendix

SHA Secure Hash algorithm

SPI Serial peripheral interface

TCG Trusted Computing Group®

TRNG True random number generator

WPC Wireless power consortium

X.509 X.509 is a standard format for public key certificates.

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