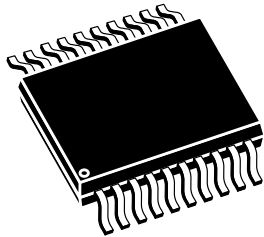


Automotive authentication device for Qi charging with I²C interface



TSSOP20 6.5 × 4.4 mm



Product status link

[STSAFE-V110](#)

Features

- AEC-Q100 qualified 

Authentication features

- I²C support at up to 200 kHz
- Qi WPC1.3 wireless charging compliant
- Asymmetric cryptography :
 - Elliptic curve digital signature algorithm (ECDSA) with SHA-256 for digital signature generation and verification
 - Secure Storage Subsystem

Hardware features

- Arm® SecurCore® SC300™ 32-bit RISC core
- Highly reliable Flash memory technology:
 - 500 000 cycles on the full temperature range
 - 25 years lifetime at 85 °C
 - 20 years lifetime at 105 °C
- Automotive grade 2: -40 °C to 105 °C
- ESD (electrostatic discharge) protection against voltages greater than 4 kV (HBM)
- 1.8 V, 3.3 V or 5 V supply voltage range
- 20-lead thin shrink small outline ECOPACK MSL1 package

Security features

- Active shield and environmental sensors
- Monitoring of environmental parameters (power and clock)
- Hardware and software protection against fault injection
- FIPS compliant RNG built on an SP800-90A compliant SHA256 DRBG and an AIS-31 Class PTG2 compliant true random number generator (TRNG)

Product compliance

- Common Criteria certifications:
 - EAL 4+

1 Description

The **STSAFE-V110** is a cost-effective and high-performance automotive authentication product targeting automotive Qi charging systems.

In the dedicated Qi WPC 1.3 wireless charging process, the **STSAFE-V110** authentication service provides proof to a receiver that it is connected to a recognized transmitter.

Following Qi WPC1.3 specification, the authentication is based on a challenge/response principle.

The **STSAFE-V110** service implements the ECDSA signature scheme with SHA-256 for digital signature generation.

It is compliant with the Qi WPC 1.3 specification.

1.1 Security certifications

This product targets EAL4+ CC certification.

1.2 Hardware features

The **STSAFE-V110** is based on a smartcard-class secure MCU that incorporates the most recent generation of Arm® processors for embedded secure systems. Its SecurCore® SC300™ 32-bit RISC core is built on the Cortex®-M3 core with additional security features to help to protect against advanced forms of attack.

The **STSAFE-V110** offers an I²C interface.

The product features hardware accelerators for advanced cryptographic functions. The AES peripheral provides a secure AES (Advanced Encryption Standard) algorithm implementation, while the NESCRYPT cryptoprocessor efficiently supports public-key algorithms.

The **STSAFE-V110** comes in the TSSOP20 ECOPACK-compliant package. ECOPACK is an ST trademark.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

arm



2 Pin and signal descriptions

The figure below gives the pinout of the TSSOP20 package in which the devices are delivered. Table 1 describes the associated signals.

Figure 1. TSSOP20 pinout (top view)

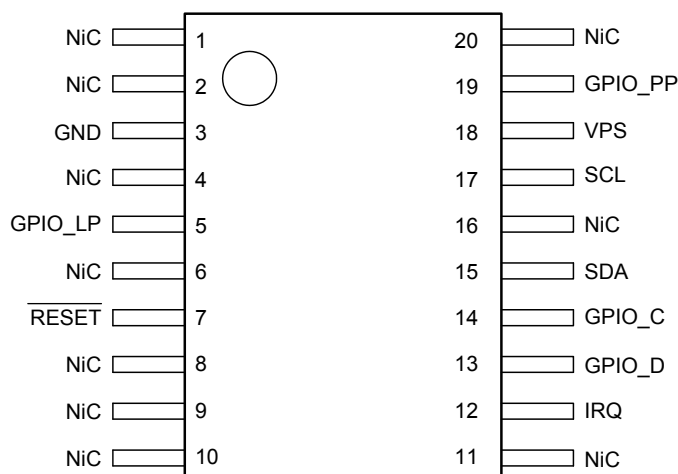


Table 1. Pin descriptions

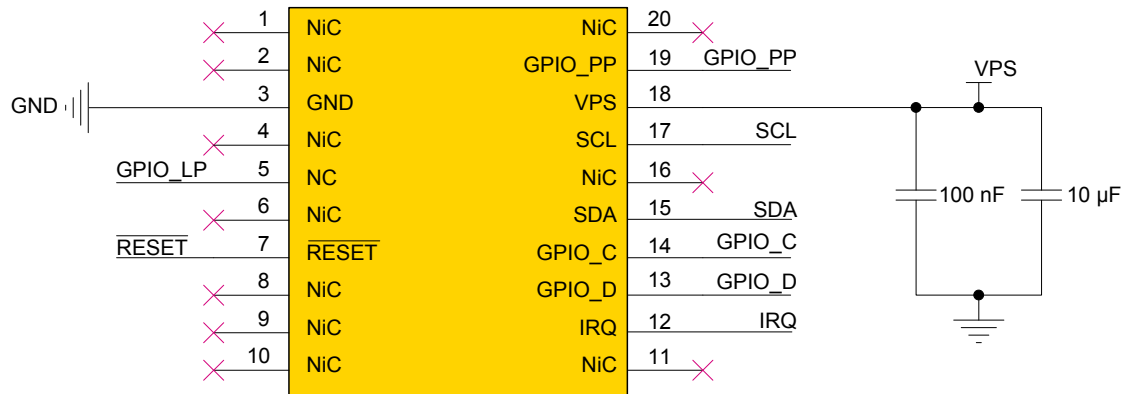
| Signal | Type | Description |
|---------|------------------|---|
| VPS | Input | Power supply. This pin must be connected to 1.8 V or 3.3 V DC power rail supplied by the motherboard. |
| GND | Input | GND has to be connected to the main motherboard ground. |
| SDA | Bidir | I ² C serial data (open drain with no weak pull-up resistor) |
| SCL | Input | I ² C serial clock (open drain with no weak pull-up resistor) |
| IRQ | Output | IRQ used by the device to generate an interrupt |
| RESET | Input | Reset used to re-initialize the device |
| GPIO_C | Input/ output | General-purpose input/output. Defaults to low. The GPIO function is modified by activating GPIO mapped with NVM storage indices feature. |
| GPIO_D | Input/ output | General-purpose input/output. Defaults to low. The GPIO function is modified by activating GPIO mapped with NVM storage indices feature. |
| GPIO_PP | Input | Physical Presence , active high, internal pull-down. Used to indicate physical presence to the device. The GPIO function is modified by activating GPIO mapped with NVM storage indices feature. |
| GPIO_LP | Input | By default, this signal is used for activating and deactivating Standby mode (not found). The GPIO function is modified by activating GPIOs mapped on the NVM storage index feature. |
| NiC | - | Not internally connected: not connected to the die. May be left unconnected, but has no impact on the device if connected. |

3 Integration guidance

3.1 Typical hardware implementation

The physical presence (PP) pin must be connected if the platform implementation (at boot level) uses a hardware physical presence function.

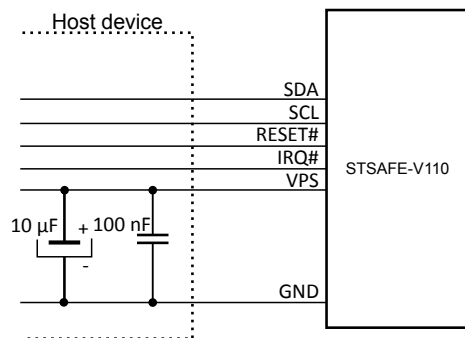
Figure 2. Typical hardware implementation (TSSOP20 package)



3.2 Power supply filtering

The power supply of the circuit must be filtered using the circuit shown in the figure below.

Figure 3. Mandatory filtering capacitors on V_{PS}



1. The capacitor values of 10 µF and 100 nF are recommended values. The minimum required capacitor value is 2.1 µF (2 µF in parallel with 100 nF).

Table 2. Maximum V_{PS} rising slope

| Symbol | Parameter | Value | Unit |
|------------------|--------------------------------------|-------|------|
| S _{VPS} | Maximum V _{PS} rising slope | 5 | V/µs |

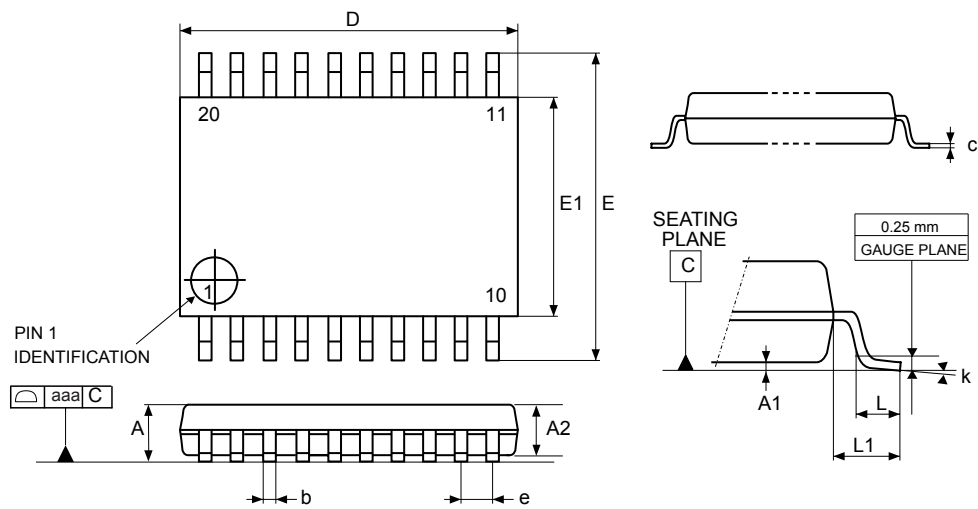
4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TSSOP20 package information

TSSOP20 is a 20-lead thin shrink small outline, 6.5 × 4.4 mm, 0.65 mm pitch package.

Figure 4. TSSOP20 – package outline



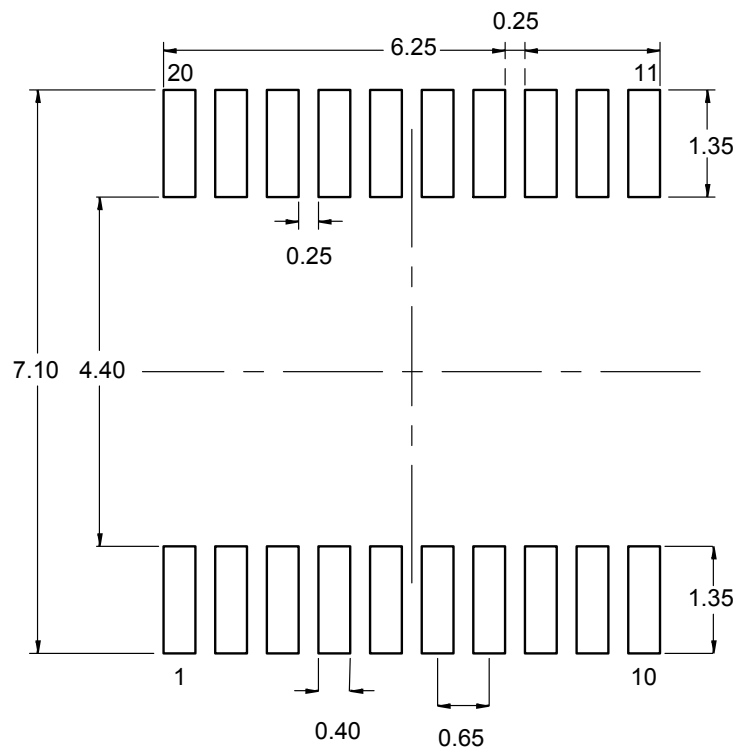
1. Drawing is not to scale.

Table 3. TSSOP20 – package mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|-------------------|-------------|-------|-------|-----------------------|--------|--------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | - | - | 1.200 | - | - | 0.0472 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 0.800 | 1.000 | 1.050 | 0.0315 | 0.0394 | 0.0413 |
| b | 0.190 | - | 0.300 | 0.0075 | - | 0.0118 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D ⁽²⁾ | 6.400 | 6.500 | 6.600 | 0.2520 | 0.2559 | 0.2598 |
| E | 6.200 | 6.400 | 6.600 | 0.2441 | 0.2520 | 0.2598 |
| E1 ⁽³⁾ | 4.300 | 4.400 | 4.500 | 0.1693 | 0.1732 | 0.1772 |
| e | - | 0.650 | - | - | 0.0256 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | - | 8° | 0° | - | 8° |
| aaa | - | - | 0.100 | - | - | 0.0039 |

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

Figure 5. TSSOP20 – package footprint



1. Dimensions are expressed in millimeters.

4.2 Delivery packing

Surface-mount packages can be supplied with tape and reel packing. The reels have a 13" typical diameter. They contain 2500 devices each.

Reels are in plastic, either anti-static or conductive, with a black conductive cavity tape. The cover tape is transparent anti-static or conductive.

The devices are positioned in the cavities with the identifying pin (normally Pin "1") on the same side as the sprocket holes in the tape.

The STMicroelectronics tape & reel specifications are compliant to the EIA 481-A standard specification.

Table 4. Packages on tape and reel

| Package | Description | Tape width | Tape pitch | Reel diameter | Quantity per reel |
|---------------------|-----------------------------------|------------|------------|---------------|-------------------|
| TSSOP20 4.4 mm body | Thin shrink small outline package | 16 mm | 12 mm | 13 in. | 2500 |

Figure 6. Reel diagram

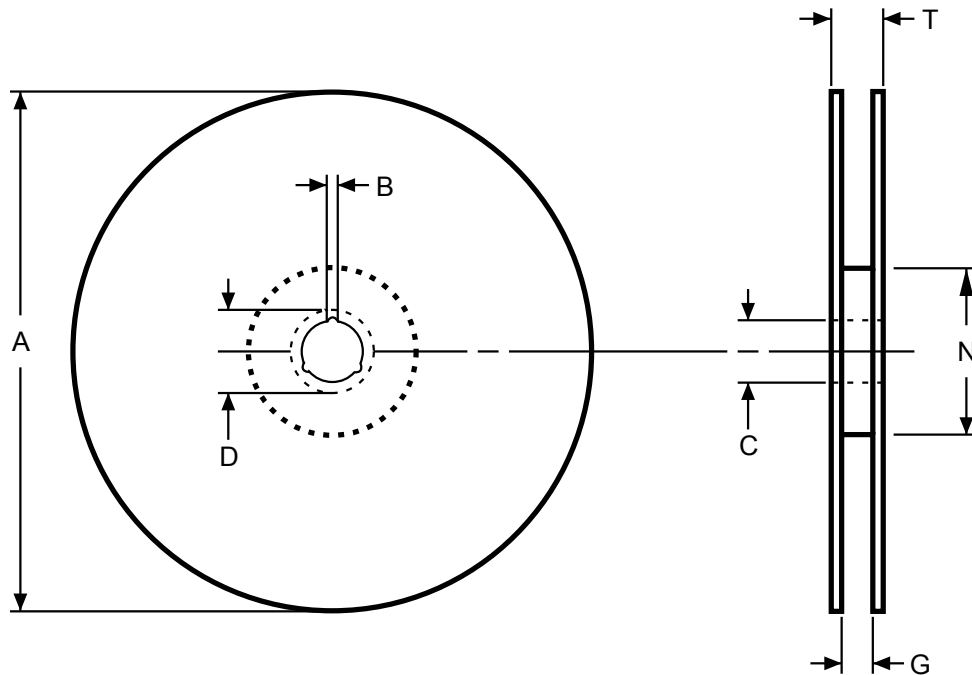
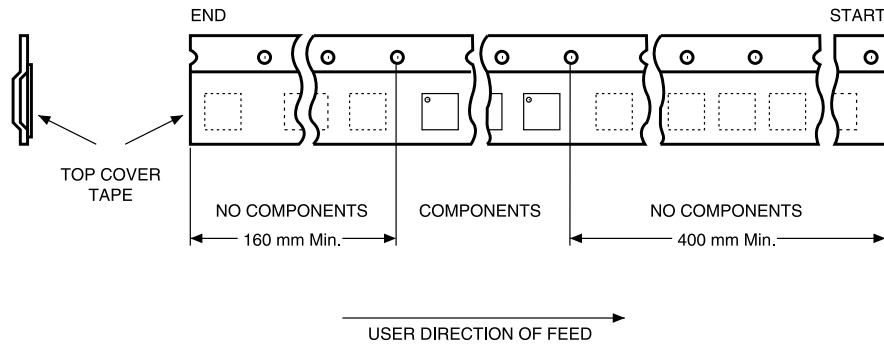
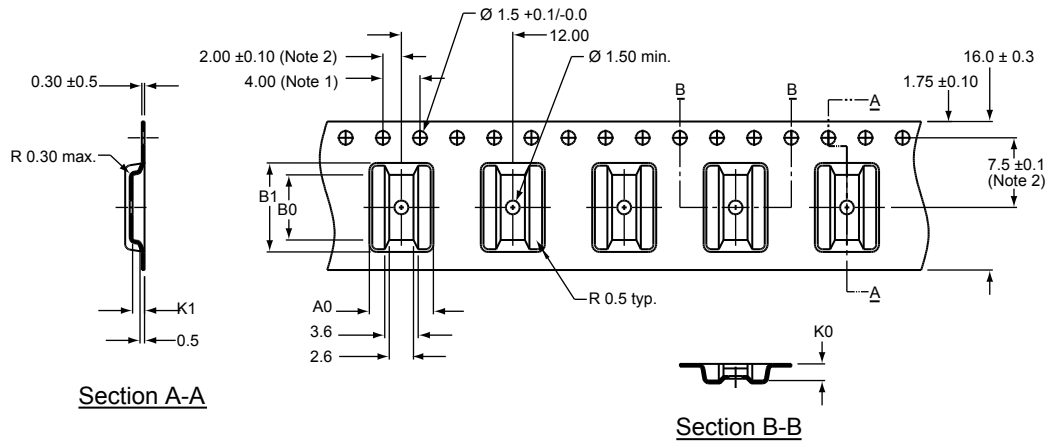


Table 5. Reel dimensions

| Reel size | Tape width | A Max. | B Min. | C | D Min. | G Max. | N Min. | T Max. | Unit |
|-----------|------------|--------|--------|----------|--------|---------|--------|---------|------|
| 13" | 16 | 330 | 0.9 | 13 ±0.25 | 21.5 | 17 ±0.3 | 100 | 19.4 ±1 | mm |

Figure 7. Leader and trailer

Figure 8. Embossed carrier tape for the TSSOP20 package


1. Cumulative tolerance of the 10 sprocket hole pitches = ± 0.2 .
2. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
3. $A0$ and $B0$ are calculated on a plane at a distance "R" above the bottom of the pocket.
4. Drawing is not to scale.
5. Unless otherwise specified, dimensions are in millimeters and decimal values of the form $x.x$ are with ± 0.2 tolerance whereas values of the form $x.xx$ are with ± 0.10 tolerance.

Table 6. Carrier tape dimensions for TSSOP20 package

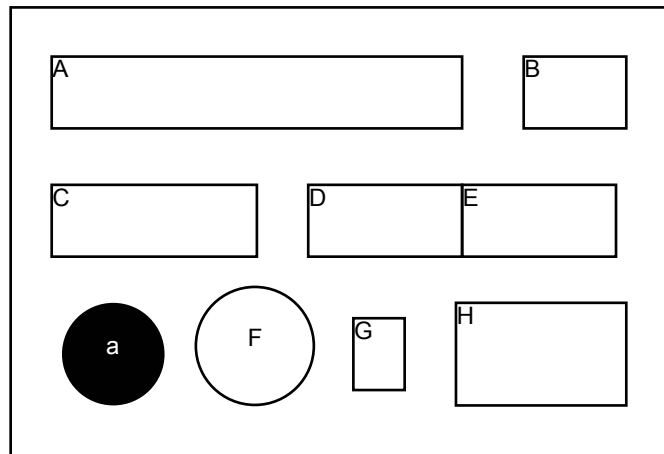
| Package | A0 | B0 | B1 | K0 | K1 | Unit |
|---------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|
| TSSOP20 4.4 mm body | 6.90 ± 0.10 | 7.00 ± 0.10 | 9.60 ± 0.10 | 1.80 ± 0.10 | 1.30 ± 0.10 | mm |

5 Package marking information

Parts marked as E or ES (for engineering sample) are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

The figure below illustrates the typical markings of the device's TSSOP20 package.

Figure 9. TSSOP20 package standard marking example



- Marking composition field
- Unmarkable surface

Caption:

a: Pin 1 reference

A: Marking area: STSAFE-V110

B: Assembly week (ww)

C: Marking area: AE6

D: Backend sequence (LLL)

E: Country of origin (3 characters)

F: ECOPACK level

G: Assembly year (Y)

H: Standard ST logo

Appendix A Terms and abbreviations

Table 7. List of abbreviations

| Term | Description |
|------------------|--|
| AES | Advanced encryption standard |
| AFL | Applicative Flash memory loader |
| CA | Certification authority |
| CC | Common criteria |
| DRBG | Deterministic random bit generator |
| EC | Elliptic curve |
| ECDA | Elliptic curve direct anonymous attestation (algorithm) |
| ECDH | Elliptic curve Diffie–Hellman |
| EGT | Extra guard time |
| FIPS | Federal information processing standards |
| GPIO | General purpose input/output |
| HMAC | Hash-based message authentication code or keyed-hash message authentication code |
| I ² C | Inter-integrated circuit |
| IC | Integrated circuit |
| NVM | Non-volatile memory |
| RSA | Ron Rivest, Adi Shamir and Leonard Adleman Public-key cryptosystem |
| RTR | Root of trust for reporting |
| SHA | Secure Hash algorithm |
| TCG | The Trusted Computing Group® |
| TRNG | True random number generator |

Appendix B Referenced documents

The following materials are to be used in conjunction with this document, or are referenced in it.

[AN2639] Application note, Soldering recommendations and package information for Lead-free ECOPACK® microcontrollers, STMicroelectronics

Revision history

Table 8. Document revision history

| Date | Version | Changes |
|-------------|---------|------------------|
| 14-Jun-2021 | 1 | Initial release. |

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