

## Firmware for the 99.3% efficiency, 2 kW, 3-channel interleaved totem-pole PFC with resonant ZVS digital control

Application	3-channel interleaved totem-pole ZVS-PFC	
Middleware	D-Power FW package	
Hardware Abstraction	Hardware Abstraction Layer API	Board Support Package
Hardware	STM32G474QET6	
Hardware	STEVAL-TTPPFC01	

### Features

- Zero voltage switching (ZVS) control algorithm for power factor correction (PFC)
- Hysteresis cycle-by-cycle current mode control
- Variable switching frequency
- Three-channel interleaved control with phase shedding
- Output DC bus regulation with input voltage and load feedforwards
- Soft startup, inrush current limiter function, and burst mode operation at light load
- Overcurrent, overvoltage, and overtemperature protections
- Based on the [STM32G474QET6](#) Arm Cortex-M4 MCU and [STM32CubeMX](#) architecture

Product summary	
Firmware for the 2 kW 3-channel interleaved totem-pole PFC with resonant ZVS digital control	<a href="#">STSW-TTPPFC01</a>
2 kW 3-channel interleaved totem-pole PFC with resonant ZVS digital control	<a href="#">STEVAL-TTPPFC01</a>
Mainstream Arm® Cortex® - M4 MCU (512 Kbytes of flash memory, Math Accelerator, HR Timer, High Analog level integration)	<a href="#">STM32G474QET6</a>
Applications	Server & Telecom Power/TV PSU/PFC Converter - Single Phase Input/Digital Power

### Description

The [STSW-TTPPFC01](#) provides a highly sophisticated control for the [STEVAL-TTPPFC01](#) 3-channel interleaved bridgeless totem-pole PFC with resonant ZVS digital control, to boost the conversion efficiency.

The [STSW-TTPPFC01](#) is fully implemented in the [STM32G474QET6](#). It includes: a slow outer voltage loop for the output voltage regulation, a faster inner current loop for the inductor currents control, and an input rectification function for the mains synchronization.

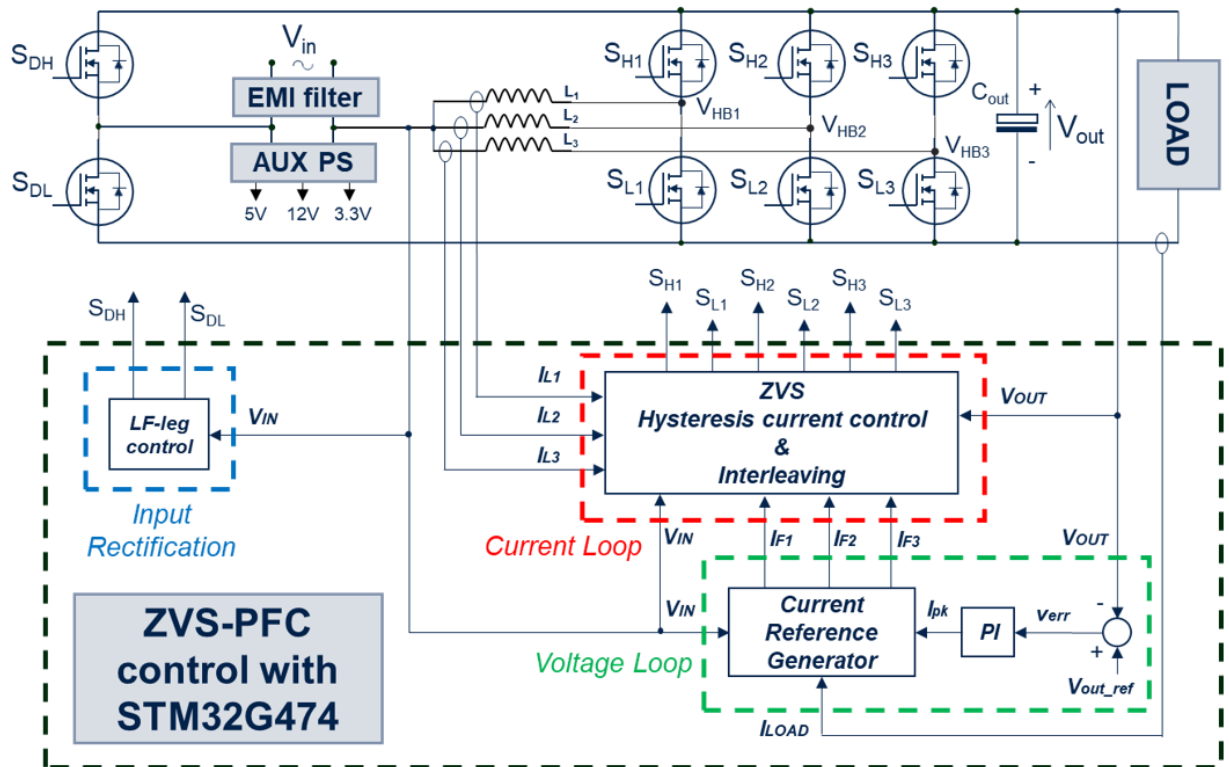
The sophisticated and high performance inner current loop is a hysteresis current control implemented through internal DACs, fast comparators, and the powerful HRTIM peripheral of the [STM32G474QET6](#). Thus, the highest possible bandwidth and cycle-by-cycle regulation are ensured.

The outer voltage loop is performed through a digital PI controller with a fast input and load feedforward. It enhances the PFC dynamic response if a load step or an input voltage variation occurs.

# 1 Block diagram

The following figure shows a detailed block diagram of the ZVS-PFC control. More in detail, the green dashed rectangle represents the slow outer voltage loop for the output voltage regulation, the red dashed rectangle indicates the faster inner current loop for the high-frequency half-bridges control, and the blue dashed rectangle includes the input rectification function of the low-frequency half-bridges.

**Figure 1. Block diagram of the ZVS-PFC control included in the STSW-TTPPFC01**



## Revision history

**Table 1. Document revision history**

Date	Revision	Changes
11-Oct-2022	1	Initial release.
25-Oct-2022	2	Updated document title.

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