# STV0991

## Versatile imaging processor

**Data brief**

10.0 x 10.0 TFBGA
201 balls, 0.65 mm pitch

## Features

- Self-contained, no external memory needed
- Central system
  - ARM® Cortex-R4 CPU @500 MHz
  - 2 Mbytes of SRAM
  - 4 Mbytes of stacked Flash or 16 Mbyte external Flash with update via communication interfaces
  - emulated EEPROM
  - interrupt and DMA controllers
- HDR on-the-fly image signal processing
  - 150 Mpixel/s effective throughput,up to 5 Mpixel and 22 bit front-end processing
  - global tone mapping
  - lens shading correction noise suppression, defective pixel repair, sharpening, adaptive color matrix, multiple scaling engines
  - image statistics engine for AEC/AWB
- Video compression
  - JPEG 8-bit/12-bit, 5/2.1 Mpixel @30 fps
  - H.264 baseline I,P, 2.1 Mpixel @30 fps
- Video analytics accelerators
  - edge data extractor
  - optical flow generator
- Lens distortion (for example fish-eye) correction
- Graphics overlay
- Code protection against hacking
- Multi-camera synchronization support
- Operation with quartz crystal or external clock
- Interfaces
  - Serial (CSI-2) input
  - Parallel video input and output
  - RGMII/GMII, 2x SDIO, 2x SPI, 3x $I^2C$, CAN, 6x LIN, multiple GPIOs with 4x ADC inputs
  - $I^2S$ in, $I^2S$ out, PDM for digital microphone
  - clock output for image sensor
- ASIL-related features
- Low power consumption
- -40 °C to +105 °C operating temperature range ($T_a$)
- AEC-Q100 grade 2 compliance

## Applications

- Automotive: multi-camera systems, stand-alone rear-view smart cameras, video chat, driver monitoring, AVin-to-Ethernet bridge, black-box system
- Security/building management: energy saving, smart sensors, video surveillance IP cameras, intruder alarm detector units, public lighting smart sensor etc.
- Consumer/residential IP cameras, video chat encoding cameras, sports cameras.

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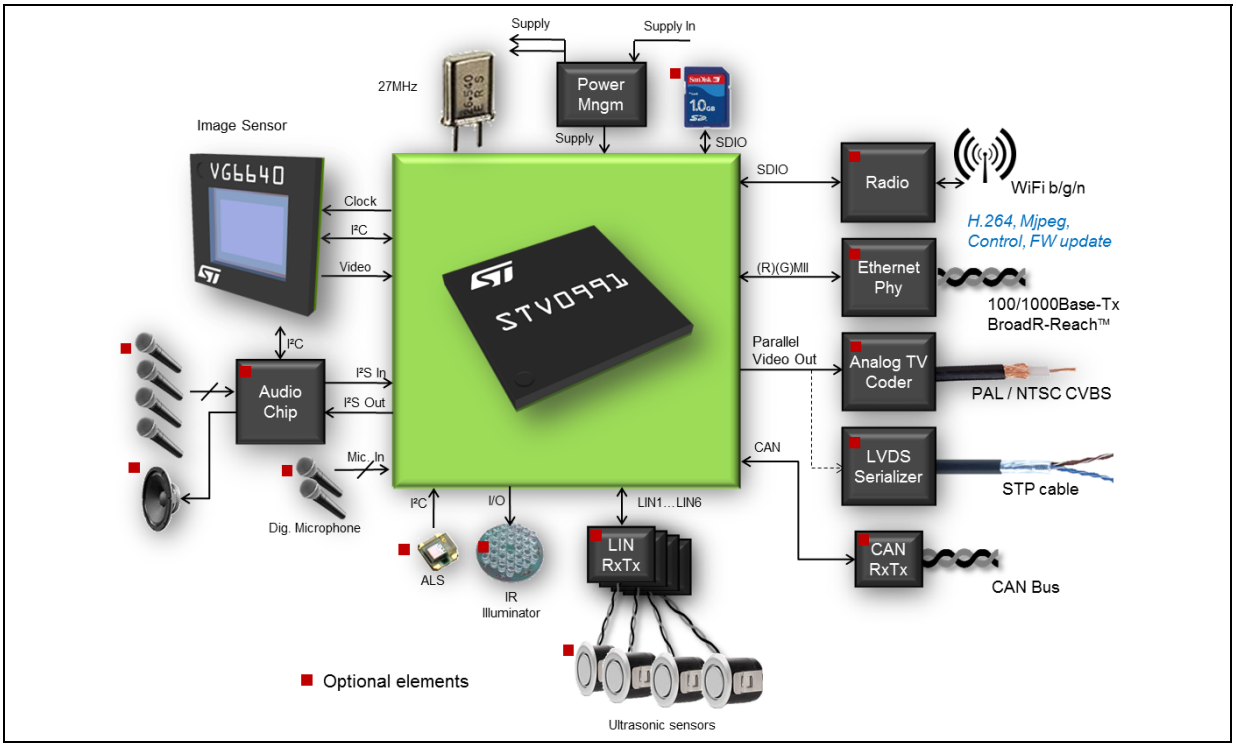
# 1 Description

The STV0991 is a versatile system-on-chip device designed for automotive, security and a multitude of other camera applications. From video and audio input through HDR image signal processing, lens distortion correction, graphics overlay, video compression, video analytics acceleration, CPU, operating and non-volatile memory, media access controller, to video and audio outputs and communication interfaces, it comprises all elements to support compact, low bill-of-material and low energy-consumption camera applications. No external memory chips such as DRAM or Flash are required for its operation, predictive H.264 video encoding inclusive.

Video analytics accelerators unload the central CPU from intensive repetitive tasks. A graphics renderer unit compensates for perceptual distortion produced by wide-angle lenses (such as fish-eye) and inserts graphical and/or textual information over the video. Resulting ready-for-display video can be output as-is over the parallel or serial video output port, or real-time compressed for streaming out through one of: RGMII/GMII, SDIO or SPI interfaces. An audio signal can be input through either an $I^2S$ or a PDM input, processed by the CPU and inserted into the output data stream. A return audio channel is also supported, outputting the audio on an $I^2S$ output. Precise Time Protocol (PTP) support and other provisions on the die allow precise instant-of-exposure synchronization of cameras in a multi-camera system, independent of cable lengths. A cryptographic and hash unit permits protection of customer intellectual property embedded in their software. Flash content can be updated via communication interfaces, thus allowing non-intrusive customer firmware updates. A debug access port (DAP) helps users in their software development process. The application diagram in *Figure 1* suggests some of the applications possible through combining optional elements as required.

**Figure 1. STV0991 application diagram**



# 2 Technical specifications

**Table 1. STV0991 technical specifications**

| Function | Value or Detail |
|---|---|
| CPU | ARM® Cortex™-R4 (ARM® V7 architecture) |
| Clock frequency | 500 MHz maximum |
| Interconnect | High-throughput AXI: 64 bit data bus size at 250 MHz |
| Caches | L1: 32 Kbyte instruction, 32 Kbyte data, L2: 128 Kbyte L2 |
| Interrupt controller | Vectored |
| DMA controller | Multi-channel general-purpose |
| System volatile memory | 2 Mbytes SRAM with programmable allocation and DMA channel |
| Flash (STV0991Fx) | 4 Mbytes serial Flash with 4 data lines |
| EEPROM (STV0991Fx) | Emulated with Flash memory (actual size depends on allocated Flash area, restrictions apply) |
| ISP throughput and resolution | 150 Mpixel/s effective throughput, 5 Mpixel maximum spatial resolution |
| ISP pipe data bit depth | 22 bit image reconstruction, 14-bit processing, 12-bit and 2 x 8-bit outputs |
| ISP scaling capabilities | Up-scaling to 4x max., down-scaling to 16x max., programmable |
| H.264 video compressor | Baseline 4.1, 75 Mpixel/s throughput, 2.1 Mpixel max; I,P; Low latency support |
| JPEG video compressor | Baseline 8 bit / 12 bit; YUV 422/420; Max resolution 5 Mpixel in 8-bit mode and 2.1 Mpixel in 12-bit mode. |
| Video analytics operating resolution | Maximum 640 x 480 pixel, scaled or/and cropped from image sensor resolution |
| Edge extraction method | Gradient maxima search, gradient continuity search with ID labelling |
| Edge extraction ROI number | 6 regions of interest, overlap allowed |
| Edge ext.output data per edge point | Coordinates, Edge ID, DMA channel |
| Feature extraction method | N-cornerness, signature of gradient distribution around the point |
| Number of extracted Feature points | 4k maximum, limited by dedicated feature point buffer sizes |
| Feature point density control | Closed loop varying detection threshold, area-based rejection of lowest cornerness points |
| Optical flow generation method | “difference of signature” in a search region, for subsequent frames |
| Optical flow output data per vector | Origin, tip delta-coordinates and matching distance of best-matched feature. Matching distance of second best-matched feature. |
| Lens distortion correction method | Combination of affine, radial and perspective transforms |
| Amount of lens distortion correction | Horizontal over 100%, Vertical 60% (VGA), 20% (HD), 9% (Full-HD) |
| Graphics Overlay general properties | 290 Mpixel/s throughput, 16 x 16 pixel tile-based rendering |
| Graphics Overlay source properties | 8-bit pixel transparency, true color, YUV or RGB with versatile planarness |
| Graphics Overlay layer properties | Affine, radial and perspective transform, 8-bit transparency |
| Graphics overlay layer number | Up to 7 layers, with independent rendering properties, blended onto an extra layer used for video rendering (lens mapping correction). |
| Serial video input port type | D-PHY/CSI-2 (MIPI) dual-lane |
| Serial video port data depth/speed | 12-bit max./ 1 Gbit/s max. per lane, total 2 Gbit/s max. (input) |

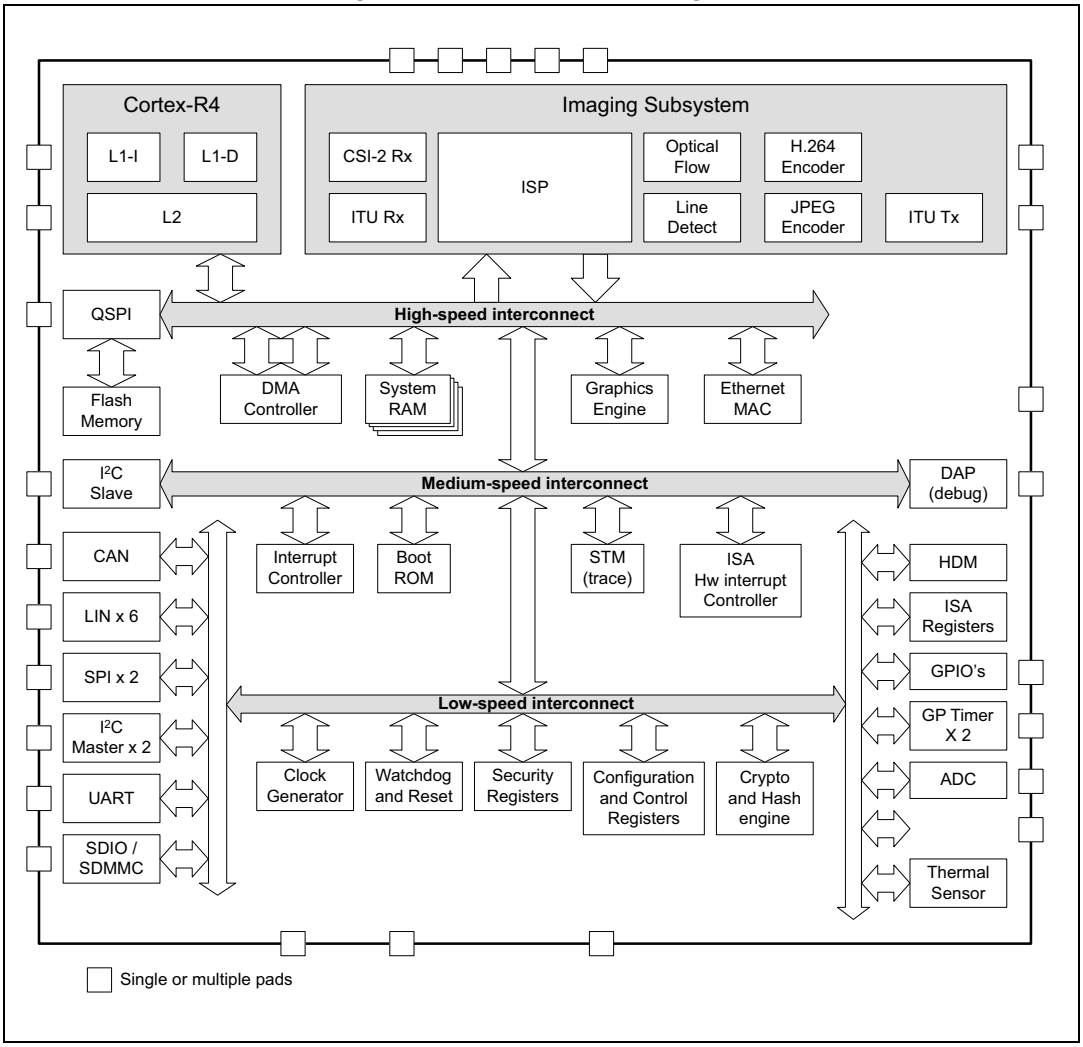
**Table 1. STV0991 technical specifications (continued)**

| Function | Value or Detail |
|---|---|
| Parallel video input port width | 16 data lines max., pixel clock, Hsync, Vsync, embedded sync. support |
| Parallel video input formats | YCbCr on 8/10/12/16 data lines, (incl. BT.601/656), RGB565 and RGB888 on 16 data lines (transparent mode for RGB data) |
| Parallel video output port width | 16 data lines max., Pixel clock, Hsync, Vsync, embedded sync. support |
| Parallel video output formats | YCbCr on 8/10/12/16 data lines (incl. BT.601/656), RGB565 and RGB888 on 16 data lines (transparent mode for RGB data) |
| Parallel video input port clock speed | 120 MHz at 1.8 V, 80 MHz at 3.3 V |
| Parallel video output port clock speed | 120 MHz at 1.8 V, 80 MHz at 3.3 V |
| Ethernet MAC operating modes | Fast Ethernet controller, Gigabit Ethernet controller |
| Ethernet MAC supported interfaces | MII, RMII, GMII, RGMII |
| Ethernet MAC real-time support | IEEE802.1 (AVB), including IEEE802.1AS (PTP) |
| (R)(G)MII operating voltage modes | 1.8 V, 3.3 V |
| $I^2C$ interface operating modes | 1.8 V, 3.3 V, 100 kHz, 400 kHz, 1 MHz, both master (2x) and slave (1x) |
| SPI interface operating modes | 1.8 V, 3.3 V, slave up to 10.4 Mbit/s, master up to 25 Mbit/s, DMA channel, 6 x CS |
| GPIO operating modes | 1.8 V (100 MHz max.), 3.3 V (60 MHz max.); 4 mA drive |
| $I^2S$ interface | 1.8 V, 3.3 V, max. 48 kHz sampling, max. 24-bit sample, TDM supported |
| SD Card interface (SDIO controller) | 3.3 V, Class 6, 48 Mbit/s max., 2 Tbyte max., SD/SDHC/SDXC |
| WiFi radio interface (SDIO controller) | 3.3 V, High-speed and Low-speed support |
| Serial Flash Interface | 1.8 V and 3.3 V modes, max.104 MHz clock, 4 data lines |
| Automotive Safety Integrity Level | Temperature sensor, PEC on some memories, WDT, Sensor status lines extractor and interpreter |
| Supply voltages | 1.1 V for digital processing (required)<br>1.8 V / 3.3 V for I/Os (at least one of the voltage levels required)<br>1.2 V for CSI-2 interfaces (required if CSI-2 used)<br>2.5 V for analog circuitry (required) |
| Operating temperature range (Tj) | -40 °C to +125 °C |
| Storage temperature range (Tstg) | -40 °C to +150 °C |
| Package | TFBGA 10.0 mm x 10.0 mm, 0.65 mm ball pitch, 201 balls |
| External clock frequency range | 6 to 27 MHz, AC or DC coupled |

# 3 Block diagram

*Figure 2* shows the schematic block diagram of the STV0991. Functional blocks are interconnected via high-speed, medium-speed and low-speed buses so as to optimize the device architecture for performance, silicon size and power consumption.

**Figure 2. STV0991 block diagram**



# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 4.1 TFBGA 201 10x10x1.12 package information

**Figure 3. TFBGA 201 10x10x1.12 package outline**

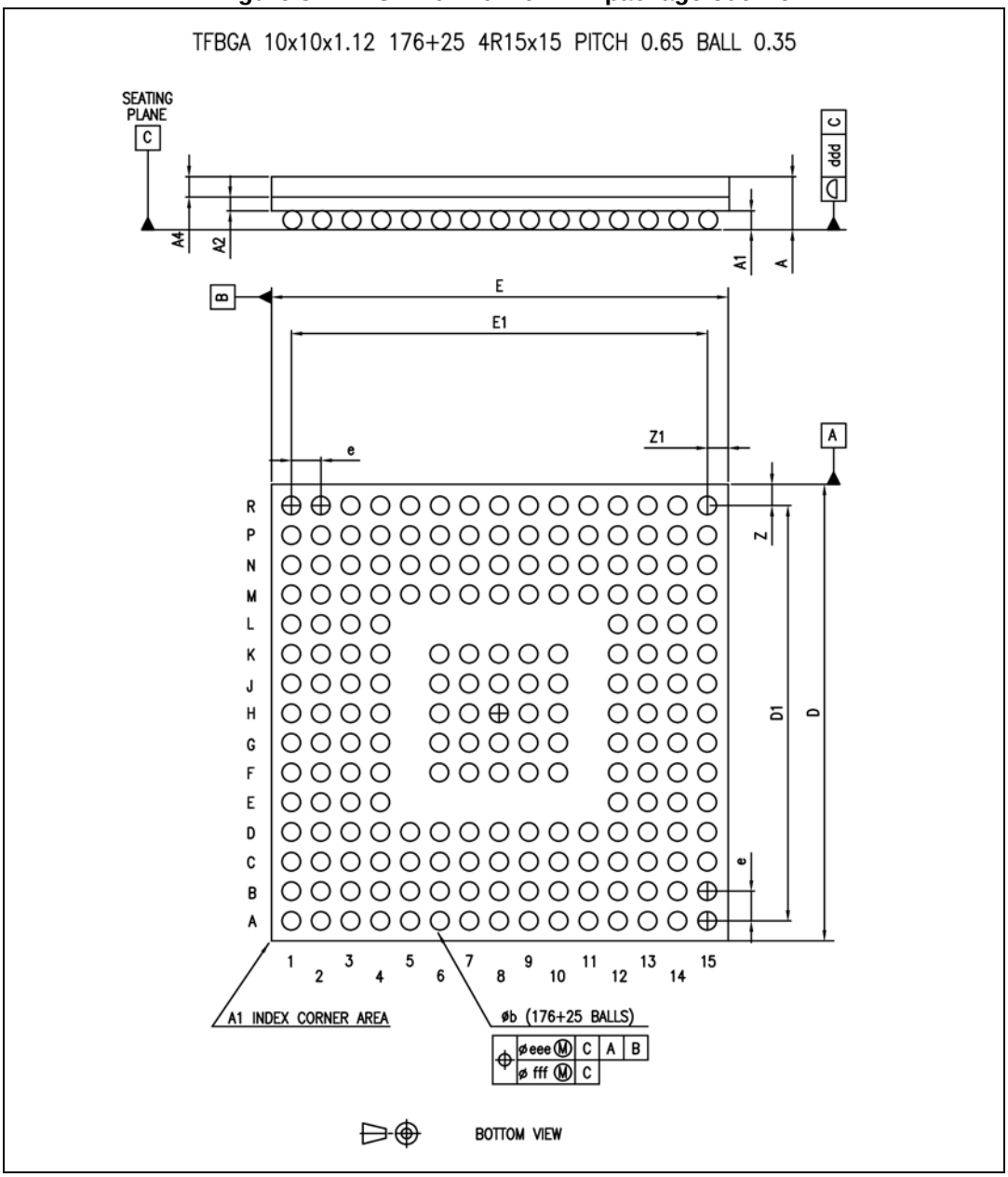


**Table 2. TFBGA201 package dimensions**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches[1] | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A[2] | | | 1.12 | | | 0.0441 |
| A1[3] | 0.22 | 0.27 | 0.32 | 0.0087 | 0.0106 | 0.0126 |
| A2[4] | 0.16 | 0.20 | 0.24 | 0.0063 | 0.0079 | 0.0094 |
| A4[5] | 0.57 | 0.585 | 0.60 | 0.0224 | 0.0230 | 0.0236 |
| b[6] | 0.30 | 0.35 | 0.40 | 0.0118 | 0.0138 | 0.0157 |
| D | 9.95 | 10 | 10.05 | 0.3898 | 0.3937 | 0.3976 |
| D1 | | 9.1 | | | 0.3583 | |
| E | 9.95 | 10.0 | 10.05 | 0.3898 | 0.3937 | 0.3976 |
| E1 | | 9.1 | | | 0.3583 | |
| e[7] | | 0.65 | | | 0.0256 | |
| Z | | 0.45 | | | 0.0177 | |
| Z1 | | 0.45 | | | 0.0177 | |
| ddd | | | 0.10 | | | 0.0039 |
| eee | | | 0.15 | | | 0.0059 |
| fff | | | 0.08 | | | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits
2. Total thickness
3. Stand Off
4. 2ML Substrate
5. Molding
6. Ball size
7. Pitch

# 5 Ordering codes

**Table 3. Ordering codes**

| Part number[1] | Description |
|---|---|
| STV0991FAH | 4 Mbyte Flash, automotive, tray |
| STV0991FAH/TR | 4 Mbyte Flash, automotive, tape & reel |

1. All versions are in 10.0 x 10.0 TFBGA package

# 6 Revision history

**Table 4. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 17-Jul-2012 | 1 | Initial release. |
| 09-Oct-2012 | 2 | Spatial resolution modified, text edits |
| 01-Aug-2013 | 3 | Update of ordering codes, removal of redundant information, update of some parameters |
| 25-Nov2013 | 4 | Alignment with Datasheet v05 |
| 04-Feb-2014 | 5 | Correct typo error (STV0991N instead of STV0991G)<br>Add ECOPACK® section<br>Modify section ordering, Revision history et the end of the data-brief |
| 07-Mar-2014 | 6 | Update<br>– *Table 1*<br>Add:<br>– *Table 1*, *Table 3*, *Table 4* |
| 07-Oct-2015 | 7 | Alignment with data-sheet rev 7.0<br>Typo corrections<br>Improved descriptions and added storage temperature in technical specifications table<br>Added package outline and mechanical data<br>Modified sections ordering |
| 26-Feb-2016 | 8 | Removed previous *Table 1: Device summary* from cover page.<br>Corrected *Table 2: TFBGA201 package dimensions*<br>Added 4 Mbyte Flash to:<br>– cover page features<br>– *Table 1: STV0991 technical specifications*<br>Added STV0991FAH(/TR) to:<br>– *Table 1: Device summary*<br>– *Table 3: Ordering codes*<br>Added STV0991FAH to *Table 4: Feature set differences* |
| 04-Oct-2018 | 9 | Updated *Features* in cover page.<br>Updated *Table 1: STV0991 technical specifications*.<br>Minor text changes |