

Rad-hard 16-bit transceiver, 1.8 V to 3.3 V bidirectional level shifter



Ceramic Flat-48

The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package

Features

- Dual supply bidirectional level shifter
- Voltage range from 1.6 V to 3.6 V
- Separated enable pin for 3-state output
- Internal 26 Ω limiting resistor on each I/O
- Bus hold
- Fail safe
- Cold spare
- Hermetic package
- 300 k/rad (Si) at any Mil1019 dose rate
- SEL immune to 110 MeV.cm²/mg LET ions
- QML-V qualification on-going

Description

The 54VCXH163245 is a rad-hard advanced high-speed CMOS, Schmitt trigger, 16-bit bidirectional, multi-purpose transceiver with 3-state outputs and cold sparing.

Designed to be used as an interface between a 3.3 V bus and a 1.8 V bus in mixed 3.3 V/1.8 V supply systems, it achieves high-speed operations while maintaining the CMOS low power dissipation.

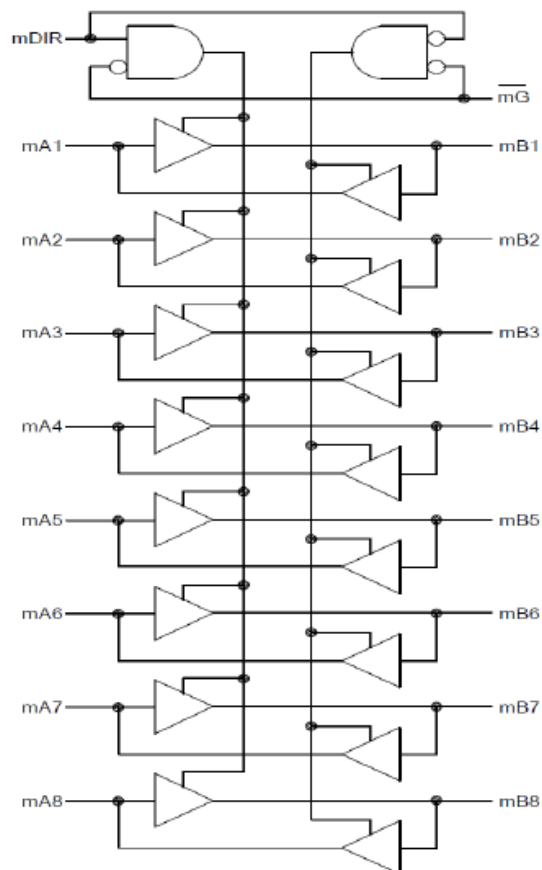
All pins have cold spare buffers to change them to high impedance when V_{DD} is tied to ground.

This IC is intended for a two-way asynchronous communication between data buses. The direction of data transmission is determined by the nDIR inputs.

Product status link

[54VCXH163245](#)

1 Functional description

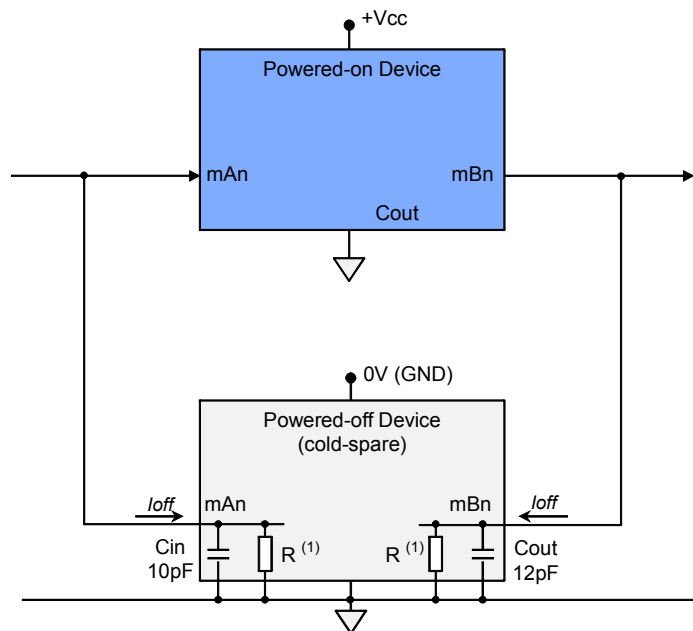
Figure 1. Logic diagram

Table 1. Truth table

Inputs		Function		Outputs	Comments
m G	mDIR	Bus A	Bus B		
L	L	Output	Input	A = B	H = high-voltage level
L	H	Input	Output	B = A	L = low-voltage level
H	X	Z	Z	Z	Z = high impedance X = irrelevant or don't care

1.1 Cold spare

The 54VCXH163245 features a cold spare input and output buffer. In high reliability applications, cold sparing enables a redundant device to be tied to the data bus with its power supply at 0 V ($V_{CC} = 0$ V) without affecting the bus signals or injecting current from the I/Os to the power supplies. Cold sparing also allows redundant devices that are not powered to be switched on when required only. Power consumption is therefore reduced by switching off the redundant circuit. This has no impact on the application. Cold sparing is achieved by implementing a high impedance between I/Os and V_{CC} . The ESD protection is ensured through a non-conventional dedicated structure. Using cold spare on Bus A and Bus B separately is not allowed. In cold spare, both V_{CCA} and V_{CCB} must be at 0 V.

Figure 2. Cold spare and cold redundancy



1. $R = I_{off}/V_{CC}$

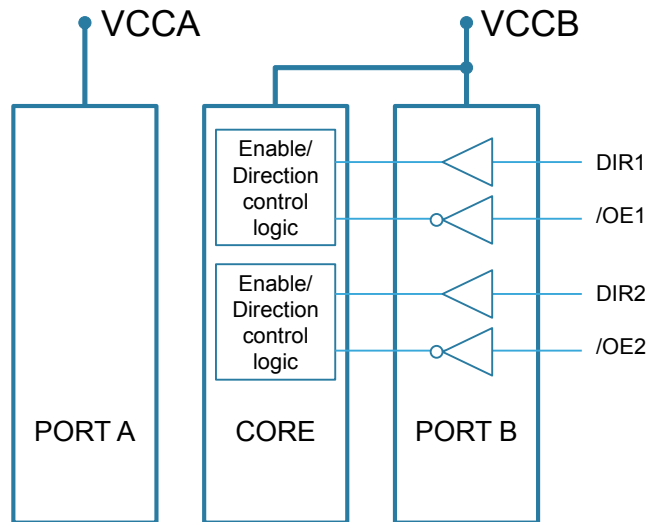
1.2 Power-up

During power-up, all outputs are forced to high impedance. The high impedance state is maintained approximately until V_{CC} is high, thus avoiding any transient and erroneous signals during power-up.

In operating mode:

to guarantee proper operation of the 54VCXH163245 level shifter functionality V_{CCA} has to be above or equal to V_{CCB} .

Figure 3. Power-up



1.3 Pin connections and description

Figure 4. Pin connections

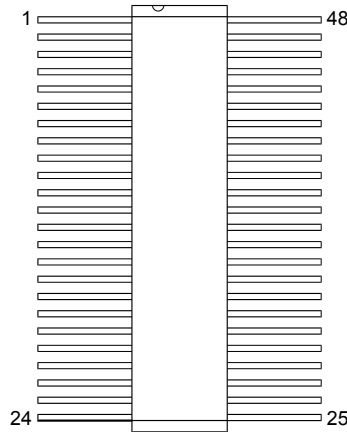


Table 2. Pin description

Device type		All	
Case outline		X	
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1DIR	25	$\overline{2G}$
2	1B1	26	2A8
3	1B2	27	2A7
4	GND	28	GND
5	1B3	29	2A6
6	1B4	30	2A5
7	V _{CCB}	31	V _{CCA}
8	1B5	32	2A4
9	1B6	33	2A3
10	GND	34	GND
11	1B7	35	2A2
12	1B8	36	2A1
13	2B1	37	1A8
14	2B2	38	1A7
15	GND	39	GND
16	2B3	40	1A6
17	2B4	41	1A5
18	V _{CCB}	42	V _{CCA}
19	2B5	43	1A4
20	2B6	44	1A3
21	GND	45	GND
22	2B7	46	1A2

Device type	All		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
23	2B8	47	1A1
24	2DIR	48	$\overline{1G}$

2 Absolute maximum ratings and operating conditions

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Unless otherwise noted, all voltages are referenced to GND. The limits for the parameters specified herein apply over the full specified V_{CC} range and case temperature range of $-55\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (V_{CCA} and V_{CCB}) ⁽¹⁾	-0.5 to 4.6	V
V_{IA}	DC input voltage range port A	-0.5 to 4.6	
V_{IB}	DC input voltage range port B	-0.5 to 4.6	
G/DIR	DC input voltage range G and DIR	-0.5 to 4.6	
V_{OA}	DC output voltage range port A	-0.5 to $V_{CCA} + 0.5\text{ V}$	
V_{OB}	DC output voltage range port B	-0.5 to $V_{CCB} + 0.5\text{ V}$	
I_{IA}	DC input currents port A, anyone input	± 20	mA
I_{IB}	DC input currents port B, anyone input	± 20	
T_{stg}	Storage temperature range	-65 to 150	$^{\circ}\text{C}$
T_L	Lead temperature (10 s)	300	
T_J	Junction temperature range	175	
R_{thjc}	Thermal resistance junction-to-case ⁽²⁾	22	$^{\circ}\text{C}/\text{W}$
ESD	HBM: human body model ⁽³⁾	2	kV

- V_{CCA} must be higher or equal to V_{CCB} . (V_{CCB} higher than V_{CCA} is forbidden).
- Short-circuits can cause excessive heating and destructive dissipation. Values are typical.
- Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 k Ω resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

In Table 4. Operating conditions below, unless otherwise noted, all voltages are referenced to GND.

Table 4. Operating conditions

Symbol	Parameter	Value	Unit
V_{CCA}	Supply voltages ⁽¹⁾	1.4 to 3.6	V
V_{CCB}			
V_I	Input voltage	0 to 3.6	
V_O	Output voltage	0 to V_{CC}	
T_{op}	Operating temperature	-55 to 125	$^{\circ}\text{C}$
d_t/d_v	Input rise and fall time, $V_{CC} = 3\text{ V}$ ⁽²⁾	0 to 10	ns/V

- V_{CCA} must be higher or equal to V_{CCB} . (V_{CCB} higher than V_{CCA} is forbidden).
- Derates system propagation delays by difference in rise time to switch point for t_r or $t_f > 1\text{ ns}/\text{V}$.

3 Electrical characteristics

In Table 5. Electrical characteristics below, $T_{op} = -55\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$, $V_{CC} = 1.4\text{ V}$ to 3.6 V , unless otherwise specified. Each input/output, as applicable, is tested at the specified temperature, for the specified limits. Non-designated output terminals are high level logic, low level logic or open, except for all I_{CC} tests, where the output terminals are open. When performing these tests, the current meter must be placed in the circuit so that all current flows through the meter.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	V_{CCA} (V)	V_{CCB} (V)	Min.	Max.	Unit
V_{IC-}	Negative input clamp voltage	$I_{IN} = -1\text{ mA}$	Open	Open	-1.5	-0.4	V
V_{OH}	High-level output voltage	Bus A output $V_{IN} = V_{IH}(\text{min})$ or $V_{IL}(\text{max})$	$I_{OH} = -100\text{ }\mu\text{A}$	3	2.3	2.8	
			$I_{OH} = -8\text{ mA}$	3	2.3	2.4	
			$I_{OH} = -8\text{ mA}$	3	1.65	2.4	
			$I_{OH} = -6\text{ mA}$	2.3	1.65	1.8	
		Bus B output $V_{IN} = V_{IH}(\text{min})$ or $V_{IL}(\text{max})$	$I_{OH} = -100\text{ }\mu\text{A}$	3	2.3	2.1	
			$I_{OH} = -18\text{ mA}$	3	2.3	1.7	
			$I_{OH} = -6\text{ mA}$	3	1.65	1.25	
			$I_{OH} = -6\text{ mA}$	2.3	1.65	1.25	
V_{OL}	Low-level output voltage	Bus A output $V_{IN} = V_{IH}(\text{min})$ or $V_{IL}(\text{max})$	$I_{OL} = 100\text{ }\mu\text{A}$	3	2.3	0.2	
			$I_{OL} = 8\text{ mA}$	3	2.3	0.55	
			$I_{OL} = 8\text{ mA}$	3	1.65	0.55	
			$I_{OL} = 6\text{ mA}$	2.3	1.65	0.4	
		Bus B output $V_{IN} = V_{IH}(\text{min})$ or $V_{IL}(\text{max})$	$I_{OL} = 100\text{ }\mu\text{A}$	3	2.3	0.2	
			$I_{OL} = 18\text{ mA}$	3	2.3	0.6	
			$I_{OL} = 6\text{ mA}$	3	1.65	0.3	
			$I_{OL} = 6\text{ mA}$	2.3	1.65	0.3	
V_{IH}	High-level input voltage	Bus A	1.8	1.8	$0.65 \times V_{CCA}$		
			2.5	2.5	1.6		
			3.3	3.3	2		
		Bus B	1.8	1.8	$0.65 \times V_{CCB}$		
			2.5	2.5	1.6		
			3.3	3.3	2		

Symbol	Parameter	Test conditions	V _{CCA} (V)	V _{CCB} (V)	Min.	Max.	Unit
V _{IL}	Low-level input voltage	Bus A	1.8	1.8		0.35 x V _{CCA}	V
			2.5	2.5		0.7	
			3.3	3.3		0.8	
		Bus B	1.8	1.8		0.35 x V _{CCA}	
			2.5	2.5		0.7	
			3.3	3.3		0.8	
I _{IH}	Input leakage current high	On nDIR and \overline{G} : For input under test: V _{IN} = V _{CC} For all other inputs: V _{IN} = V _{CC} or GND	3.6	2.7		5	μA
I _{IL}	Input leakage current low	On nDIR and \overline{G} : For input under test: V _{IN} = GND For all other inputs: V _{IN} = V _{CC} or GND	3.6	2.7	-5		
I _{CCH}	Quiescent current, output high	DIR and \overline{G} = V _{CCB} or GND: For Bus A, V _{IN} = V _{CCA} or GND For Bus B, V _{IN} = V _{CCB} or GND	3.6	3.6		20	
I _{CCL}	Quiescent current, output low	DIR and \overline{G} = V _{CCB} or GND: For Bus A, V _{IN} = V _{CCA} or GND For Bus B, V _{IN} = V _{CCB} or GND	3.6	3.6		20	
ΔI _{CC}	Quiescent current delta, TTL input levels	For input under test: V _{IH} = V _{CC} - 0.6 V For all other inputs: V _{IN} = V _{CC} or GND	3.6	3.6		750	
I _{CCZ}	Quiescent current, output three-state	DIR and \overline{G} = V _{CCB} or GND: For Bus A, V _{IN} = V _{CCA} or GND For Bus B, V _{IN} = V _{CCB} or GND	3.6	3.6		20	
I _{OZH}	Three-state output leakage current high	V _{IN} = V _{IH} min. or V _{IL} max, V _{OUT} = V _{CC} or GND	3.6	2.7		5	
I _{OZL}	Three-state output leakage current low	V _{IN} = V _{IH} min. or V _{IL} max, V _{OUT} = V _{CC} or GND	3.6	2.7	-5		
I _{OFF}	Power-off leakage current (cold spare)	DIR and \overline{G} = GND to 3.6 V: For Bus A, V _{IN} = V _{CCA} to 3.6 V For Bus B, V _{IN} = V _{CCB} to 3.6 V	0	0	-10	10	

Symbol	Parameter	Test conditions	V _{CCA} (V)	V _{CCB} (V)	Min.	Max.	Unit	
I _{I(HOLD)}	Input hold current	Bus A	V _{INA} = 0.7 V	2.3	1.65	45		μA
			V _{INA} = 1.6 V	2.3	1.65		-45	
			V _{INA} = 0.8 V	3	1.65	75		
			V _{INA} = 2 V	3	1.65		-75	
			V _{INA} = 0.8 V	3	2.3	75		
			V _{INA} = 2 V	3	2.3		-75	
			V _{INA} 0 to 3.6 V	3.6	2.7		±500	
		Bus B	V _{INB} = 0.57 V	2.3	1.65	25		
			V _{INB} = 1.07 V	2.3	1.65		-25	
			V _{INBv} = 0.57 V	3	1.65	25		
			V _{INB} = 1.07 V	3	1.65		-25	
			V _{INBv} = 0.7 V	3	2.3	45		
			V _{INB} = 1.6 V	3	2.3		-45	
V _{INB} 0 to 2.7 V	3.6		2.7		±500			
C _{IN}	Input capacitance	T _C = 25 °C (1)	GND	GND		10	pF	
C _{OUT}	Output capacitance		GND	GND		12		
C _{PD}	Power dissipation capacitance, 1 MHz		3.3	2.5		20		
—	Functional tests	V _{IN} = V _{IH} min. or V _{IL} max.	3.6 V	1.8 V	L	H	—	
			2.7 V	2.3 V				

Symbol	Parameter	Test conditions	V _{CCA} (V)	V _{CCB} (V)	Min.	Max.	Unit
t _{PHL1} and t _{PLH1}	Propagation delay time mAn to mBn	C _L = 30 pF min., R _L = 500 Ω	2.5	1.8		6	ns
			3.3	1.8		6	
			3.3	2.5		5.5	
t _{PHL2} and t _{PLH2}	Propagation delay time mBn to mAn	C _L = 30 pF min., R _L = 500 Ω	2.5	1.8		7.5	
			3.3	1.8		7	
			3.3	1.8		7	
t _{PZL1}	Propagation delay time, output enable, m \overline{G} to mBn	C _L = 30 pF min., R _L = 500 Ω	2.5	1.8		10	
			3.3	1.8		10	
			3.3	2.5		7	
t _{PZH1}			2.5	1.8		10	
			3.3	1.8		10	
			3.3	2.5		7	
t _{PZL2}	Propagation delay time, output enable, m \overline{G} to mAn	C _L = 30 pF min., R _L = 500 Ω	2.5	1.8		8.5	
			3.3	1.8		8.5	
			3.3	2.5		8	
t _{PZH2}			2.5	1.8		8.5	
			3.3	1.8		8.5	
			3.3	2.5		8	
t _{PLZ1}	Propagation delay time, output disable, m \overline{G} to mBn	C _L = 30 pF min., R _L = 500 Ω	2.5	1.8		6	
			3.3	1.8		6	
			3.3	2.5		5.5	
t _{PHZ1}			2.5	1.8		6	
			3.3	1.8		6	
			3.3	2.5		5.5	
t _{PLZ2}	Propagation delay time, output disable, m \overline{G} to mAn	C _L = 30 pF min., R _L = 500 Ω	2.5	1.8		7.5	
			3.3	1.8		7	
			3.3	2.5		7	
t _{PHZ2}			2.5	1.8		7.5	
			3.3	1.8		7	
			3.3	2.5		7	

1. C_{IN}, C_{OUT}, and C_{PD} are measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} are measured between the designated terminal and GND at a frequency of 1 MHz. This test may be performed at 10 MHz and guaranteed, if not tested, at 1 MHz. The DC bias for the pin under test (V_{BIAS}) = 2.5 V or 3.0 V. For C_{IN}, C_{OUT}, and C_{PD}, all applicable pins are tested on five devices with zero failures. Power dissipation capacitance (C_{PD}) determines both the power consumption (PD) and dynamic current consumption (IS), where: $PD = (C_{PD} + C_L) (V_{CC} \times V_{CC}) f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$, $IS = (C_{PD} + C_L) V_{CC} f + I_{CC} + n \times d \times \Delta I_{CC}$. For both P_D and I_S, n is the number of device inputs at TTL levels, d is the duty cycle of the input signal, f is the frequency of the input signal, and C_L is the external output load capacitance.

4 Radiations

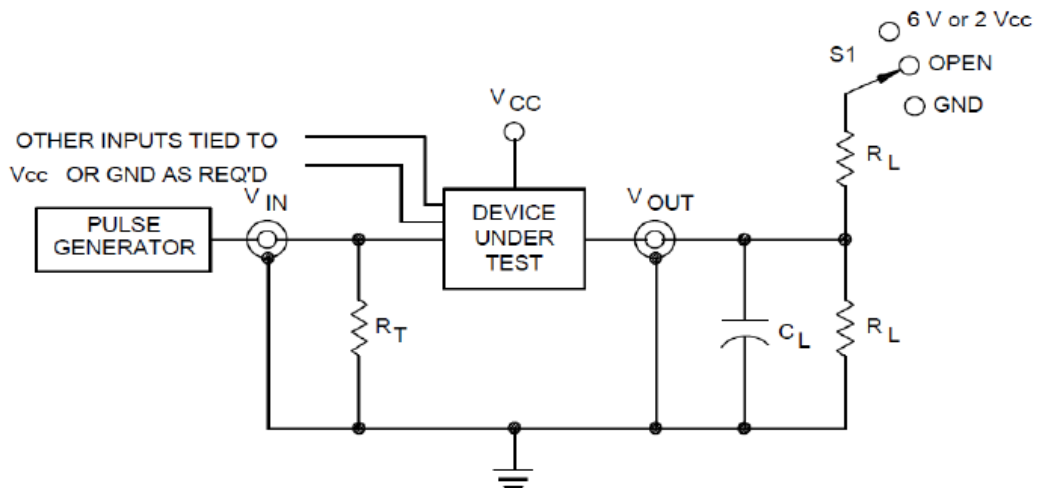
Total dose (Mil1019 dose rate): all parameters are post-irradiation guaranteed by wafer-lot acceptance (after dose, all guaranteed electrical parameters are tested on a sample of units of each wafer lot). All parameters provided in [Table 5. Electrical characteristics](#) apply to both pre- and post-irradiation. The 54VCXH163245 is a pure CMOS product. The irradiation is performed at high dose rates.

Heavy-ions: the behavior of the product when submitted to heavy ions is guaranteed by qualification and is not tested in production. Heavy-ion trials are performed on qualification lots only.

Table 6. Radiations

Type	Features	Value	Unit
TID	Total Ionizing dose, high-dose rate (50 - 300 rad/s) up to:	100	krad
Heavy ions	SEL immune (at 125 °C) up to:	110	MeV.cm ² /mg
	SEU immune up to:	18.5	

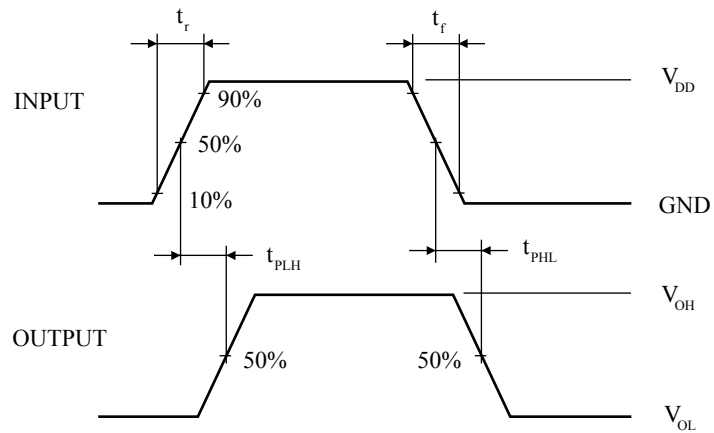
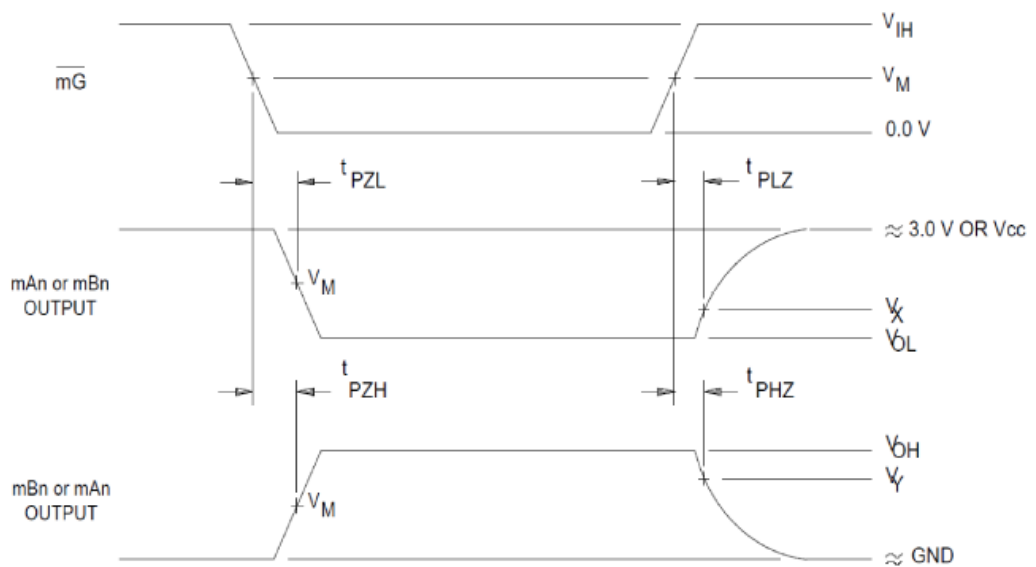
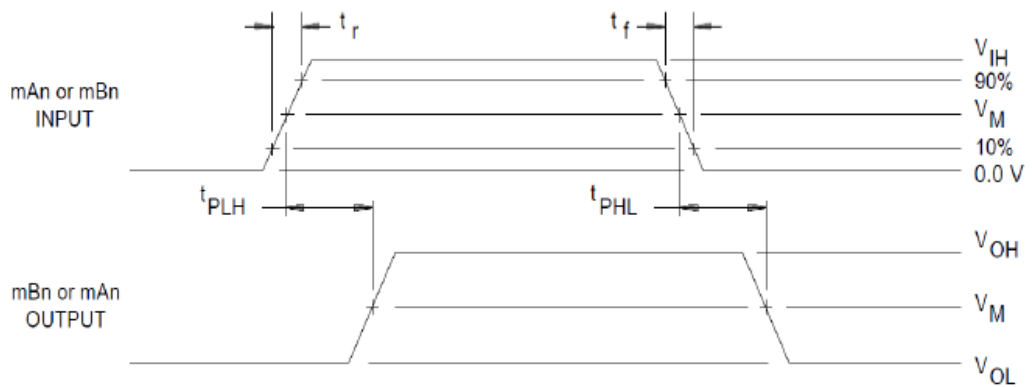
5 Test circuit

Figure 5. Test circuit


1. $C_L = 50$ pF or equivalent (includes jig and probe capacitance), $R_T = Z_{OUT}$ of pulse generator (typically 50Ω), $V_{REF} = 0.5 V_{DD}$. I_{SRC} is set to -1.0 mA and I_{SNK} is set to 1.0 mA for t_{PHL} and t_{PLH} measurements. Input signal from pulse generator: $V_I = 0.0$ V to V_{DD} ; $f = 10$ MHz; $t_r = 1.0$ V/ns ± 0.3 V/ns; $t_f = 1.0$ V/ns ± 0.3 V/ns; t_r and t_f are measured from $0.1 V_{DD}$ to $0.9 V_{DD}$ and from $0.9 V_{DD}$ to $0.1 V_{DD}$ respectively.
2. When measuring t_{PLH} and t_{PHL} : S1 = open
3. When measuring t_{PLZ} and t_{PZL} : S1 = 2VCC for $V_{CC} = 1.8$ V and $V_{CC} = 2.3$ V to 2.7 V; S1 = 6.0 V for $V_{CC} = 3.0$ V to 3.6 V.
4. When measuring t_{PHZ} and t_{PZH} : S1 = GND.
5. The t_{PZL} and t_{PZH} reference waveform is for the output under test with internal conditions set so that the output is low at V_{OL} except when disabled by the output enable control. The t_{PZL} and t_{PZH} reference waveform is for the output under test with internal conditions set so that the output is high at V_{OH} except when disabled by the output enable control.
6. $C_L = 30$ pF minimum or equivalent (includes test jig and probe capacitance)
7. $R_T = 50 \Omega$ or equivalent, $R_L = 500 \Omega$ or equivalent
8. Input signal from pulse generator: $V_{IN} = 0.0$ V to V_{IH} ; PRR = 1 MHz; $Z_O = 50 \Omega$; $t_r = 2.0$ ns; $t_f = 2.0$ ns; t_r and t_f are measured from 10 % of V_{IH} to 90 % of V_{IH} and from 90 % of V_{IH} to 10 % of V_{IH} , respectively; duty cycle = 50 percent.
9. Timing parameters are tested at a minimum input frequency of 1 MHz

Table 7. Voltage points for measurements

Symbol	Parameter	V_{CC}	
		1.8 V, 2.3 V, and 2.7 V	3 V to 3.6 V
V_{IH}	High-level input voltage	V_{CC}	2.7 V
V_M	Middle threshold voltage point	$V_{CC}/2$	1.5 V
V_X	Low threshold voltage point	$V_{OL} + 0.15$ V	$V_{OL} + 0.3$ V
V_Y	High threshold voltage point	$V_{OH} - 0.15$ V	$V_{OH} - 0.3$ V

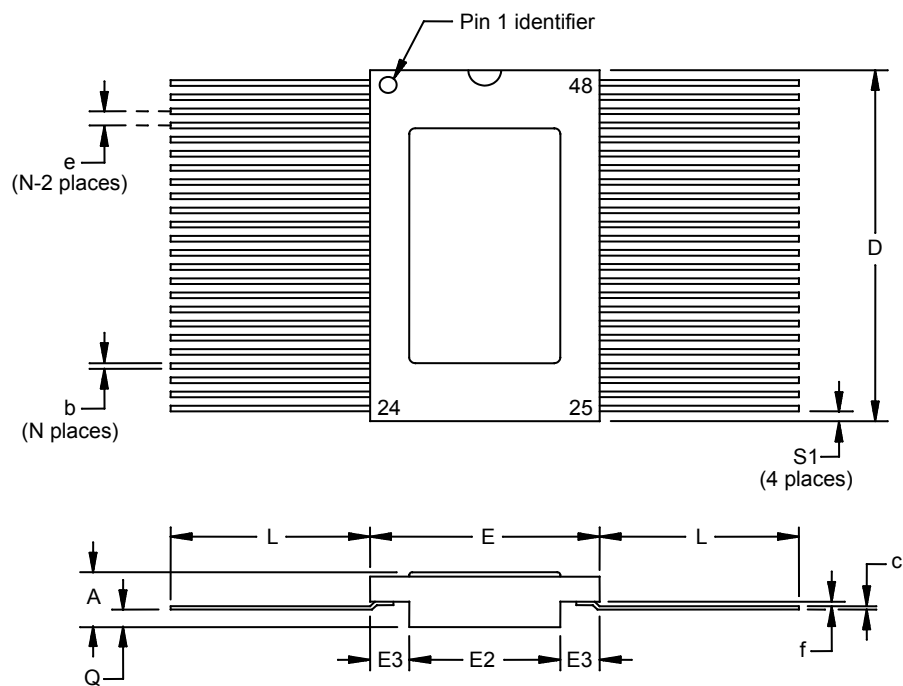
Figure 6. Propagation delay

Figure 7. Enable and disable times

Figure 8. Propagation delay times


6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

6.1 Ceramic Flat-48 package information

Figure 9. Ceramic Flat-48 package outline



The upper metallic lid is neither electrically connected to any pins, nor to the IC die inside the package. Connecting any unused pins or the metal lid to ground or to the power supply does not affect the electrical characteristics.

Table 8. Ceramic Flat-48 mechanical data

Ref.	Dimensions					
	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.18	2.47	2.72	0.086	0.097	0.107
b	0.20	0.254	0.30	0.008	0.010	0.012
c	0.12	0.15	0.18	0.005	0.006	0.007
D	15.57	15.75	15.92	0.613	0.620	0.627
E	9.52	9.65	9.78	0.375	0.380	0.385
E2	6.22	6.35	6.48	0.245	0.250	0.255
E3	1.52	1.65	1.78	0.060	0.065	0.070
e		0.635			0.025	
f		0.20			0.008	
L	6.85	8.38	9.40	0.270	0.330	0.370
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.25	0.43	0.61	0.010	0.017	0.024

7 Ordering information

Table 9. Order code

Order code	SMD ⁽¹⁾	Quality level	Temp. range	Mass	Package	Marking	Packing
RHFXH163245K1	-	Engineering model	-55 to +125 °C	1.50 g	Flat-48	-	Conductive strip pack
RHFXH163245K01V	5962F1120701VXC	QML-V flight				5962F1120701VXC	

1. Standard microcircuit drawing.

Revision history

Table 10. Document revision history

Date	Revision	Changes
27-Jul-2016	1	Initial release
15-Sep-2016	2	Table 4: "Absolute maximum ratings": updated V_{IA} value and added G/DIR parameter. Table 5: "Operating conditions": updated V_I value
29-Sep-2016	3	Section 1.1: "Cold spare": updated text Section 1.2: "Power-up": updated footnotes of Figure 3: "Power-up"
30-Nov-2017	4	Updated Heavy ions value Table 7: "Radiations"
17-Sep-2018	5	Updated Figure 3. Power-up and Section 1.2 Power-up, Section 1.3 Pin connections and description and Section 7 Ordering information. Minor text changes.

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