STV200N55F3
N-channel 55 V, 1.8 mΩ, 200 A, PowerSO-10
STripFET™ Power MOSFET

Features

<table>
<thead>
<tr>
<th>Type</th>
<th>V_{DSS}</th>
<th>R_{D(\text{on})\text{ max}}</th>
<th>I_D^{(1)}</th>
</tr>
</thead>
<tbody>
<tr>
<td>STV200N55F3</td>
<td>55 V</td>
<td>&lt; 2.5 mΩ</td>
<td>200 A</td>
</tr>
</tbody>
</table>

1. Current limited by package

- Conduction losses reduced
- Low profile, very low parasitic inductance

Application

- Switching applications

Description

This n-channel enhancement mode Power MOSFET is the latest refinement of ST’s STripFET™ process. The resulting transistor shows extremely high packing density for low on resistance, rugged avalanche characteristics and low gate charge.

Table 1. Device summary

<table>
<thead>
<tr>
<th>Order code</th>
<th>Marking</th>
<th>Package</th>
<th>Packaging</th>
</tr>
</thead>
<tbody>
<tr>
<td>STV200N55F3</td>
<td>200N55F3</td>
<td>PowerSO-10</td>
<td>Tape and reel</td>
</tr>
</tbody>
</table>

Figure 1. Internal schematic diagram and connection diagram (top view)
Contents

1 Electrical ratings ......................................................... 3

2 Electrical characteristics ............................................. 4
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3 Test circuits .............................................................. 8

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1 Electrical ratings

Table 2. Absolute maximum ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>Drain-source voltage ($v_{gs} = 0$)</td>
<td>55</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Gate-source voltage</td>
<td>± 20</td>
<td>V</td>
</tr>
<tr>
<td>$I_D^{(1)}$</td>
<td>Drain current (continuous) at $T_C = 25 , ^{\circ}C$</td>
<td>200</td>
<td>A</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Drain current (continuous) at $T_C = 100 , ^{\circ}C$</td>
<td>170</td>
<td>A</td>
</tr>
<tr>
<td>$I_{DM}^{(2)}$</td>
<td>Drain current (pulsed)</td>
<td>800</td>
<td>A</td>
</tr>
<tr>
<td>$P_{TOT}^{(3)}$</td>
<td>Total dissipation at $T_C = 25 , ^{\circ}C$</td>
<td>300</td>
<td>W</td>
</tr>
<tr>
<td>$E_{AS}^{(4)}$</td>
<td>Single pulse avalanche energy</td>
<td>1.0</td>
<td>J</td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>Storage temperature</td>
<td>-55 to 175</td>
<td>°C</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Operating junction temperature</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. Current limited by package
2. Pulse width limited by safe operating area
3. This value is rated according to $R_{thj-c}$
4. Starting $T_J = 25 \, ^{\circ}C$, $I_D = 60 \, A$, $V_{DD} = 35 \, V$

Table 3. Thermal data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{thj-case}$</td>
<td>Thermal resistance junction-case max</td>
<td>0.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{thj-pcb}^{(1)}$</td>
<td>Thermal resistance junction-pcb max</td>
<td>50</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

1. When mounted on 1 inch² FR-4 2 oz Cu
2 Electrical characteristics

(T\textsubscript{case} = 25 °C unless otherwise specified)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>$V_{(BR)DSS}$</td>
<td>Drain-source breakdown voltage</td>
<td>$I_D = 250 \mu A, V_{GS}= 0$</td>
<td>55</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{DSS}$</td>
<td>Zero gate voltage drain current ($V_{GS} = 0$)</td>
<td>$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating, } T_c = 125 \degree C$</td>
<td>1</td>
<td>10</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{GS}$</td>
<td>Gate body leakage current ($V_{DS} = 0$)</td>
<td>$V_{DS} = \pm 20 V$</td>
<td>±100</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$V_{GS(th)}$</td>
<td>Gate threshold voltage</td>
<td>$V_{DS} = V_{GS}, I_D = 250 \mu A$</td>
<td>2</td>
<td>4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$R_{DS(on)}$</td>
<td>Static drain-source on resistance</td>
<td>$V_{GS} = 10 V, I_D = 75 A$</td>
<td>1.8</td>
<td>2.5</td>
<td></td>
<td>mΩ</td>
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</table>

Table 5. Dynamic

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{iss}$</td>
<td>Input capacitance</td>
<td>$V_{DS} = 25 V, f = 1 \text{ MHz, } V_{GS}=0$</td>
<td>6800</td>
<td>1450</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$C_{oss}$</td>
<td>Output capacitance</td>
<td></td>
<td></td>
<td></td>
<td>15</td>
<td>pF</td>
</tr>
<tr>
<td>$C_{rss}$</td>
<td>Reverse transfer capacitance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_g$</td>
<td>Total gate charge $V_{DD} = 44 V, I_D = 120 A,$ $V_{GS} = 10 V$</td>
<td></td>
<td>100</td>
<td>30</td>
<td>26</td>
<td>nC</td>
</tr>
<tr>
<td>$Q_{gs}$</td>
<td>Gate-source charge</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_{gd}$</td>
<td>Gate-drain charge</td>
<td></td>
<td></td>
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</table>

Figure 14
### Table 6. Switching times

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>$t_{d(on)}$</td>
<td>Turn-on delay time</td>
<td>$V_{DD} = 27.5\ V$, $I_D = 60\ A$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\ V$, $\text{Figure } 13$</td>
<td>25</td>
<td>150</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Rise time</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{d(off)}$</td>
<td>Turn-off delay time</td>
<td>$V_{DD} = 27.5\ V$, $I_D = 60\ A$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\ V$, $\text{Figure } 13$</td>
<td>110</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_f$</td>
<td>Fall time</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
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</table>

### Table 7. Source drain diode

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{SD}$</td>
<td>Source-drain current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>$I_{SD}^{(1)}$</td>
<td>Source-drain current (pulsed)</td>
<td></td>
<td>200</td>
<td>800</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>$V_{SD}^{(2)}$</td>
<td>Forward on voltage</td>
<td>$I_{SD} = 120\ A$, $V_{GS} = 0$</td>
<td></td>
<td></td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>$t_{rr}$</td>
<td>Reverse recovery time</td>
<td>$I_{SD} = 120\ A$, $dI/dt = 100\ A/\mu s$</td>
<td></td>
<td></td>
<td>60</td>
<td>ns</td>
</tr>
<tr>
<td>$Q_{rr}$</td>
<td>Reverse recovery charge</td>
<td>$V_{DD} = 35\ V$, $T_J = 150\ ^\circ C$, $\text{Figure } 18$</td>
<td></td>
<td></td>
<td>110</td>
<td>nC</td>
</tr>
<tr>
<td>$I_{RRM}$</td>
<td>Reverse recovery current</td>
<td></td>
<td></td>
<td></td>
<td>3.5</td>
<td>A</td>
</tr>
</tbody>
</table>

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 $\mu$s, duty cycle 1.5%
2.1 Electrical characteristics (curves)

Figure 2. Safe operating area
Figure 3. Thermal impedance

Figure 4. Output characteristics
Figure 5. Transfer characteristics

Figure 6. Normalized $B_{VDSS}$ vs temperature
Figure 7. Static drain-source on resistance
Figure 8. Gate charge vs gate-source voltage

\[ V_{GS}(\text{V}) \]
\[ Q_{g} \text{[nC]} \]

- \( V_{GP} = 4 \text{V} \)
- \( I_{D} = 120 \text{mA} \)

Figure 9. Capacitance variations

\[ C_{GS} \text{[pF]} \]

- \( f = 1 \text{MHz} \)
- \( V_{GS} = 0 \text{V} \)

Figure 10. Normalized gate threshold voltage vs temperature

\[ V_{GS} \text{[mV]} \]

\[ T_{J} \text{[°C]} \]

- \( I_{D} = 250 \mu\text{A} \)

Figure 11. Normalized on resistance vs temperature

\[ R_{ON} \text{[mΩ]} \]

\[ T_{J} \text{[°C]} \]

- \( V_{GS} = 10 \text{V} \)
- \( I_{D} = 7.5 \text{A} \)

Figure 12. Source-drain diode forward characteristics

\[ V_{DS} \text{[V]} \]

\[ I_{D} \text{[mA]} \]

- \( T_{J} = -50 \text{°C} \)
- \( 25 \text{°C} \)
- \( 175 \text{°C} \)
3 Test circuits

Figure 13. Switching times test circuit for resistive load

Figure 14. Gate charge test circuit

Figure 15. Test circuit for inductive load switching and diode recovery times

Figure 16. Unclamped inductive load test circuit

Figure 17. Unclamped inductive waveform

Figure 18. Switching time waveform
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.
# PowerSO-10 mechanical data

<table>
<thead>
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<th>Dim</th>
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</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
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<td>A</td>
<td></td>
<td>3.70</td>
<td></td>
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<td>3.60</td>
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<td>9.60</td>
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<td>D1</td>
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<td>7.60</td>
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<td>9.30</td>
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<td>E2</td>
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<td>7.60</td>
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<td>5.90</td>
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<tr>
<td>e</td>
<td>1.27</td>
<td>1.65</td>
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</tr>
<tr>
<td>L</td>
<td>0.95</td>
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<td>&lt;</td>
<td>0°</td>
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[Diagram of PowerSO-10 mechanical data]

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STV200N55F3
# 5 Revision history

Table 8. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
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<td>05-Mar-2008</td>
<td>1</td>
<td>First release.</td>
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<tr>
<td>10-Nov-2008</td>
<td>2</td>
<td>Document status promoted from preliminary to datasheet.</td>
</tr>
<tr>
<td>02-Mar-2009</td>
<td>3</td>
<td>Figure 2 has been updated.</td>
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