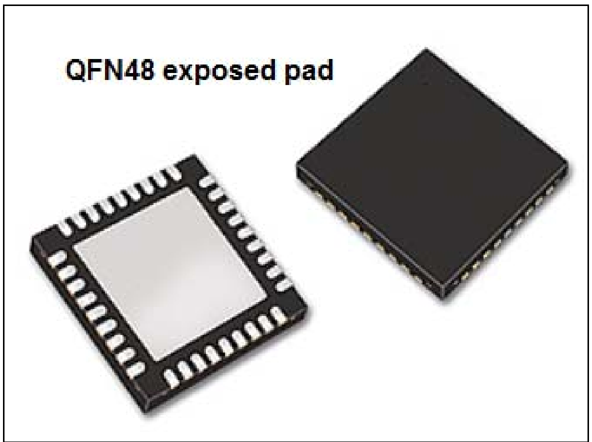
ST-PLC-AFE

Power-line communication, analog front-end

Datasheet - production data



Features

- Integrated, analog power-line driver and receiver
- EN 50065-1 - CENELEC, European bands A, B, C, and D
- Supports FSK, S-FSK, and OFDM
- Supports PRIME, G3, and IEC 61334
- Half-duplex mode
- Thermal protection
- Programmable overcurrent protection
- 10 V p-p single-ended output range
- 20 V p-p differential-ended output range
- Programmable transmitter chain (Tx) and receiver chain (Rx) filters
- Programmable Rx and Tx gain control
- 7 V to 14 V line driver supply
- Low power consumption: 10 mW (receive mode)
- Reverse sensitivity 20 µVrms typical
- Four-wire, serial peripheral interface
- Two integrated zero cross detectors
- Temperature range: -40 °C to 125 °C

Applications

- E-metering
- Smart grid applications
- Smart light control
- Solar energy management
- Building automation
- Remote monitoring and control

Description

The ST-PLC-AFE is a power-line communication, analog front-end device capable of capacitive or transformer-coupled connections to the power line while under the control of a microcontroller or a DSP.

The line driver is able to drive low-impedance lines, requiring up to 1.65 A, into reactive loads. It can also work in differential mode for high performance, as well as single-ended mode for a low-cost bill of materials (BOM). The integrated receiver is able to detect signals down to 20 µVrms. The system works in half-duplex mode.

The AFE is protected against over temperature and short-circuit conditions. It also provides four adjustable current limits through an internal register. Through the four-wire serial peripheral interface, or SPI, each functional block can be enabled or disabled to optimize power consumption.

Contents

1 Package pin description and connections

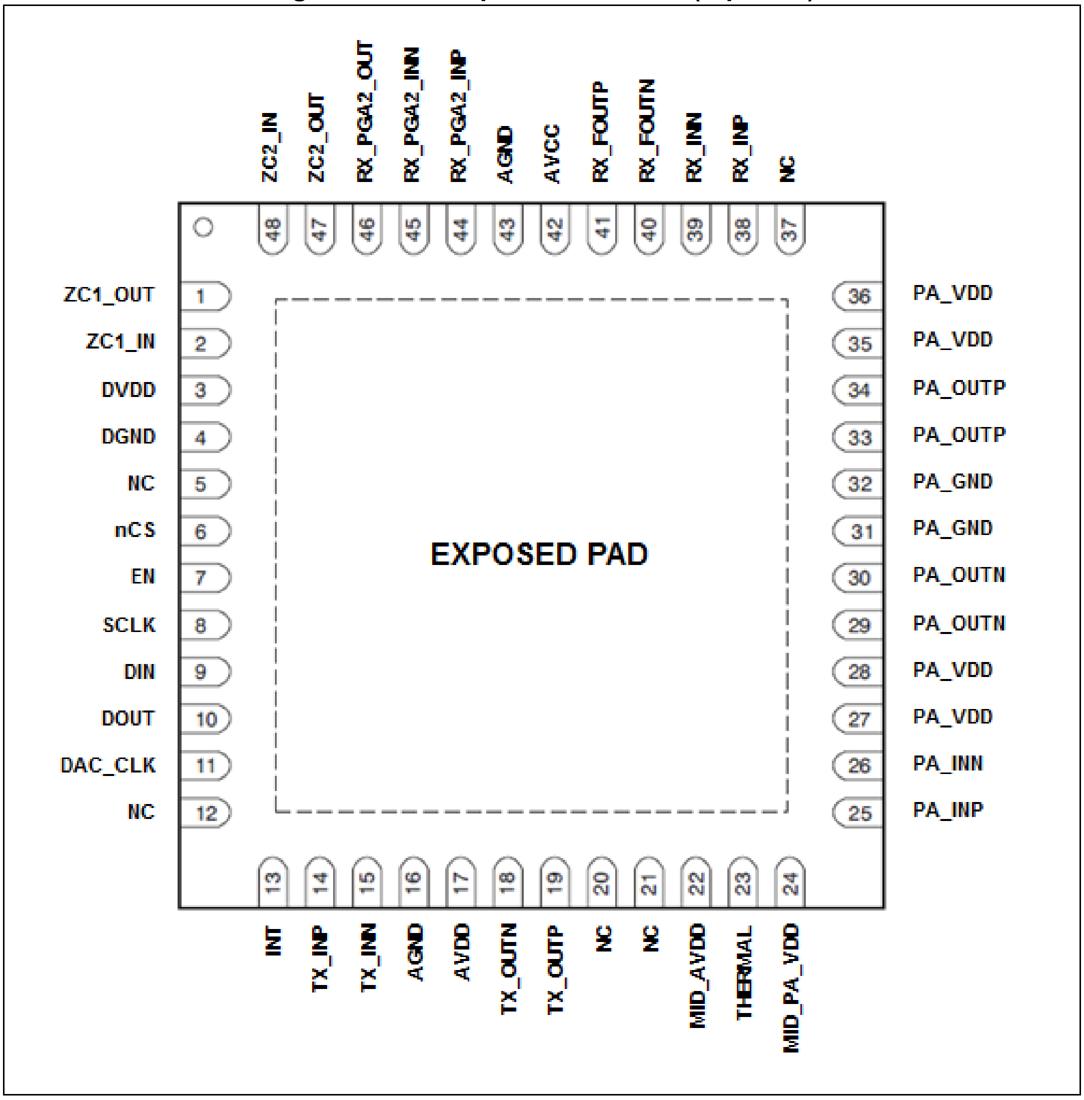
Table 1. QFN48 pin description

Pin no.	Name	Type	Description
1	ZC1_OUT	OUT ANALOG	Zero cross detector 1 output node
2	ZC1_IN	IN ANALOG	Zero cross detector 1 input node
3	DVDD	POWER DIGITAL	Digital positive supply
4	DGND		Digital ground
5	NC1	NC	Not connected to the Silicon
6	nCS	IN DIGITAL	SPI digital select
7	EN		System enable
8	SCLK		SPI serial clock
9	DIN		SPI digital input
10	DOUT	OUT	SPI digital output
11	DAC_CLK	IN DIGITAL	DAC input frequency
12	NC2	NC	Not connected to the Silicon
13	INT	OUT DIGITAL	Interrupt on overcurrent or thermal limit
14	TX_INP	IN ANALOG	DAC output (positive side)
15	TX_INN		DAC output (negative side)
16	AGND	POWER ANALOG	Analog ground
17	AVDD		Analog positive supply
18	TX_OUTN	OUT ANALOG	Tx LPF output (negative side)
19	TX_OUTP		Tx LPF output (positive side)
20	NC3	NC	Not connected to the Silicon
21	NC4		
22	MID_AVDD	OUT ANALOG	Rx common mode voltage, AVDD/2 to be connected to 150 nF capacitor
23	THERMAL		Thermal sensor output voltage, to be connected to an ADC
24	MID_PA_VDD		PA common mode voltage, PA supply voltage divided by 2, to be connected to 10 nF capacitor
25	PA_INP	IN ANALOG	PA non inverting input
26	PA_INN		PA inverting input
27	PA_VDD	POWER PA	Power amplifier positive supply
28	PA_VDD		
29	PA_OUTN	OUT PA	PA output inverting side
30	PA_OUTN		

Table 1. QFN48 pin description (continued)

Pin no.	Name	Type	Description
31	PA_GND	POWER PA	Power amplifier ground
32	PA_GND		
33	PA_OUTP	OUT PA	PA output non inverting side
34	PA_OUTP		
35	PA_VDD	POWER PA	Power amplifier positive supply
36	PA_VDD		
37	NC5	NC	Not connected to the Silicon
38	RX_INP	IN ANALOG	Rx chain input pin, non-inverting input
39	RX_INN		Rx chain input pin, inverting input
40	RX_FOUTN	OUT ANALOG	Rx output after LPF filter, inverting output
41	RX_FOUTP		Rx output after LPF filter, non-inverting output
42	AVDD	POWER ANALOG	Analog positive supply
43	AGND		Analog ground
44	RX_PGA2_INP	IN ANALOG	Rx PGA2 input pin, non-inverting input
45	RX_PGA2_INN		Rx PGA2 input pin, inverting input
46	RX PGA2_OUT	OUT ANALOG	Rx PGA2 output pin, single mode
47	ZC2_OUT		Zero cross detector 2 output node
48	ZC2_IN	IN ANALOG	Zero cross detector 2 input node

Figure 1. QFN48 pin connections (top view)



1. The exposed pad must be connected to ground

2 General description

The ST-PLC-AFE combines a digital-to-analog converter (DAC), an adaptive gain control (AGC), programmable filters, and a line driver on a single chip. The architecture is divided into three primary functional blocks:

- Power amplifier (PA)

The PA is characterized by the following features:

  - Differential or single-ended output architecture
  - 1.65 A drive capability @ 14 Vpp
  - Gain of 6.9 V/V
  - PA current limiter with four programmable limits: 0.5 A, 1 A, 1.5 A, and 2.1 A
  - Integrated thermometer placed closed to the PA

- Transmitter chain (Tx)

The Tx is characterized by the following features:

  - Can work with a 10-bit internal DAC
  - Can be driven with an external DAC through the TX_INP input pin
  - Programmable unity-gain fourth-order low-pass filter, following CENELEC bands A, B, C, and D.
  - PGA with gains of 6 dB, 0 dB, -18 dB, and -36 dB

- Receiver chain (Rx)

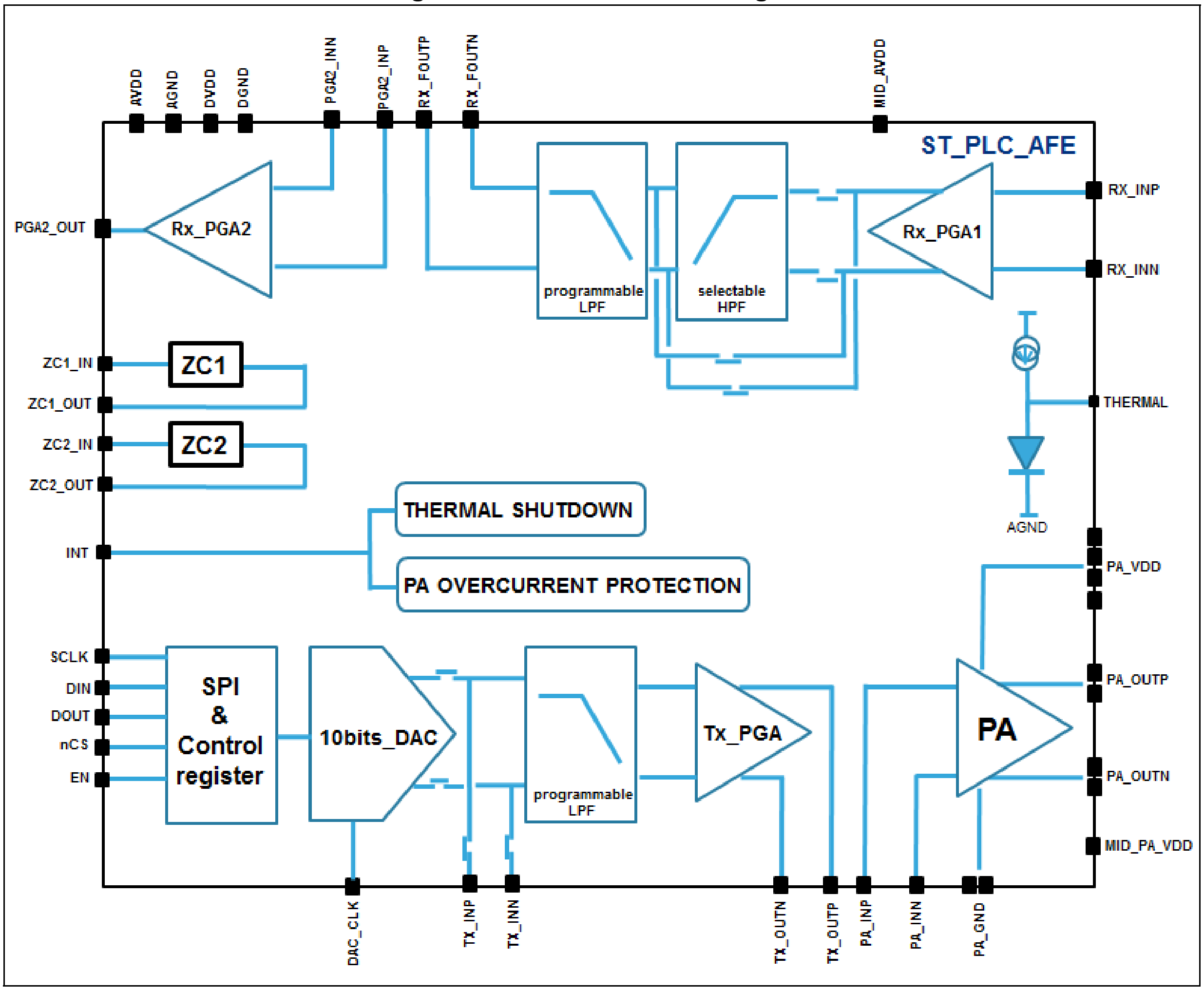
The Rx is characterized by the following features:

  - PGA1 with gains of -3 dB, 3 dB, 9 dB, and 15 dB
  - Sensitivity of 20 µVrms typical
  - Can be connected in differential or single-input mode
  - Programmable unity-gain fourth-order low-pass filter, following CENELEC bands A, B, C, and D.
  - Selectable high-pass filter with a 35 kHz cutoff frequency)
  - PGA2 with gains of -6 dB, 6 dB, 18 dB, and 30 dB

The ST-PLC-AFE supports other circuitry blocks, such as:

- SPI interface for the microcontroller
- Thermal shutdown
- Two zero crossing detectors

Figure 2. Functional block diagram



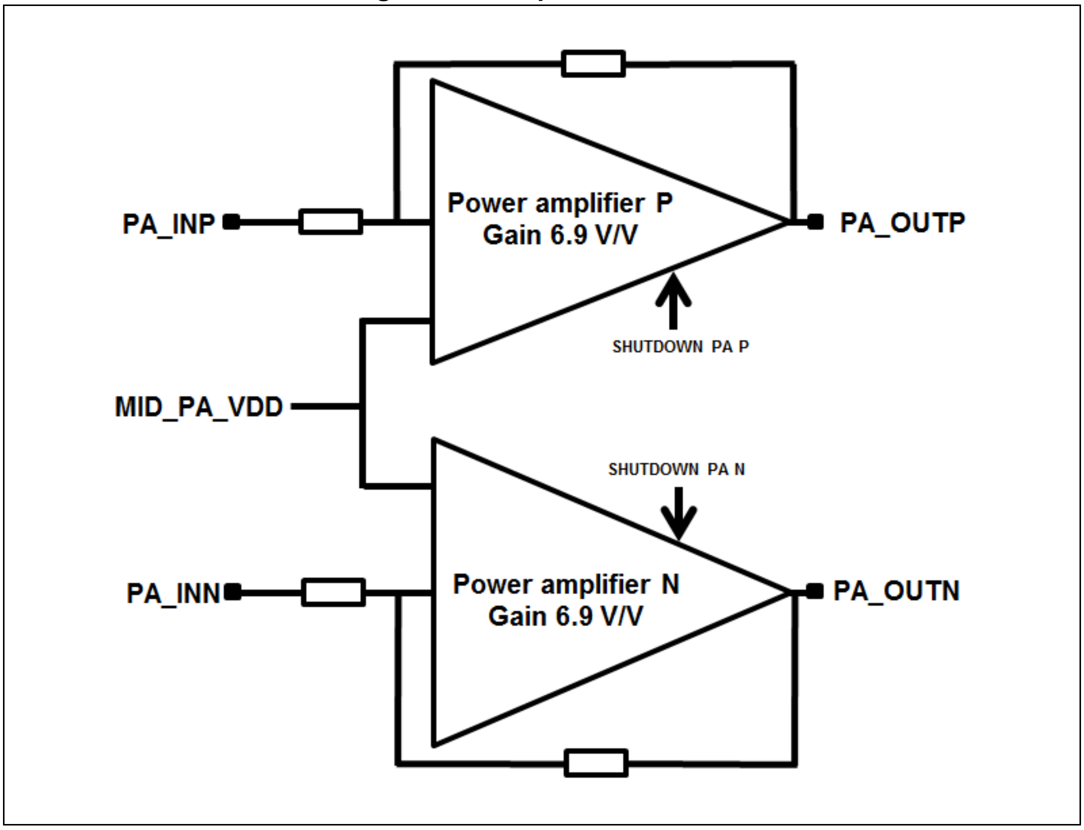
2.1 PA block

The PA block has a low-pass filter response when configured with a gain of 6.9 V/V. The PA is specified to operate from 7 V to 14 V and can deliver up to 1.65 A of continuous output current over the specified junction temperature range of -40 °C to 125 °C.

In differential mode, both PAs are turned on (see *Figure 3*).

In single-ended configuration, the N side of the PA is turned off and its output is placed into high impedance. This is achieved by setting the PA2_EN bit in the Enable register to 0 (see *Figure 3*).

Figure 3. PA equivalent circuit

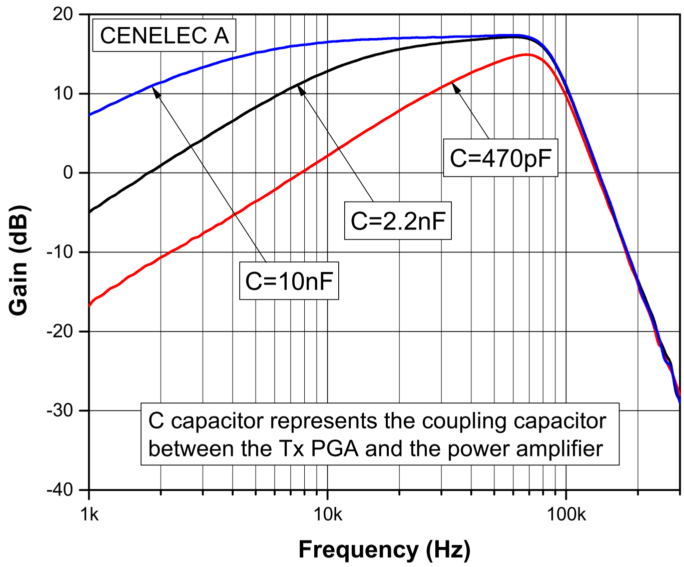


2.1.1 Typical connections to the PA

Connecting the PA in a typical PLC application requires an input AC coupling capacitor, C_IN_PA (see *Figure 5* and *Figure 7*). This capacitor introduces a single-pole, high-pass characteristic to the PA transfer function; combined with the inherent low-pass transfer function, this characteristic results in a pass band response.

Figure 4 shows the impact of this coupling capacitor.

Figure 4. Tx chain with different coupling capacitor



If using CENELEC band A, it is recommended to use a 2.2 nF capacitor. For CENELEC bands B, C, and D, a 1 nF can be used.

2.1.2 Power amplifier power management

When the transmitter is not in use, the outputs can be disabled and placed into a high-impedance state. This is achieved by setting the PA_EN bit in the Enable register to 0. A description of energy consumption following sub-block activation through the internal registers is given in *Section 10.7: ST-PLC-AFE consumption (no load)*.

The PA integrates a current limiter that is programmable by an internal register thanks to the SPI communication. The current limit is set by the CL bits in the Gain register. Four limits are available: 0.5 A, 1 A, 1.5 A, and 2.1 A. See *Section 9.3.1: Overcurrent condition* for overcurrent protection.

2.2 Tx block

The Tx block is divided into an internal DAC, an internal fourth-order filter, a programmable amplifier, and a power liner driver. There are two ways to drive this transmission line:

1. The internal DAC driving mode, achieved through the SPI interface and the internal 10-bit DAC.
2. Using an external driving mode where the signal received by the ST-PLC-AFE is purely analog, coming from an external MCU DAC. This signal is applied on the TX_INP input pin.

Tx PGA can be configured through the SPI to operate as an attenuator or to work in follower. The gain steps of the Tx PGA are 6 dB, 0 dB, -18 dB, and -36 dB. The gain can be programmed through the TX_PGA1<1:0> bits in the Gain register.

The **Tx_filter** is a unity-gain, fourth-order, low-pass filter. Its cutoff frequency is selectable between CENELEC A or CENELEC B, C, or D modes. The selection of the band is achieved through the BAND_SEL bit in the Enable register.

2.2.1 Internal DAC driving mode

The ST-PLC-AFE accepts serial data from the microprocessor and writes the data to the internal DAC registers. Operating in DAC mode results in the lowest distortion signal injected onto the AC mains. DAC mode is selected by setting the DAC_EN bit in the Enable register to 1. *Figure 5* and *Figure 6* show the connection to the power line while using the internal DAC in differential mode and in single-ended mode respectively.

Figure 5. Connection to the power line in differential mode

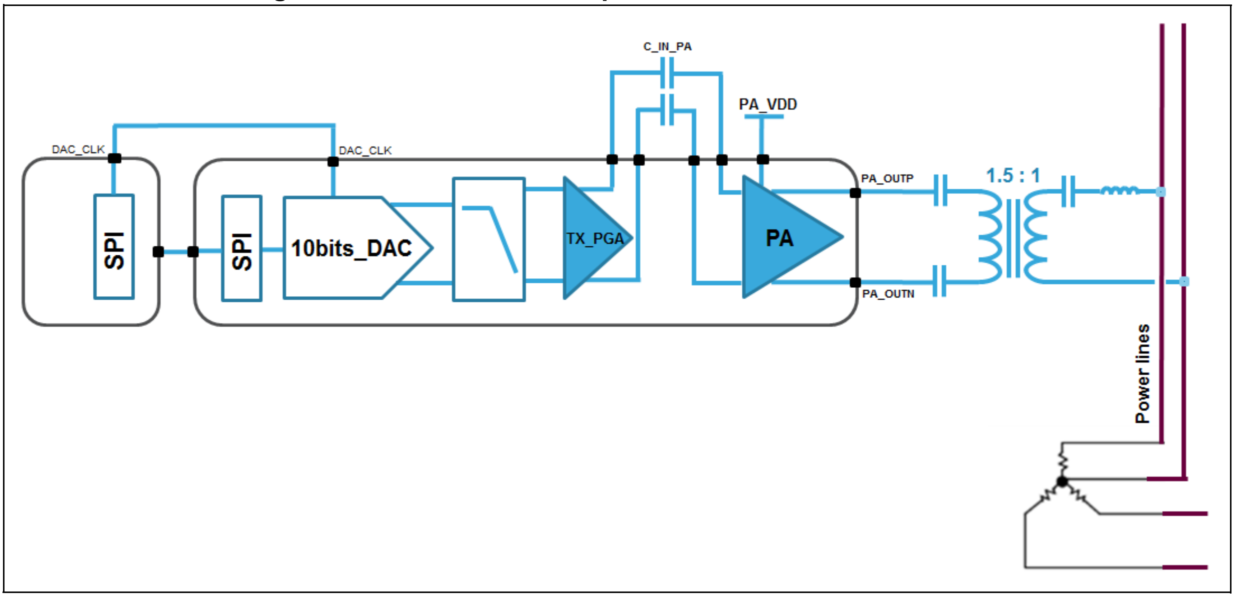
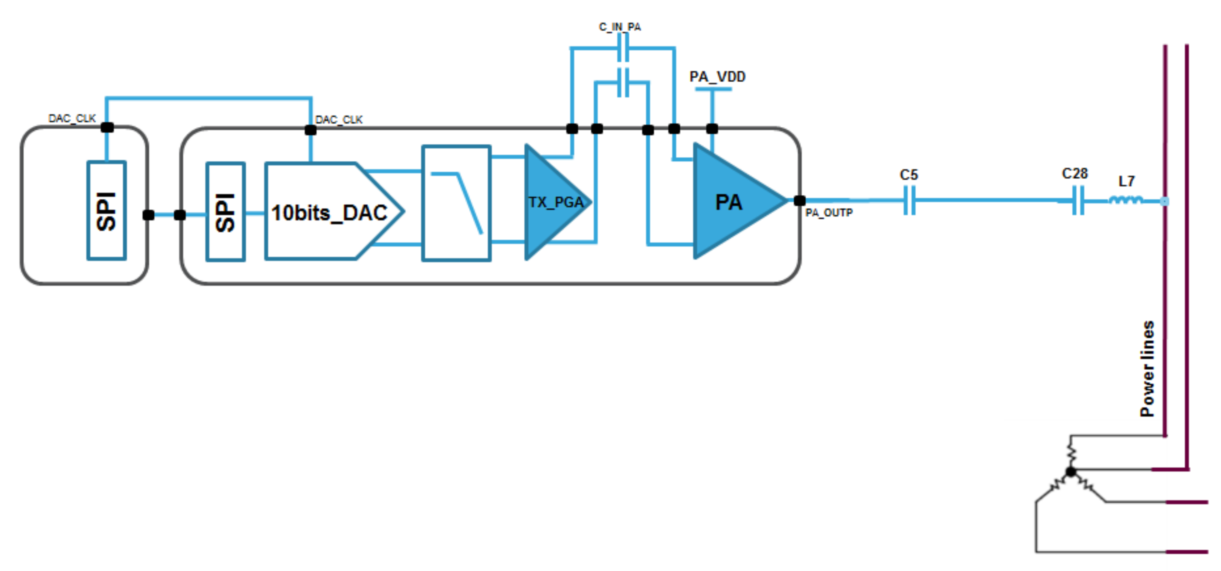


Figure 6. Connection to the power line in single-ended mode



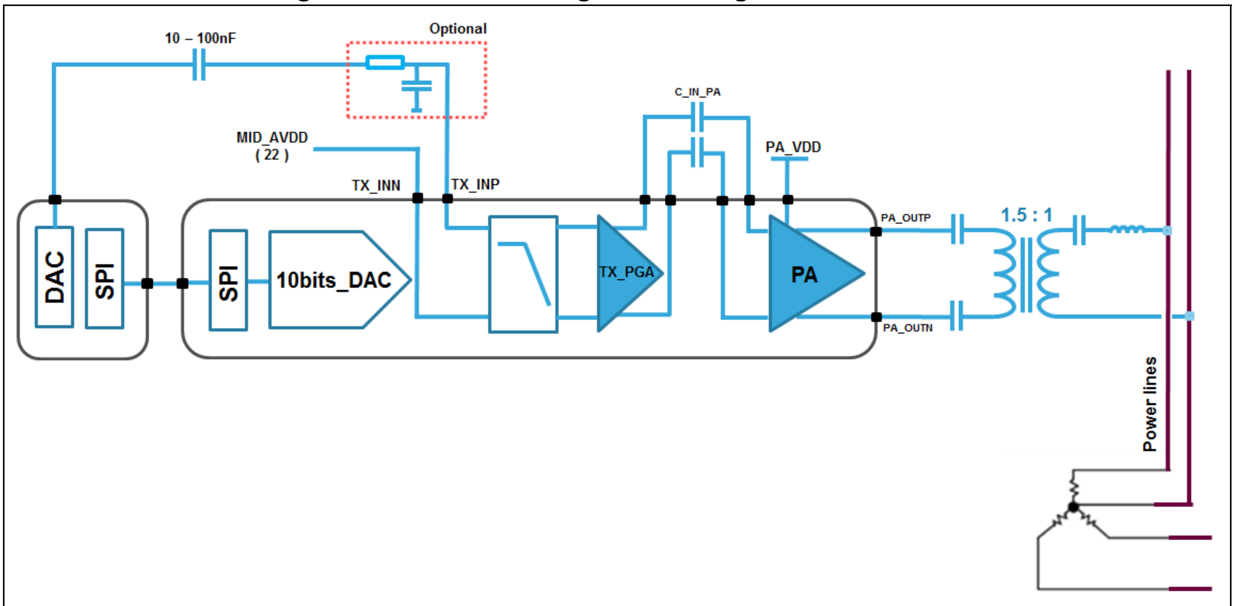
This mode requests an external clock generator from the MCU. See *Section 6* for the constraints related to this conduction mode.

2.2.2 External driving mode, differential-ended power amplifier mode

Figure 7 shows the differential coupling with the power line. The input signal is driven with an external DAC.

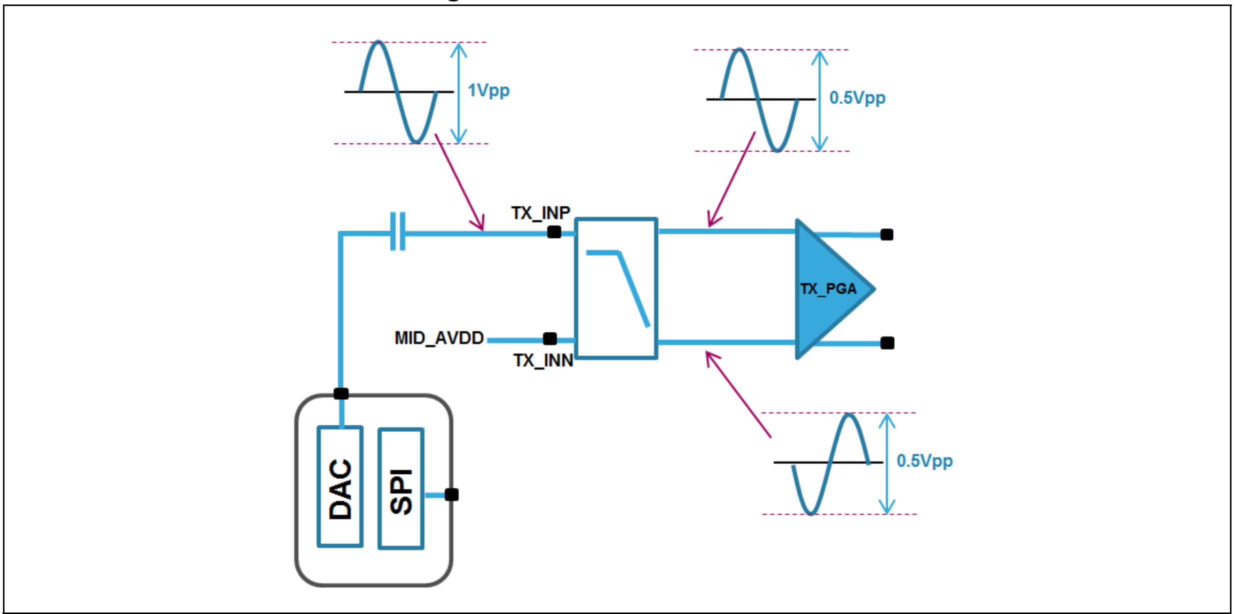
When in external driving mode, the ST-PLC-AFE accepts being driven by analog through the TX_INP input pin. In this case, TX_INN has to be connected to the pin MID_AVDD (pin 22). External drive mode is selected by setting the DAC_EN bit in the Enable register to 0.

Figure 7. External driving mode using an external DAC



Single to differential gain through the filter is equal to 1. If the single-ended input voltage amplitude is 1 Vpp, then the output voltage in differential mode is also equal to 1 Vpp. *Figure 8* shows the single-ended to differential gain conversion.

Figure 8. PGA filter connection



2.3 Rx block

The Rx block consists of:

- Two programmable gain amplifiers (Rx PGA1 and Rx PGA2)
- A fourth-order, low-pass filter
- A selectable high-pass filter

The input sensing mode can be differential mode for better noise immunity or single mode for the lowest BOM.

The **Rx PGA1** can be configured through the SPI to operate as either an attenuator or an amplifier. The gain steps of the Rx PGA1 are -3 dB, 3 dB, 9dB, and 15 dB. The gain can be programmed through the RX_PGA1<1:0> bits in the Gain register. Configuring the Rx PGA1 as an attenuator (at gains less than 0 dB) is useful for applications where large interference signals are present within the signal band. Attenuating large interference allows these signals to pass through the analog Rx signal chain without causing an overload; the interference signal can then be processed and removed within the microprocessor as necessary. The gain steps of the **Rx PGA2** are -6 dB, 6 dB, 18 dB, and 30 dB. The gain can be programmed through the RX_PGA2<1:0> bits in the Gain register.

The **Rx filter** is a very low-noise, unity-gain, fourth-order low-pass filter. Its cutoff frequency is selectable between CENELEC A or CENELEC B, C, or D bands. The selection of the band is achieved through the BAND_SEL bit in the Enable register.

The 35 kHz **high-pass filter** is activated by the HP_EN bit in the Enable register.

Recommended connections for the Rx signal chain are shown in *Figure 9*, *Figure 10*, and *Figure 11*.

Figure 9. Read path with high-pass filter/differential input sense

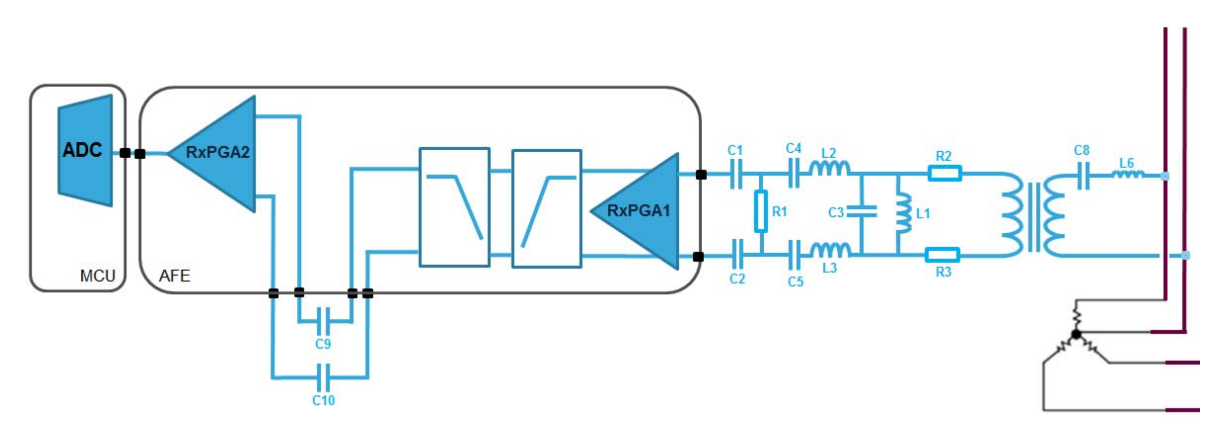


Figure 10. Read path without high-pass filter/differential input sense

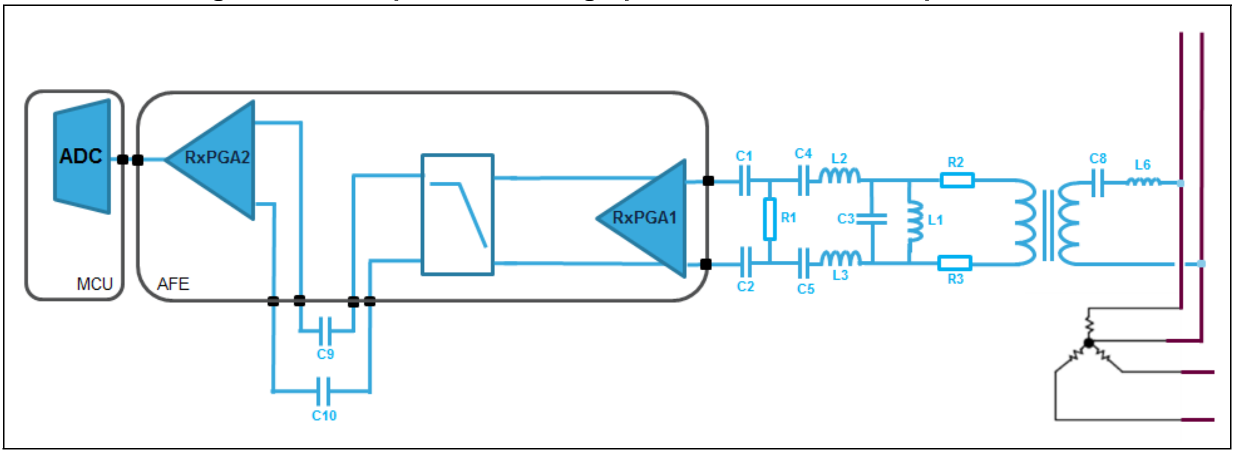
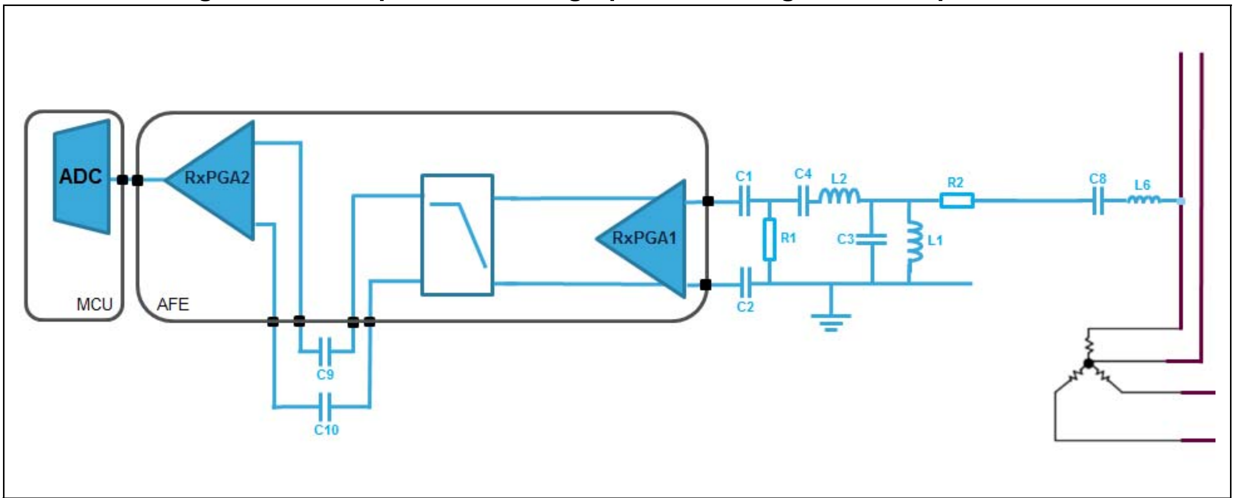


Figure 11. Read path without high-pass filter/single-ended input sense



3 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
PA_VDD	Supply voltage	15	V
AVDD		4.8	
DVDD		4.8	
TOP	Operating temperature, TA (1)	–40 to 150	°C
TSRT	Storage temperature, TA	–55 to 150	
Rthja	Thermal resistance junction-to-ambient QFN48 power PAD	30	°C/W
Rthjc	Thermal resistance junction-to-case QFN48 power PAD	4	
HBM	Human body model ESD	2000	V
MM	Machine model ESD	200	
CDM	Charged device model ESD	500	

1. The device automatically shuts down above 160°C

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
PA_VDD	Power amplifier supply voltage	7 to 14	V
DVDD	Digital supply voltage	3 to 3.6	
AVDD	Analog supply voltage	3 to 3.6	
TOPER	Operating free air temperature range (1)	-40 to 125	°C

1. The device automatically shuts down above 160°C

4 Electrical characteristics

Unless otherwise specified, the test conditions are TJ = 25 °C, PA_VDD = 11 V, AVDD = DVDD = 3.3 V.

Table 4. Power supply

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Current consumptions						
IQPA_vs	Power amplifier current	Iout = 0, PAs P and N on	50	60	80	mA
IQDVDD	Digital supply current	Tx configuration (1)		130	175	µA
		Rx configuration (2)		180	200	
IQAVDD	Analog supply current	Tx configuration (1)	2.6	2.9	3.5	mA
		Rx configuration (2)	2.5	2.8	3.1	
		Zero-cross detectors on, Rx and Tx off, for both zero-cross detectors		60		µA
Power-down (EN = 0)						
PA_VS	Power amplifier supply voltage	EN pin is low			35	µA
DVDD	Digital supply voltage				150	
AVDD	Analog supply voltage				50	
Temperature						
Tj	Junction temperature		-40		125	°C

1. In Tx configuration, the following blocks are enabled: DAC, Tx, and PA. All other blocks are disabled.
2. In Rx configuration, the Rx block is enabled. All other blocks are disabled.

Table 5. Power amplifier

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Frequency response						
BW_PA	Bandwidth	RLOAD = 5 Ω	600	790		kHz
		RLOAD = 50 Ω	1200	1600		
SR_PA	Slew rate	Single-ended mode, 2 V input step and 50 Ω load	20	27		V/µs
		Single-ended mode, 2 V input step and 2 Ω load		10		
		Differential mode, 2 V input step and 100 Ω load	40	54		
		Differential mode, 2 V input step and 4.5 Ω load		20		
FPBW_PA	Full-power bandwidth	Single-ended mode, VPA_OUTP = 5 VPP, 50 Ω load and 100 pF output capacitance		1700		kHz
Output						
V_{OH_PA}	Voltage output swing from PA_Vs	Io = 300 mA, sourcing		0.2	0.6	V
		Io = 1.6 A, sourcing		1.3	2	
V_{OL_PA}	Voltage output swing from PA_Vs	Io = 300 mA, sink		0.2	0.6	
		Io = 1.6 A, sink		1.3	2	
$I_{OUT\_PA\_DC}$	Maximum DC output current	CL0 = CL1 = 11	1.65	2.1		A
$I_{OUT\_PA\_AC}$	Maximum peak current, AC	TJ = –40 °C to 125°C, f = 50 kHz		2.3		
I_{LIM_PA}	PA current limitation	[CL1; CL0] = 00	0.3	0.5		
		[CL1; CL0] = 10	0.75	1		
		[CL1; CL0] = 01	1.2	1.5		
		[CL1; CL0] = 11	1.65	2.1		
$Z_{OUT\_PA\_off}$	Output impedance when PA off	limll	100	150		kΩ
Ro	Output resistance	Io = 1 A, f = 60 kHz		0.2		Ω
Gain						
G	Nominal gain	RLOAD = 50 Ω	6.8	6.9		V/V
—	Gain error		3	0.1	3	%
—	Gain drift	Tj = -40 °C to 125 °C	0.5		0.5	
Input						
Z_{IN_PA}	Input impedance			20		kΩ

Table 5. Power amplifier (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Thermal shutdown						
T_{J_SD}	Junction temperature at shutdown			160		°C
T_{hyst}	Hysteresis			15		
—	Return to normal operation			145		

Table 6. Transmitter

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Tx_DAC						
—	DAC resolution			10		Bits
INL	INL			0.5	±1	LSB
DNL	DNL			0.25	±0.5	
f_{S_DAC}	Sampling frequency			1	1.6	MHz
SINAD	SINAD	Between 0 to 1.6 MHz sampling frequency	47	55		dB
—	DAC maximum output voltage	Differential output VAVDD = 3.3 V	2	2.1		VPP
Tx_filter (fourth-order, Butterworth, low-pass filter) CENELEC A						
V_{IN_Tx}	Input voltage range		GND – 0.1		AVDD + 0.1	V
Z_{IN_Tx}	Input impedance			65		kΩ
f_{C_Tx}	Cut-off frequency		95	100	105	kHz
A_{tt_Tx}	Stop-band attenuation	@ 400 kHz	45	48		dB
		@ 700 kHz		75		
Tx_filter (fourth-order, Butterworth, low-pass filter) CENELEC B, C, and D						
V_{IN_Tx}	Input voltage range		GND – 0.1		AVDD + 0.1	V
Z_{IN_Tx}	Input impedance			65		kΩ
f_{C_Tx}	Cut-off frequency		145	152	160	kHz
A_{tt_Tx}	Stop-band attenuation	@ 400 kHz	30	33		dB
		@ 700 kHz		59		
Tx_PGA						
G_{Tx_PGA}	Gain	[TX_PGA1; TX_PGA0] = 00, 2V/V		+ 6		dB
		[TX_PGA1; TX_PGA0] = 01, 1 V/V		0		
		[TX_PGA1; TX_PGA0] = 10, 1/8 V/V		18		
		[TX_PGA1; TX_PGA0] = 11, 1/64 V/V		36		
$I_{OUT\_Tx\_PGA}$	Output current				1	mA
$Z_{OUT\_Tx\_PGA}$	Output impedance			1		Ω

Table 6. Transmitter (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Global Tx chain						
V_{in_Tx}	Input voltage range		GND – 0.1		AVDD + 0.1	V
t_{WK_Tx}	Wake-up time	All blocks disabled to “ready to transmit”			100	µs
e_{n_Tx}	Differential noise	V(PA_OUTP) – V(PA_OUTN), CENELEC A, Tx PGA gain = 6 dB/PA gain = 6.9 V/V		660		µVrms
		V(PA_OUTP) – V(PA_OUTN), CENELEC B, C, and D, Tx PGA gain = 6 dB/PA gain = 6.9 V/V		670		
—	Filter and PGA gain accuracy			0.5	4	%
Thermometer ladder						
—		Referenced to AVDD/2		4		mV/°C
—		Output voltage @ temp = 25 °C		AVDD/2		V
—		Precision	-5		5	°C

Table 7. Receiver

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Rx PGA1						
V_{IN_PGA1}	DC input level		GND – 0.1		AVDD + 0.1	V
G_{Rx_PGA1}	Gain	[PGA1_G1; PGA1_G0] = 00		-3		dB
		[PGA1_G1; PGA1_G0] = 01		3		
		[PGA1_G1 ; PGA1_G0] = 10		9		
		[PGA1_G1 ; PGA1_G0] = 11		15		
—	Gain accuracy			0.5	4	%
$Z_{IN\_Rx\_PGA1}$	Input impedance	[PGA1_G1; PGA1_G0] = 00		35		kΩ
		[PGA1_G1; PGA1_G0] = 01		25		
		[PGA1_G1; PGA1_G0] = 10		16		
		[PGA1_G1; PGA1_G0] = 11		9		
$BW_{\_Rx\_PGA1}$	Bandwidth	G = -3 dB, 0.707 V/V		10		MHz
		G = 3 dB, 1.414 V/V		8		
		G = 9 dB, 2.83 V/V		8		
		G = 15 dB, 5.66 V/V		4.5		
Rx filter						
V_{IN_Rx}	Input voltage range		GND – 0.1		AVDD + 0.1	V
Rx, third-order, Butterworth, high-pass filter						
$f_{C\_Rx\_HPF}$	Cut-off frequency		33	35	37	kHz
$A_{tt\_Rx\_HPF}$	Stop band attenuation	@ 7 kHz	37	40		dB
Rx_filter (fourth-order, Butterworth, low-pass filter) CENELEC A						
$I_{OUT\_Rx\_filter}$	Output maximum, continuous current	Sourcing, sinking		1	5	mA
$f_{C\_Rx\_LPF}$	Cut-off frequency		95	100	105	kHz
$A_{tt\_Rx\_LPF}$	Stop-band attenuation	@ 400 kHz	45	48		dB
		@ 700 kHz		68		
Rx_filter (fourth-order, Butterworth, low-pass filter) CENELEC B, C, and D						
$I_{OUT\_Rx\_filter}$	Output maximum, continuous current	Sourcing, sinking		1	5	mA
$f_{C\_Rx\_LPF}$	Cut-off frequency		145	152	160	kHz
$A_{tt\_Rx\_LPF}$	Stop-band attenuation	@ 400 kHz	30	33		dB
		@ 700 kHz		63		

Table 7. Receiver (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Rx PGA2						
$V_{IN\_Rx\_PGA2}$	Input voltage range		GND – 0.1		AVDD + 0.1	V
G_{Rx_PGA2}	Gain	[PGA2_G1; PGA2_G0] = 00		- 6		dB
		[PGA2_G1; PGA2_G0] = 01		6		
		[PGA2_G1; PGA2_G0] = 10		18		
		[PGA2_G1; PGA2_G0] = 11		30		
—	Gain accuracy			0.5	4	%
BW_{Rx_PGA2}	Frequency response	[PGA2_G1; PGA2_G0] = 00		5		MHz
		[PGA2_G1; PGA2_G0] = 01		4		
		[PGA2_G1; PGA2_G0] = 10		3		kHz
		[PGA2_G1; PGA2_G0] = 11		1.5		
$Z_{IN\_Rx\_PGA2}$	Input impedance	[PGA2_G1; PGA2_G0] = 00		45		kΩ
		[PGA2_G1; PGA2_G0] = 01		18		
		[PGA2_G1; PGA2_G0] = 10		18		
		[PGA2_G1; PGA2_G0] = 11		10		
Rx chain						
e_{n_Rx}	Integrated noise that includes whole Rx line (referred to the input)	CENELEC Band A μV_{RMS} (40 kHz to 95 kHz) Gain = 45 dB		8		μV_{RMS}
		CENELEC Bands B/C/D μV_{RMS} (95 kHz to 140 kHz) Gain = 45 dB		8		μV_{RMS}
t_startup	Wake up time	From all devices powered down to Rx ready for operations			500	µs
t_read_start up	Rx power-up time	Tx to Rx transition time, coupling capacitors of 3.3 nF		10		
Rx out						
V_{OUT_Rx}	Output voltage range	Vcc = 3.3 V, single ended output	0.1		3.2	V
C_{OUT_Rx}	Output capacitance				50	pF
Z_{OUT_Rx}	Output impedance			1		Ω

Table 8. Digital domain

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Digital inputs (nCS, EN, SCLK, DIN, and DAC_CLK)						
V_{IH}	High-level input voltage		0.25 x VDVDD			V
V_{IL}	Low-level input voltage				0.75 x. VDVDD	
Digital outputs (DOUT and INT)						
V_{OH}	High-level output voltage	Source current, IOH = 2 mA	VDVDD – 0.45		VDVDD	V
V_{OL}	Low-level output voltage	Sink current, IOL = - 2 mA	GND		GND + 0.45	

Table 9. Zero crossing detector

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN_ZCR}	DC input, ZC1_IN; ZC2_IN		AGND – 0.3		AVDD + 0.3	V
V_{THR_ZCR}	Rising threshold		0.9		1	
V_{THF_ZCR}	Falling threshold		0.45		0.55	
C_{IN_ZCR}	Input capacitance			3		pF
V_{OH_ZCR}	High-level output ZC1_OUT; ZC2_OUT	IOL = 3 mA	DVDD – 0.3		DVDD	V
V_{OL_ZCR}	Low-level output ZC1_OUT; ZC2_OUT	IOH = - 3 mA	DGND		DGND + 0.3	

5 Registers

Table 10. Main register table

Register	Address	Default	Function
Data	0x00h	000h	Data register
Status/Flag	0x01h	000h	Status register
Gain	0x02h	003h	Tx, Rx gain and current limitation selection
Enable	0x03h	12Ch	Block enable or disable
ID	0x04h	069h	Die name and revision

Each register is 12 bits in width.

The registers are described in more detail in the tables below. Note in the column “Location”, 0 = LSB and 11 = MSB.

Table 11. Data register

Bit name	Location	Function
DATA0	0	LSB of SPI DATA
DATA1	1	SPI DATA
DATA2	2	
DATA3	3	
DATA4	4	
DATA5	5	
DATA6	6	
DATA7	7	
DATA8	8	
DATA9	9	MSB of SPI DATA

Table 12. Status register

Bit name	Location	Default	R/W	Function
OVC_FLAG	2	0	R/W	Overcurrent condition Read 1: over current condition Read 0: no over current Write 0: reset the bit See *Section 9.3: Interruptions* for further information
T_FLAG	1	0	R/W	Thermal temperature shutdown Read 1: thermal shutdown activated Read 0: no thermal shutdown Write 0: reset the bit See *Section 9.3: Interruptions* for further information

Table 13. Gain register

Bit name	Location	Default	R/W	Function
RX_PGA2<1:0>	7-6	00	R/W	Select gain of Rx PGA2 00: - 6 dB 01: 6 dB 10: 18 dB 11: 30 dB
RX_PGA1<1:0>	5-4	00	R/W	Select gain of Rx PGA1 00: -3 dB 01: 3 dB 10: 9 dB 11: 15 dB
TX_PGA1<1:0>	3-2	00	R/W	Select gain of Tx PGA 00: + 6 dB 01: 0 dB 10: - 18 dB 11: - 36 dB
CL<1:0>	1-0	00	R/W	PA current limitation 00: 0.5 A typ 01: 1.5 A typ 10: 1 A typ 11: 2.1 A typ

Table 14. Enable register

Bit name	Location	Default	R/W	Function
ZCR_EN	9	0	R/W	Zero crossing detector enable 0: ZC1 and ZC2 off 1: ZC1 and ZC2 on
BAND_SEL	8	1	R/W	Select CENELEC bandwidth 1: 100 kHz CENELEC band A 0: 150 kHz CENELEC band B, C, and D
PA_EN	7	0	R/W	Enable power amplifier 0: PAs P and N off 1: PAs P and N on
TX_EN	6	0	R/W	Enable Tx channel 0: Tx off 1: Tx on
RX_EN	5	1	R/W	Enable Rx channel 0: Rx off 1: Rx on
DAC_EN	4	0	R/W	Enable internal DAC 0: DAC off and Tx path driven by external DAC 1: Tx path driven by the internal DAC
PA2_EN	3	1	R/W	Enable power amplifier N 0: PA N side off 1: PA N side on
HP_EN	2	1	R/W	Enable high-pass filter 0: high-pass filter off 1: high-pass filter on
RST_SPI	1	0	R/W	Reset all registers (1) 0: normal mode 1: reset all the registers to their default value
PD_SPI	0	0	R/W	Power-down all devices (2) 0: all devices on 1: all devices off

1. The HP_EN bit is self-resetting.
2. A reset cancels this command to its “0” default value.

Table 15. ID register

Bit name	Location	Default	R/W	Function
ID	7-3	01101	R	ID number
REV	2-0	001	R	revision

6 SPI interfaces

The ST-PLC-AFE interface supports SPI mode 0.0 and 1.1. A host SPI frame consists of a read/write bit, a 3-bit register address, and a 12-data bit register. Data are shifted out on the falling edge of the SCLK and latched on the rising edge of the SCLK. Refer to *Section 6.1: SPI timing* for a valid host and SPI communication protocol.

When nCS = 1, the state machine is reset asynchronously to the R/W state. The nCS does not need to go high between transfers but, it must be low during the entire transfer. Address bits identify target registers for writing data. There are three address bits which allow 8 x 12 bit registers, including the DAC register. Received data are stored in the target register on the 16th edge of the SCLK, if R/W is low.

6.1 SPI timing

Figure 12. SPI mode 0.0

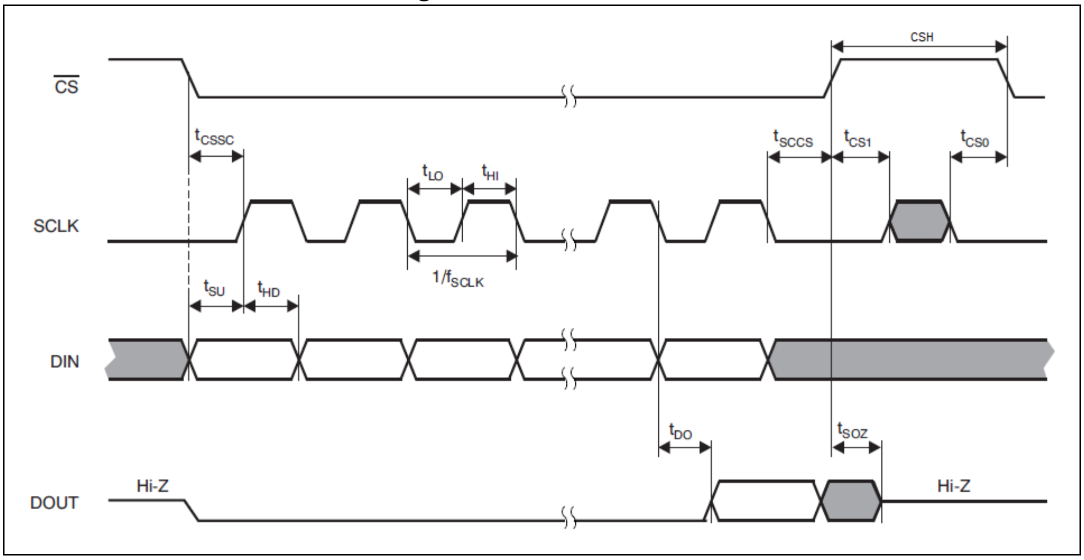
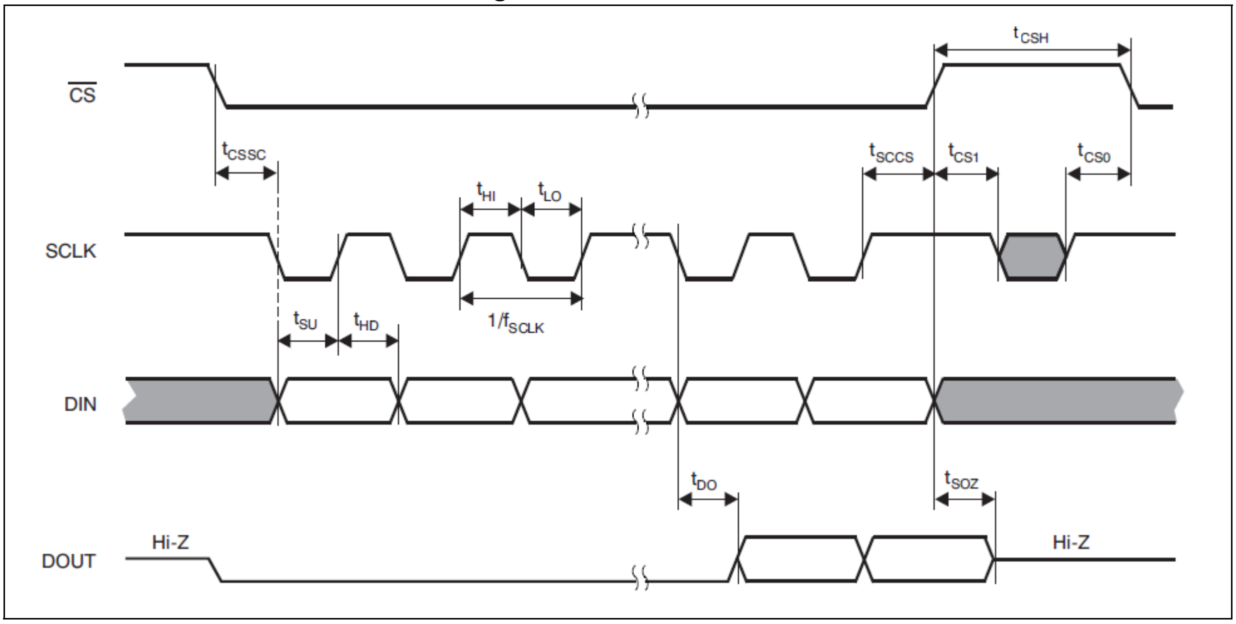


Table 16. Timing table, DVDD from 3 V to 3.6 V, temperature between -40 °C to 125 °C, CLOAD on SDOUT = 10 pF

Symbol	Parameter	Condition	Min	Typ	Max	Unit
—	Input capacitance			—	1	pF
tRFI	Input rise/fall time	nCS, DIN, SCLK			2	ns
tRFO	Output rise/fall time	SDOUT			10	
tCSH	nCS high time		20			
tCSO	SCLK edge to nCS fall setup time		10			
tCSSC	nCS fall to first SCLK edge setup time		10			
fSCLK	SCLK frequency				30	MHz
tHI	SCLK high time		12			ns
tLO	SCLK low time		12			
tSCCS	SCLK last edge to nCS rise time		10			
tSU	DIN setup time		5			
tHD	DIN hold time		5			
tDO	SCLK to DOUT valid propagation delay				12	
tSOZ	nCS rise to DOUT forced to Hi-Z				20	

Figure 13. SPI mode 1.1



6.2 Read/write figures in SPI mode 0.0

Figure 14. SPI write

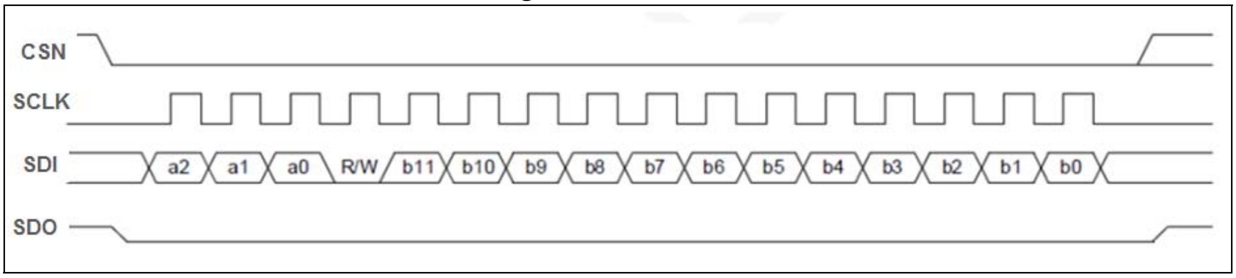
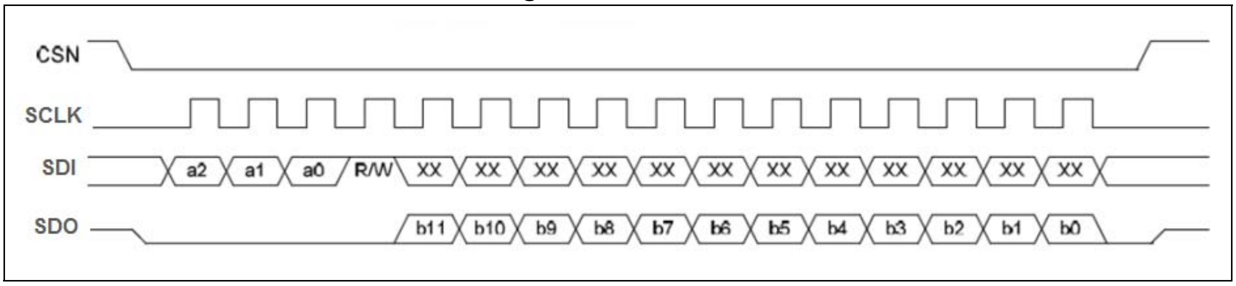


Figure 15. SPI read



7 Powering the device and resetting the SPI and registers

7.1 Turning the device on and off

The ENABLE input pin (EN) allows the device to be turned on and off.

When EN is set to zero, all internal consumptions are reduced to a minimum, the SPI interface is ready to receive messages from the microcontroller, and all internal registers keep their value. Consequently, EN does not reset the IC. Using the SPI interface when the IC is powered down, allows the system to be preprogrammed.

When the EN pin is high (1), the ST-PLC-AFE device operates normally.

By default, the PD_SPI bit is set to 0 (which means that all internal blocks of the device are activated). To turn off the device using the registers, the PD_SPI must be set to 1. Then, all internal blocks are turned off. The SPI interface is still active for microcontroller communication and all registers keep their value without any resets.

7.2 Resetting the internal registers

The internal registers are reset by setting the RST_SPI bit in the Enable register to 1. By doing this, all internal registers are set to their default values and the SPI interface performs an auto-reset.

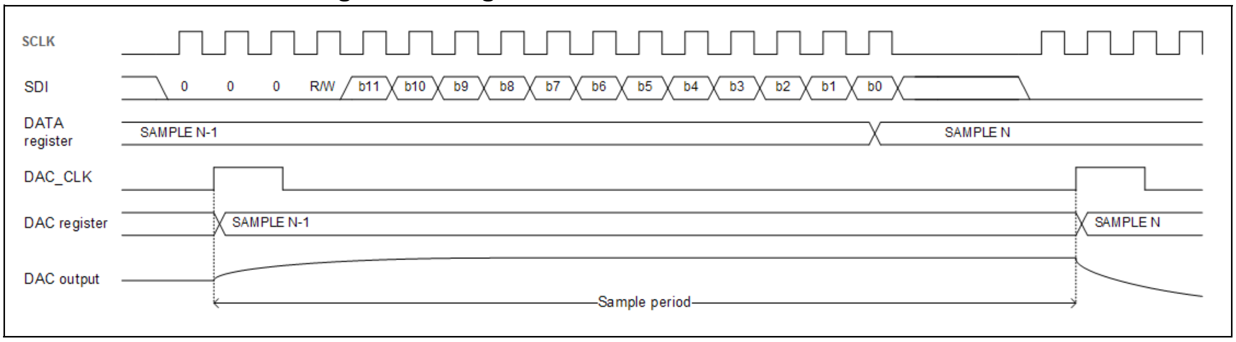
When the analog power supply, AVDD, increases from zero to its final value, an internal power-on-reset (POR) occurs. All digital registers are reset when AVDD crosses the voltage window 1.6 V to 2.4 V.

7.3 Resetting the SPI

The SPI is reset using the high state of the input pin nCS.

7.4 Use of an external DAC

Figure 16. Register access with an external DAC



The Data register is used to update the DAC output. It is programmed directly by the SPI at address 000h. Data are transferred to the DAC at the rising edge of DAC_CLK pin which triggers the start of a conversion.

The DAC_CLK pin must be supplied with a stable, low-jitter, clock signal at the required sample frequency.

The SCLK and DAC_CLK pins can be completely asynchronous, but SCLK must be more than 16 times the frequency of the DAC_CLK pin to ensure that the Data register is updated with a new sample between each DAC_CLK pulse.

8 Typical characteristics

Figure 17. Tx filter CENELEC band A

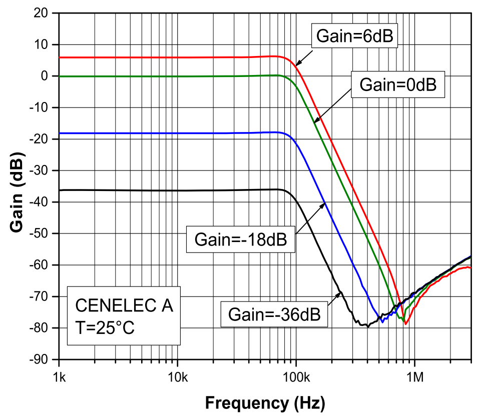


Figure 18. Tx filter CENELEC band B, C, and D

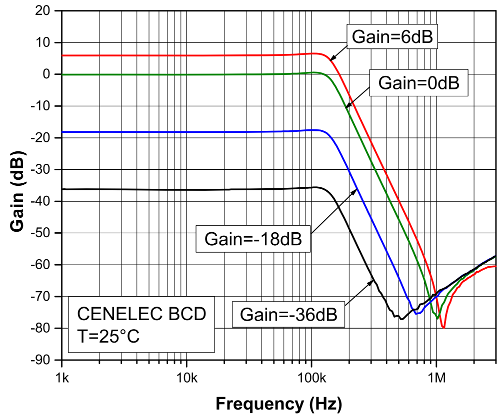


Figure 19. Tx filter small step

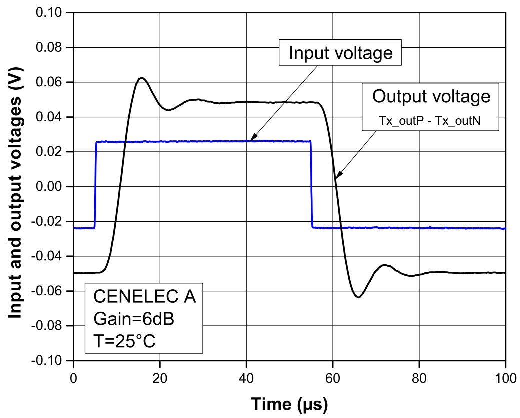


Figure 20. Tx and Rx low-pass cut-off frequencies vs temperature

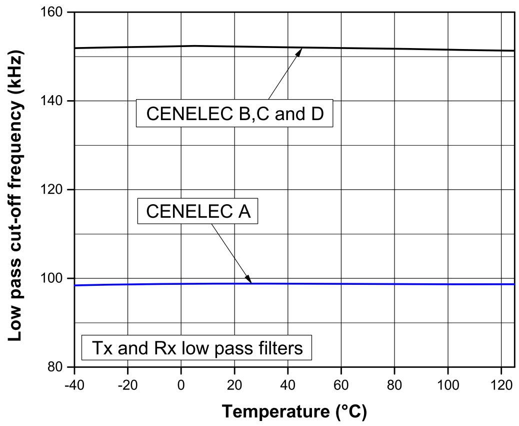


Figure 21. Power amplifier bode diagram

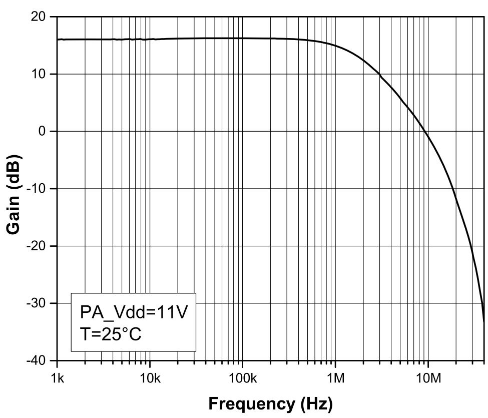


Figure 22. Power amplifier small step response

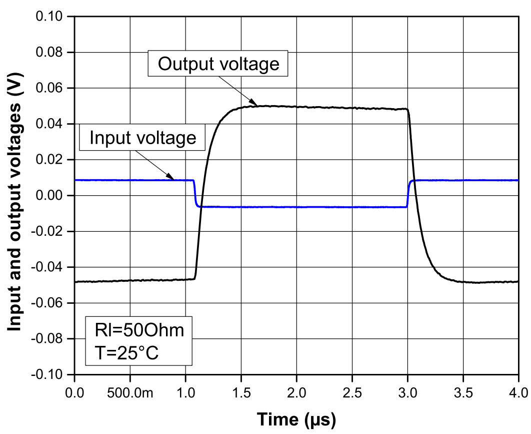


Figure 23. Power amplifier output voltage vs output current

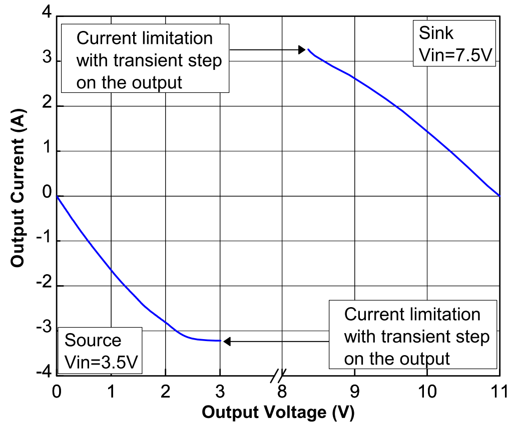


Figure 24. Power amplifier large step response

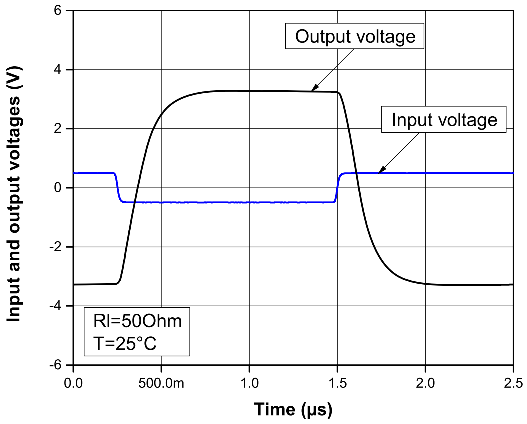


Figure 25. Power amplifier output impedance

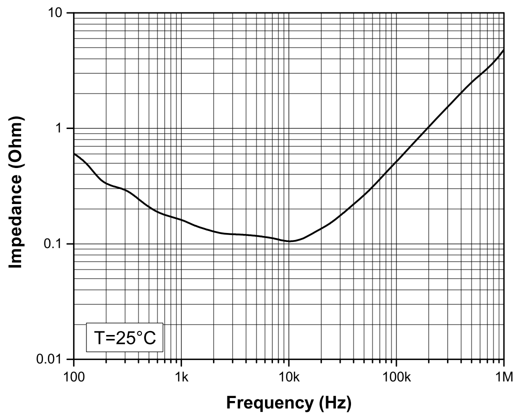


Figure 26. Rx to Tx transition

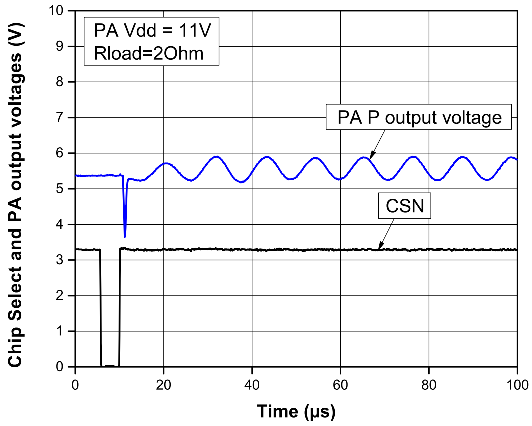


Figure 27. Tx to Rx transition

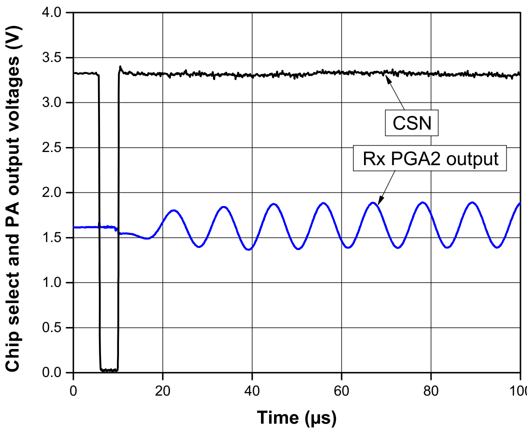


Figure 28. Rx low-pass filter with PGA1

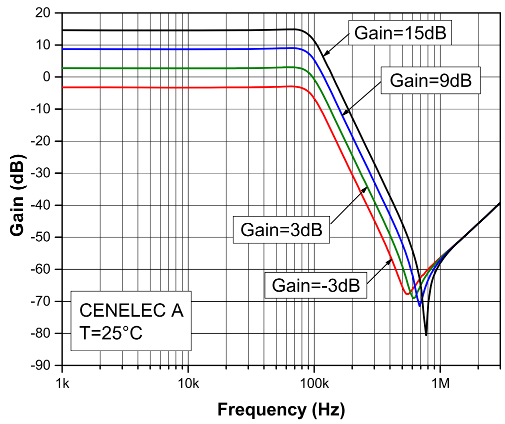


Figure 29. Rx low- and high-pass filters with PGA1

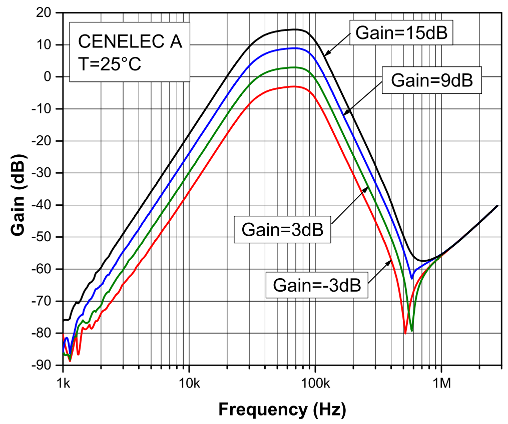


Figure 30. Rx PGA2 bode diagram

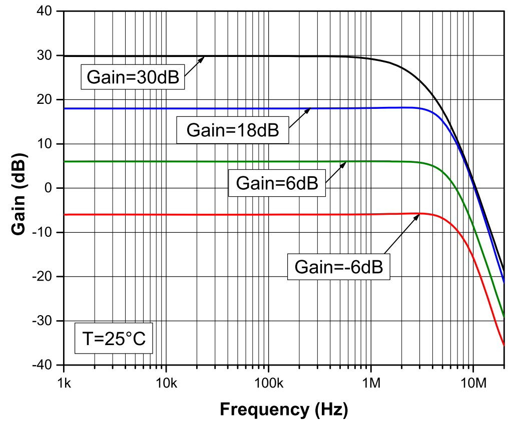


Figure 31. Rx small step response

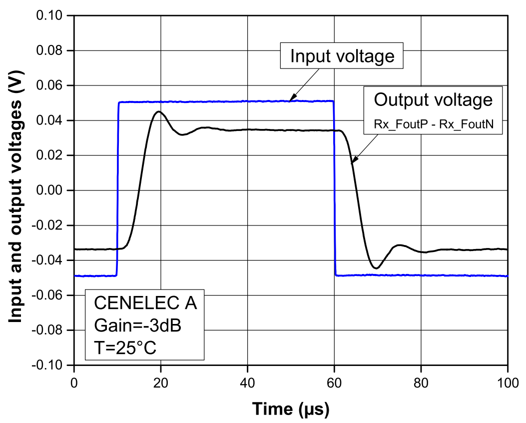


Figure 32. Rx noise density

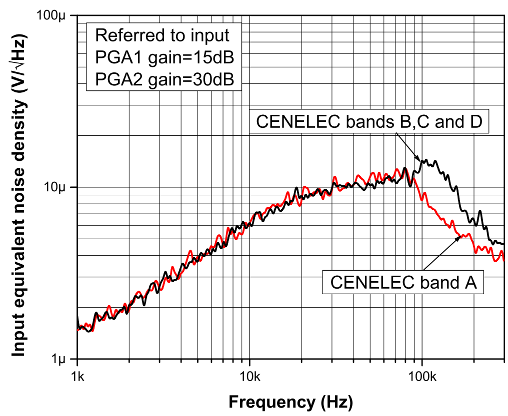


Figure 33. Tx noise density in single-ended mode

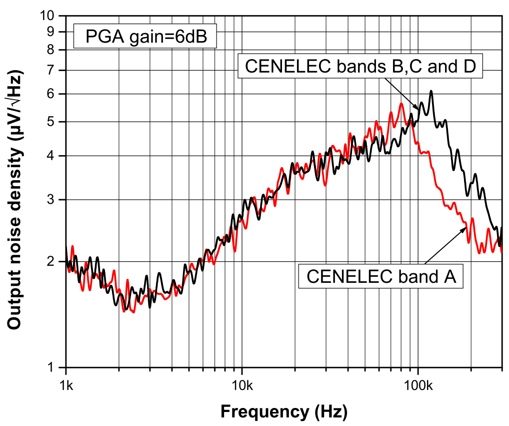


Figure 34. Tx noise density in differential mode

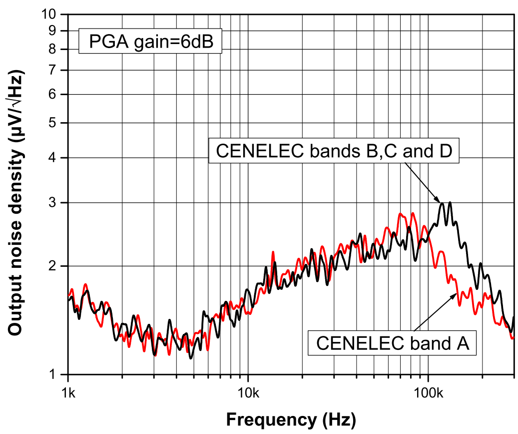
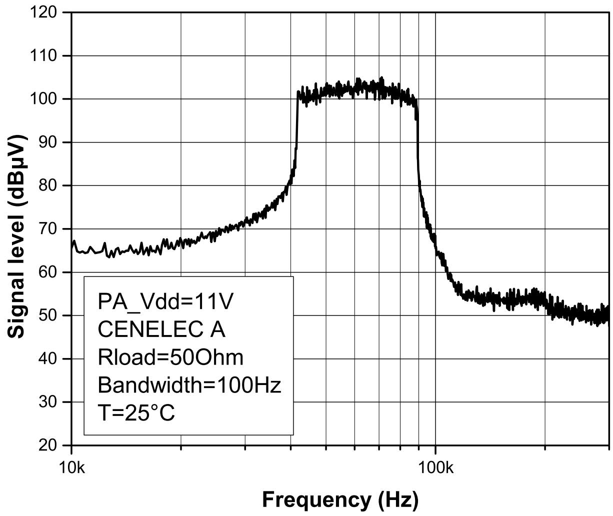


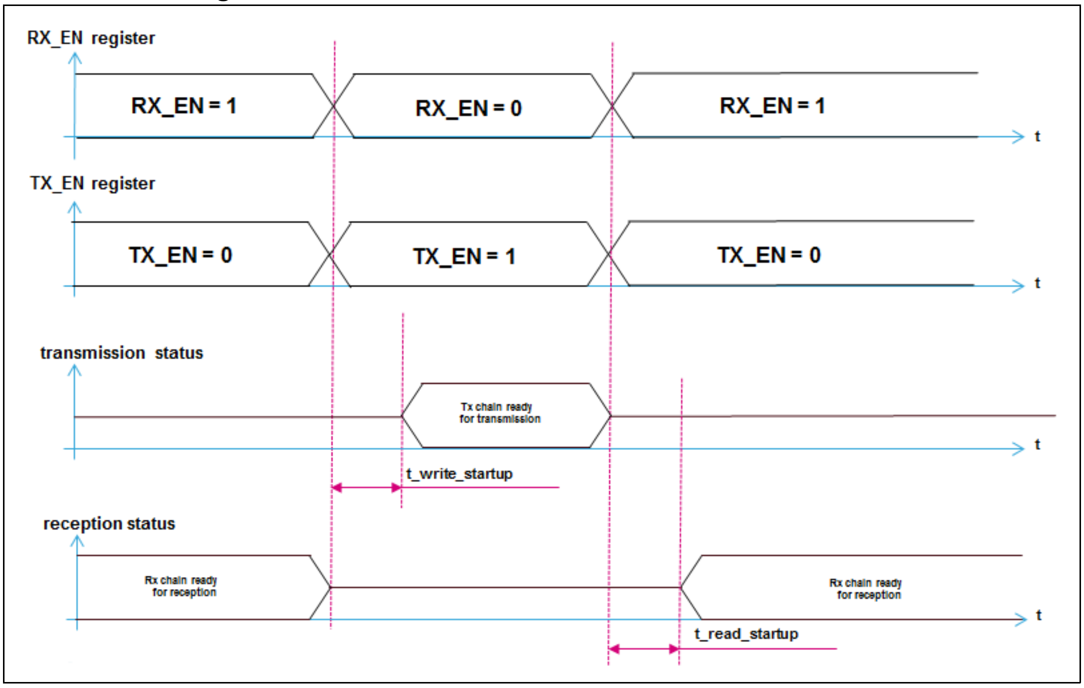
Figure 35. OFDM spectral response



9 System timings and interruptions

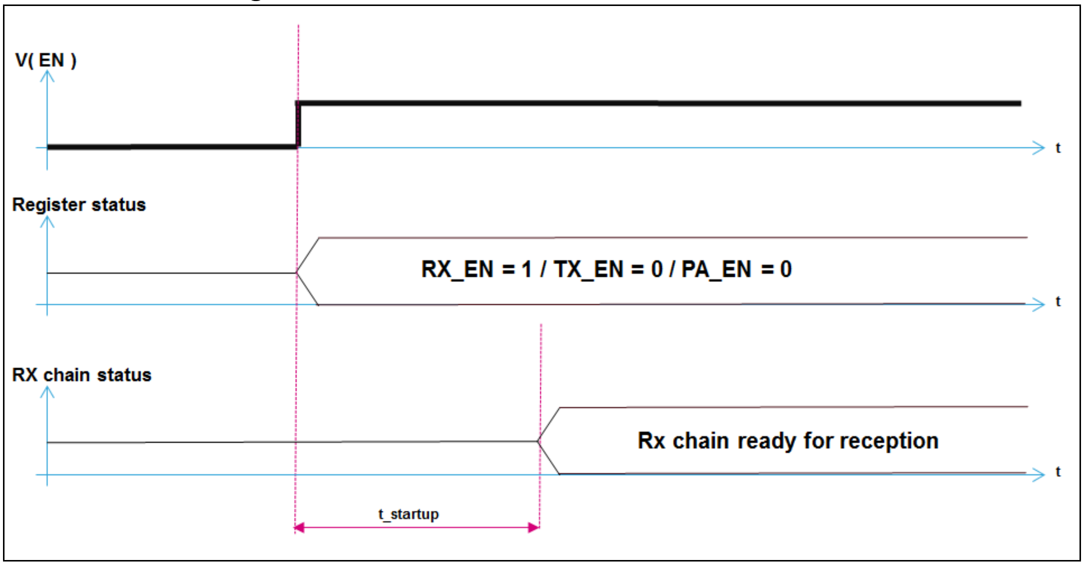
9.1 Rx - Tx - Rx transitions

Figure 36. Transmission between read and write modes



9.2 Power-down to Rx

Figure 37. Transmission between off mode to read



The analog front end needs t_startup to bias the external capacitors correctly. This period of time lasts 50 µs, but it can vary depending on external capacitors values.

9.3 Interruptions

The interrupt pin (INT) can be used to warn the microprocessor/DSP of unusual operating conditions. The INT pin can be triggered by two external circuit conditions, depending on the enable register settings. The ST-PLC-AFE can be programmed to issue an interrupt on current or thermal overload.

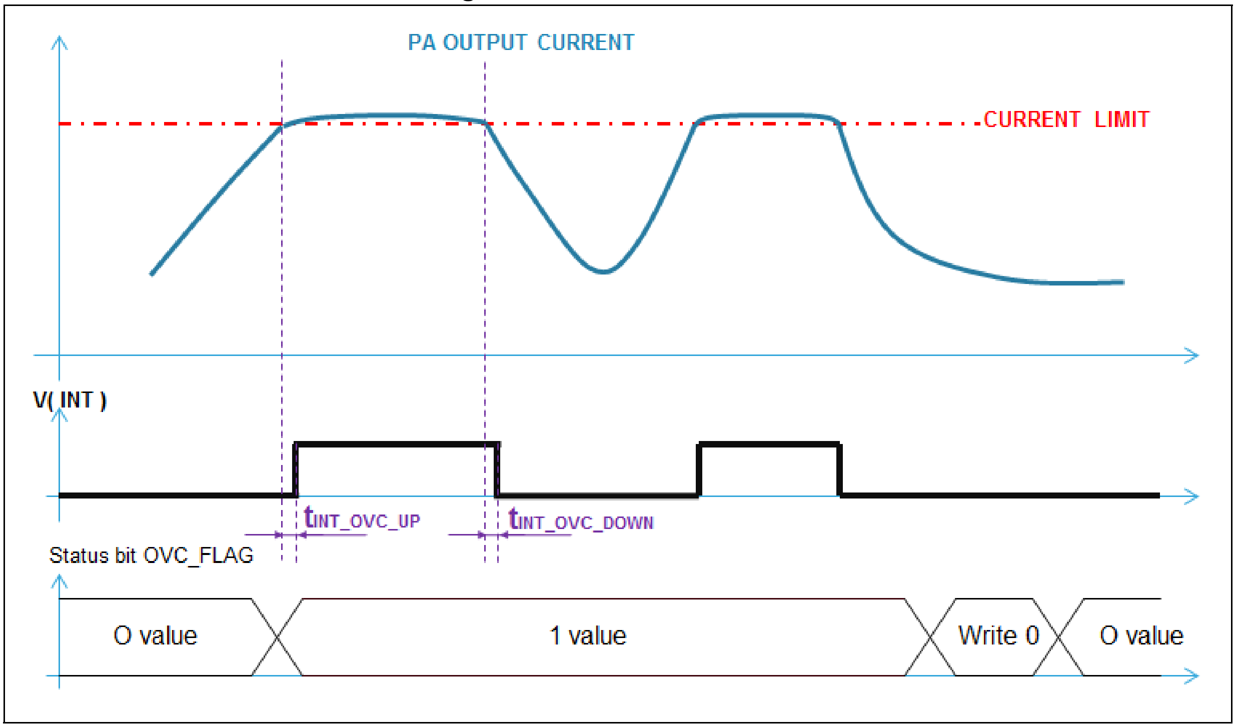
9.3.1 Overcurrent condition

The maximum output current allowed from the PA can be programmed using the SPI communication system (CL<1:0> bit in the Gain register). If a FAULT condition occurs and causes an overcurrent, the PA goes into current limitation and the OVC_FLAG bit (in the Status register) changes to 1.

The OVC_FLAG bit remains set to 1 even after the device returns to normal operation. It can be reset when the microprocessor writes 0 inside the Status register. It can also be set back to 0 through a system reset using the RST_SPI bit in the Enable register.

This configuration results in the presence of an interrupt signal at the INT pin. The INT signal returns to 0 when the device returns to normal operation. The latency time between the interrupt and the INT change of state $t_{INT\_OVC\_UP}$ and $t_{INT\_OVC\_DOWN}$ is 1 µs.

Figure 38. Overcurrent event

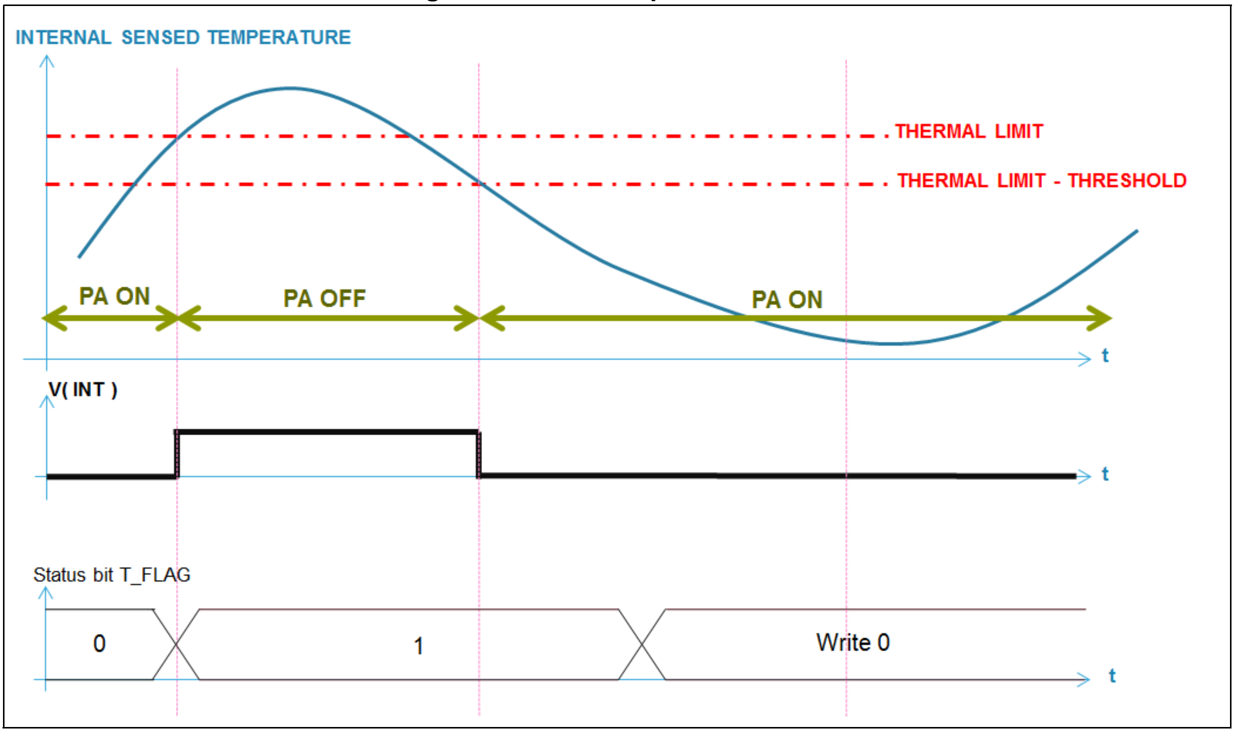


9.3.2 Over temperature condition

The ST-PLC-AFE contains protective, internal circuitry that automatically disables the PA output stage if the junction temperature exceeds 160 °C. The device also includes a thermal hysteresis which allows the PA to resume normal operation when the junction temperature falls to 145 °C.

If a fault condition occurs that causes a thermal overload, the T_FLAG bit switches from 0 to 1. This configuration results in an interrupt signal at the INT pin. The T_FLAG bit remains set to 1 even after the device returns to normal operation. The T_FLAG bit remains 1 until it is reset by the microprocessor (when 0 is written inside the T_FLAG bit of the Status register). Another way to reset the T_FLAG bit is to use the RST_SPI system reset operation.

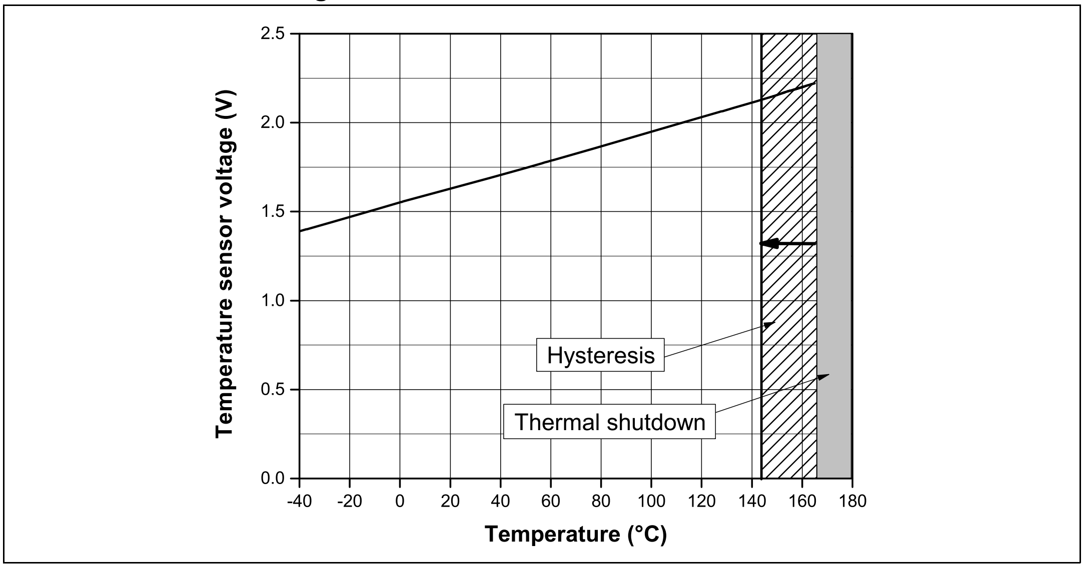
Figure 39. Over temperature event



10 Application information

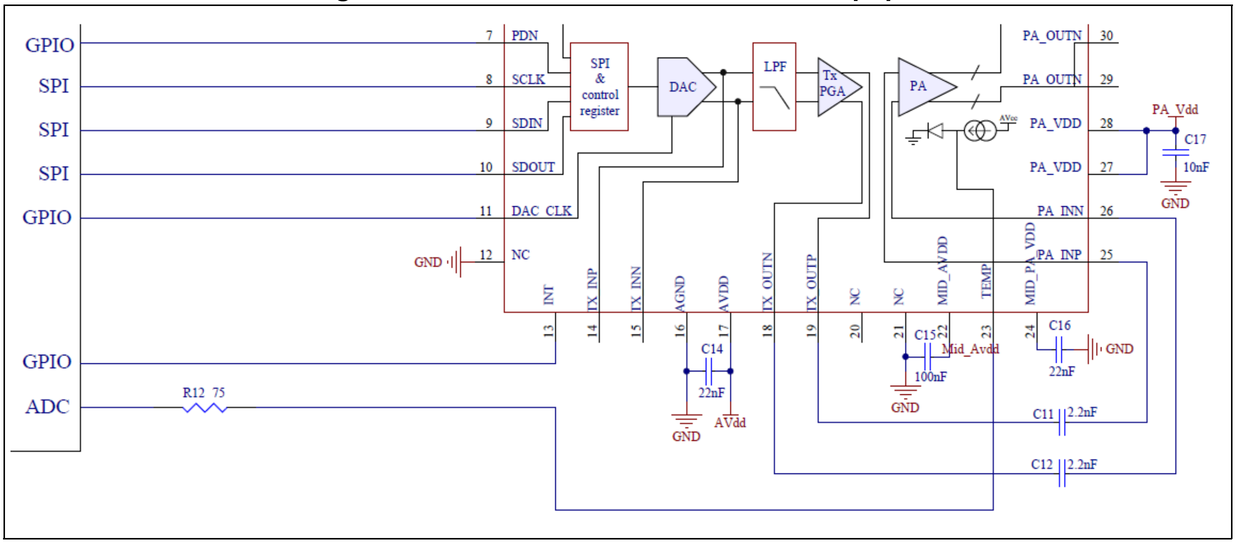
10.1 Thermal sensor

Figure 40. Thermal ladder characteristic



The THERMAL pin can be connected to a microcontroller GPIO pin which allows the internal temperature to be directly measured. The thermal sensor is physically placed close to the PAs to give the highest temperature indication inside the silicon.

Figure 41. Connection of TEMP and interrupt pin



10.2 Thermal considerations

When the ST-PLC-AFE transmits information on low-impedance, power-line domains, more power is dissipated which leads to junction temperature increase. If the junction temperature reaches 160 °C, the thermal protection latches to freeze the transmission. This is why good PCB design and correct management of the heat flow from the ST-PLC-AFE is necessary to minimize losses and decrease system temperature, extend device operating life, and maximize performance.

10.2.1 Maximizing the heat flow from the junction temperature to the PCB

The package of the ST-PLC-AFE is a QFN48-pin with an exposed PAD. The majority of heat is evacuated through the exposed PAD, on the underside of the package, which is why the package must be soldered to the PCB thermal pad with the lowest resistivity possible. The thermal pad should be the same size as the exposed pad and multiple vias.

10.2.2 Reducing the PCB thermal resistance

This can be done by increasing the number of layers, using thicker copper, and/or increasing the PCB area. The figures below show PCB examples of thermal resistance as a function of the number of PCB layers, PCB area, and copper thickness.

Figure 42. Thermal resistance as a function of the number of layers in the PCB

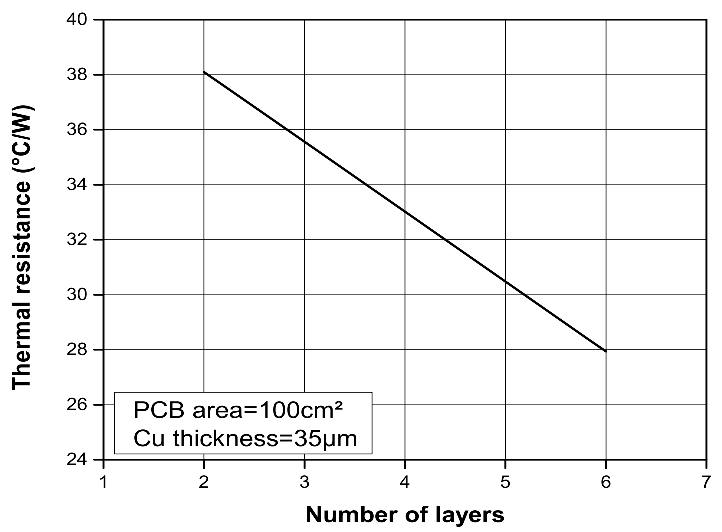


Figure 43. Thermal resistance as a function of PCB area

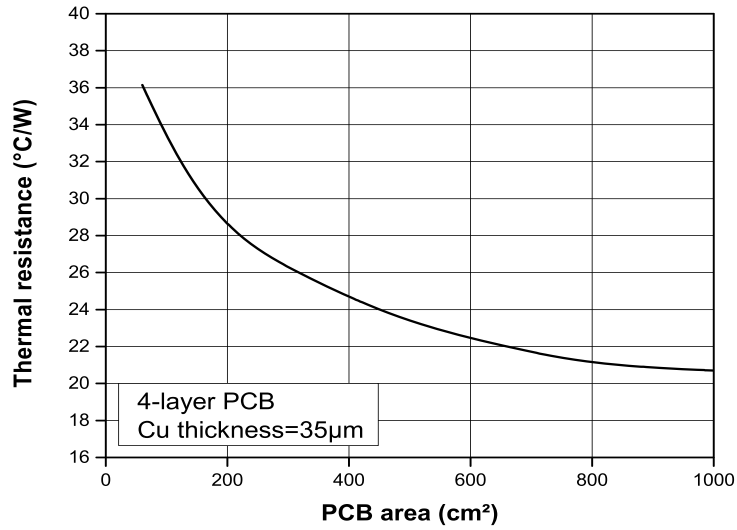
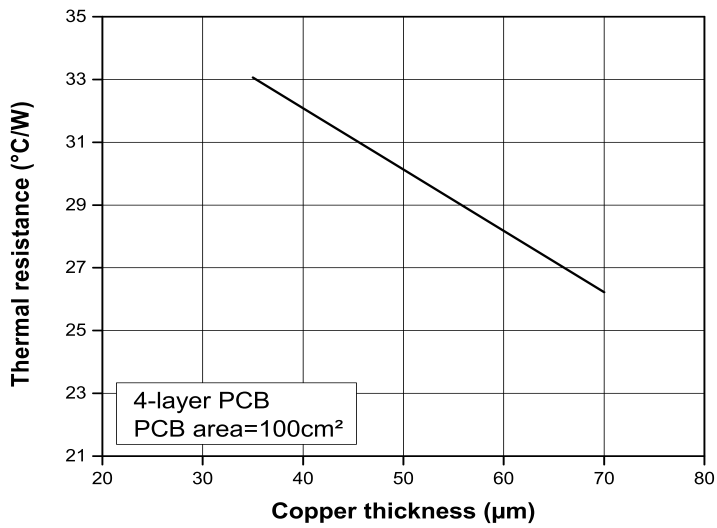


Figure 44. Thermal resistance as a function of copper thickness



10.2.3 Reducing supply voltage from the power amplifier

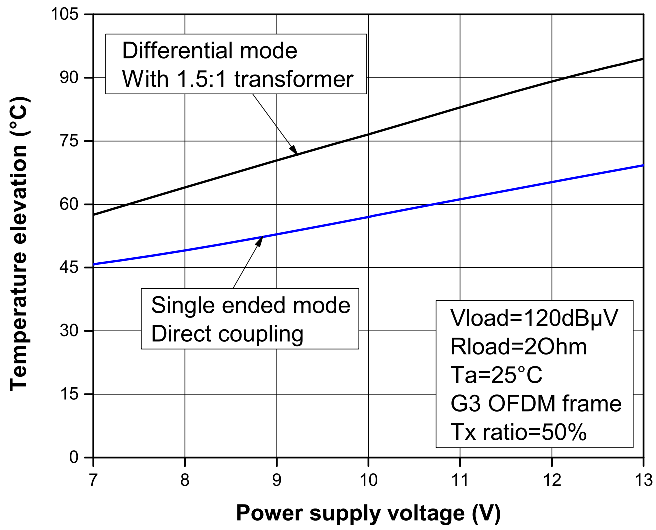
The system architecture has to take into account that power dissipated in transmission is strongly linked to the supply voltage level of the PA. For example, in differential mode with a 50 % Tx duty cycle, the power dissipated with 2 Ω load is 2.28 W when PA_VDD = 11 V and 1.66 W when PA_VDD = 8 V.

Note that this power corresponds to the current being drawn out of the PA power supply voltage multiplied by its supply voltage.

10.3 Moving from differential mode to single-ended mode

Differential mode can drive extremely low impedances, even at low supply voltage. However, differential mode also activates two PAs at the same time which increases the internal temperature (see *Figure 45*).

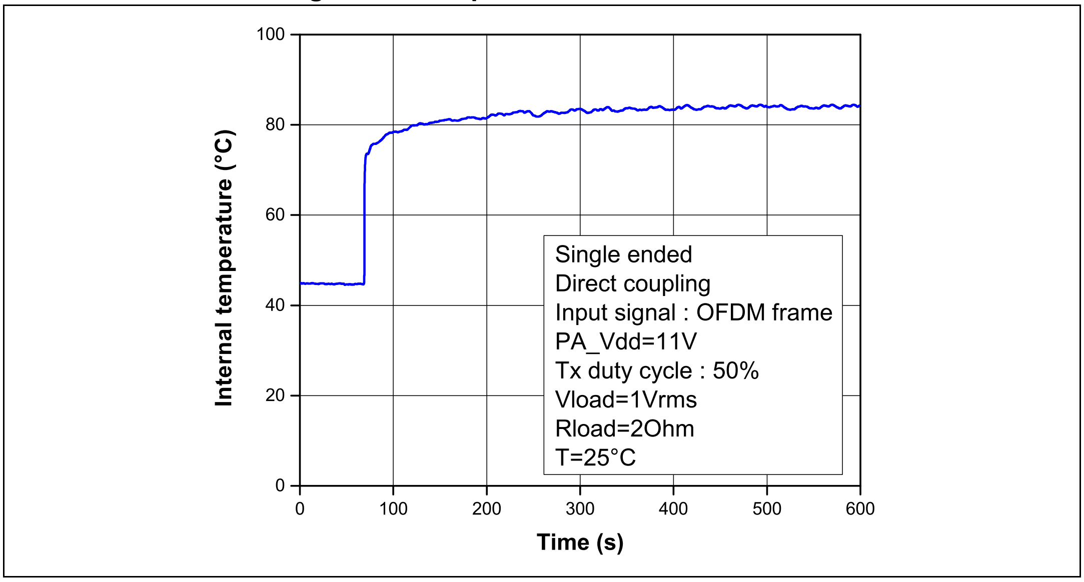
Figure 45. Temperature elevation in differential-ended and single-ended modes vs power supply voltage



To minimize the dissipated power and thus the temperature elevation, it is recommended to use the minimum power supply voltage.

In *Figure 45*, the temperature elevation was monitored after a “waiting” time to achieve a stable temperature. Such “waiting” time and the temperature elevation depends on the number of PCB layers, copper thickness, PCB area, and PCB layout. *Figure 46* is an example of temperature elevation over time for the following board features: 24 cm², 4-layer PCB, and 35 µm copper thickness.

Figure 46. Temperature elevation vs time



10.4 Circuit protection

Electrical perturbations may happen on the power lines, such as capacitor bank switching, inductive switching, lighting, and other grid fault conditions. Consequently, it is recommended to protect the ST-PLC-AFE in differential mode using the schematic shown in *Figure 47* and in single-ended, direct coupling mode using the schematic shown in *Figure 48*.

Figure 47. Protection in differential coupling mode

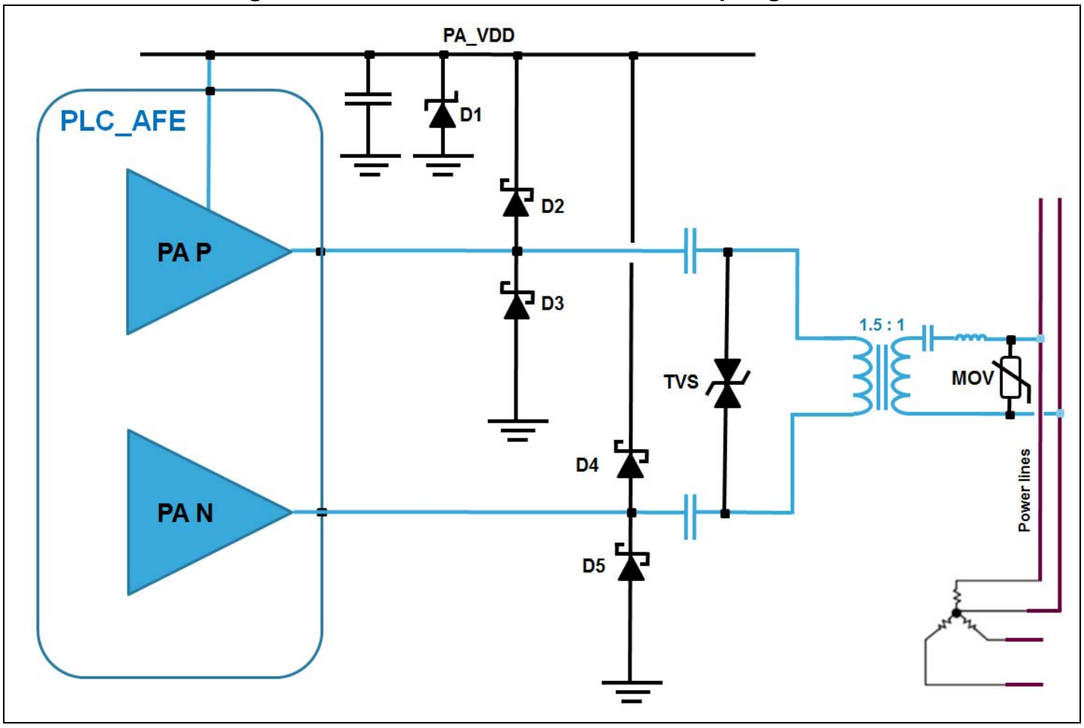


Figure 48. Protection in single-ended coupling mode

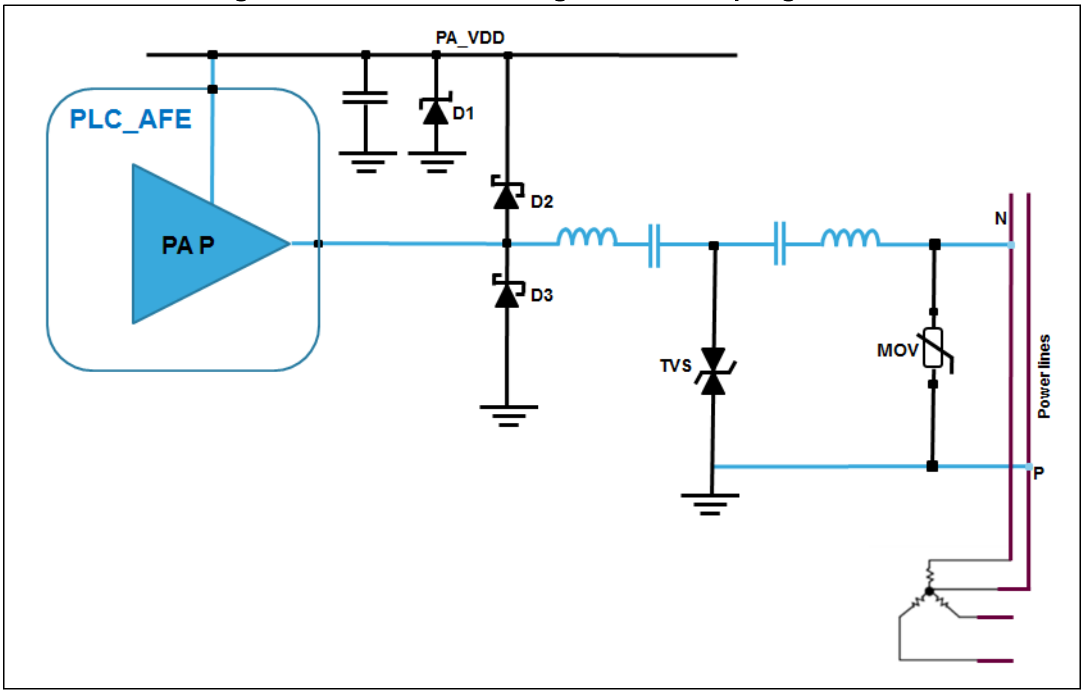


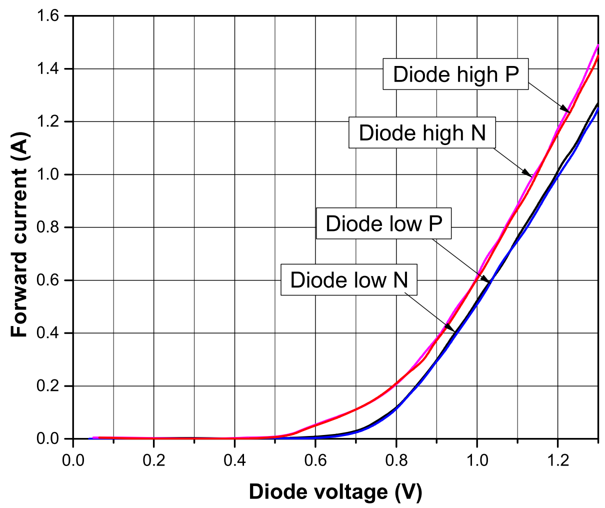
Table 17 gives a list transient, protective devices which are recommended for use with the ST-PLC-AFE.

Table 17. List of recommended, transient, protective devices

<table>
<tr><th>Component</th><th>Description</th><th>Manufacturer</th><th>P/N</th></tr>
<tr><td>D1</td><td>Zener diode</td><td>—</td><td>—</td></tr>
<tr><td>D2, D3, D4, D5</td><td>Schottky diode</td><td rowspan="3">STMicroelectronics</td><td>STPS3L40S</td></tr>
<tr><td>TVS, single-ended configuration</td><td rowspan="2">Transient voltage suppressor</td><td>SM6T6V8CA</td></tr>
<tr><td>TVS, differential-ended configuration</td><td>SM6T12CA</td></tr>
<tr><td>MOV</td><td>Metal oxyde varistor</td><td>Bourns</td><td>MOV-20D431K</td></tr>
</table>

In addition to external, protective circuits, the PAs integrate robust ESD diodes at their output which help to protect the ST-PLC-AFE against over-voltages (*Figure 48*).

Figure 49. ESD diode characteristics at the PA output



1. Diode high P: diode between PA_V_{DD} and positive PA output
2. Diode high N: diode between PA_V_{DD} and negative PA output
3. Diode low P: diode between GND and positive PA output
4. Diode low N: diode between GND and negative PA output

10.5 Application schematics

Figure 50. Application schematic, differential-ended coupling mode

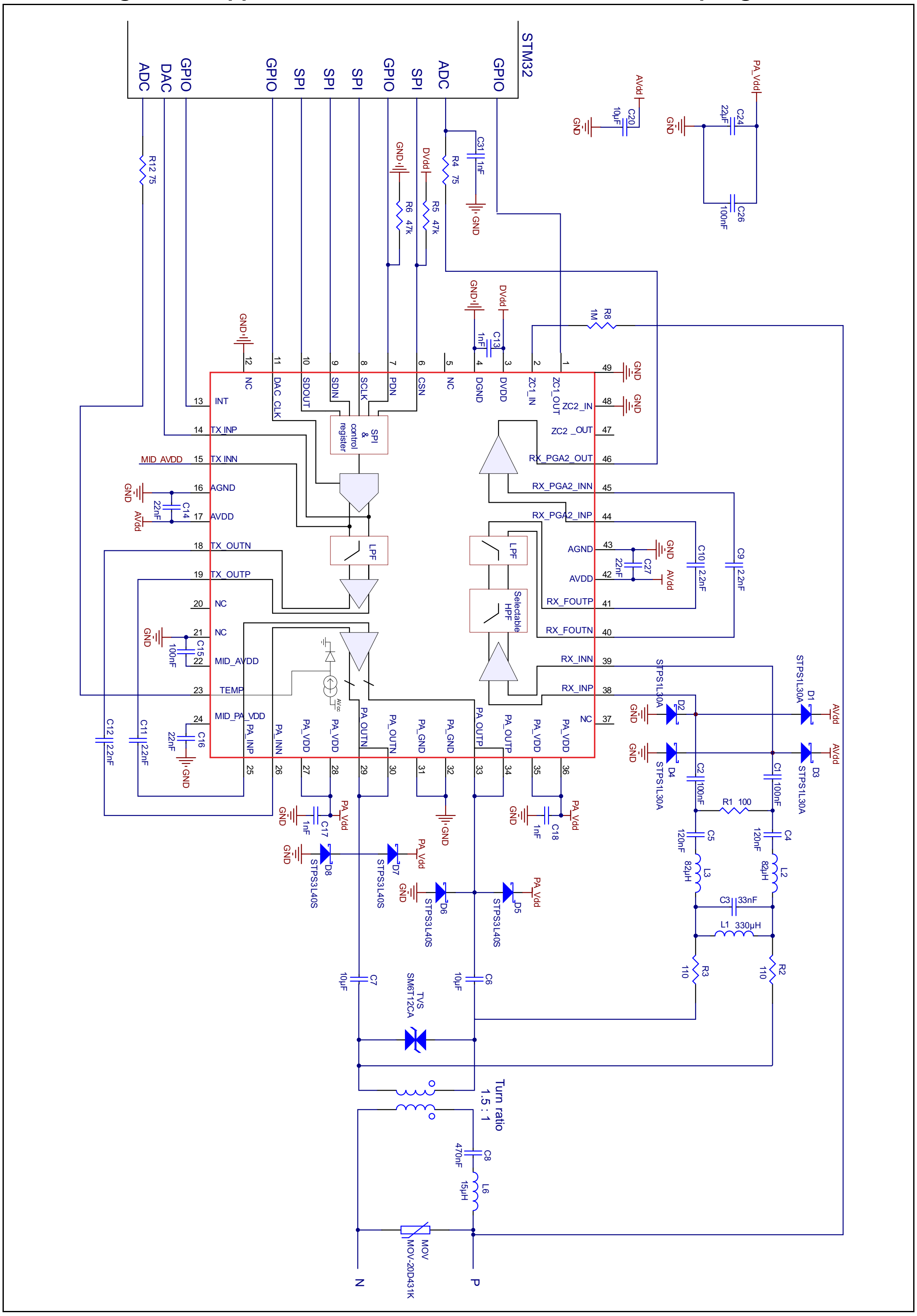
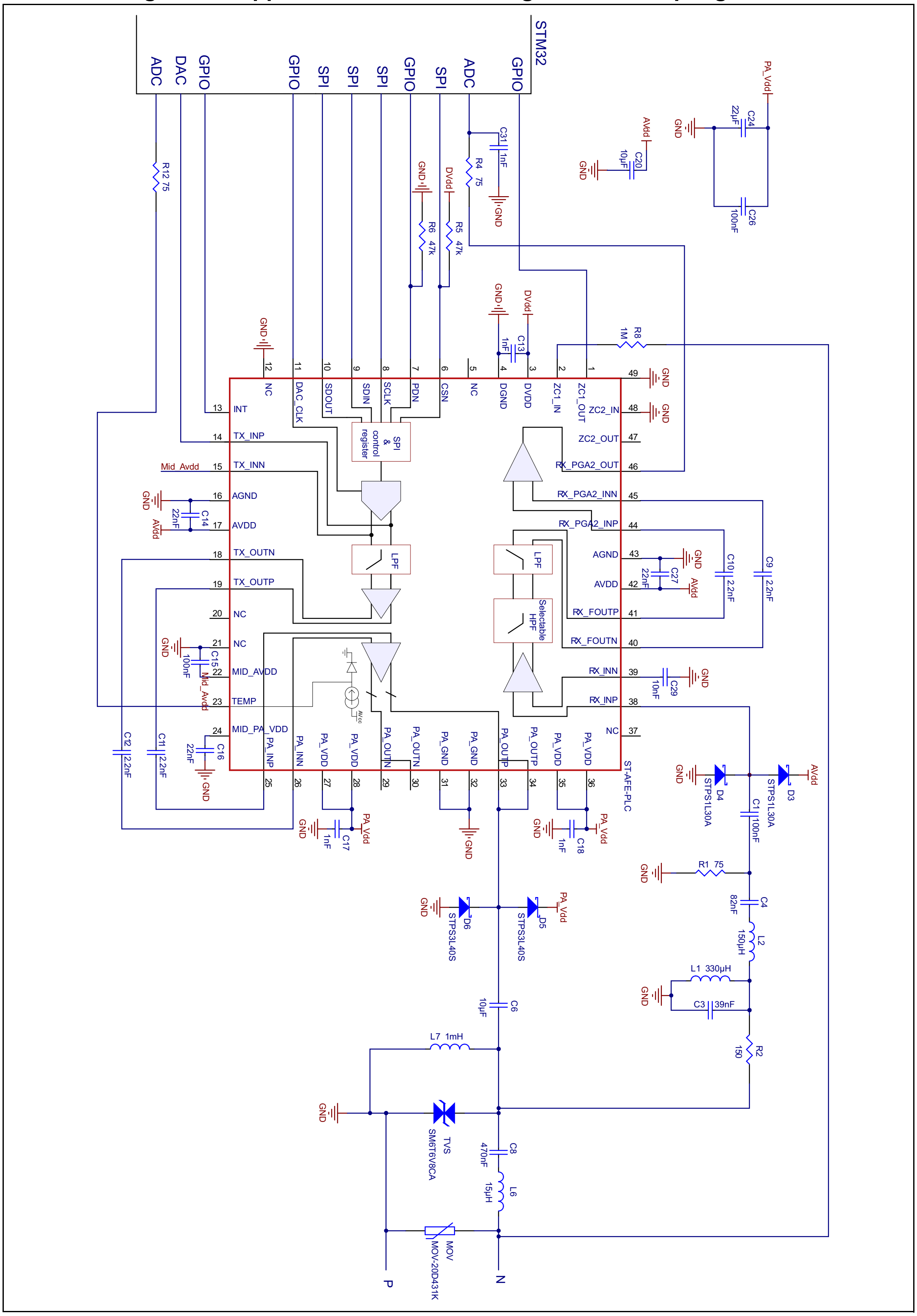


Figure 51. Application schematic, single-ended coupling mode



10.6 Bill of materials (BOM)

Table 18. BOM for differential-ended mode configuration

Description	Designator	Quantity	Value/PN	Comment
AFE smart metering	ST-AFE-PLCTR	1	ST_PLC_AFE	QFN48 package
Capacitor	C1, C2, C15, C26	4	100 nF	
	C3	1	33 nF	
	C4, C5	2	120 nF	
	C6, C7, C20	3	10 µF	
	C9, C10, C11, C12	4	2.2 nF	
	C13, C17, C18, C31	4	1 nF	
	C14, C16, C27	3	22 nF	
	C24	1	22 µF	
Schottky diode	D1, D2, D3, D4	4	STPS1L30A	STMicroelectronics, SMA package
	D5, D6, D7, D8	4	STPS3L40S	
Inductance	L1	1	330 µH	
	L2, L3	2	82 µH	
Transformer		1		Turn ratio 1.5:1
Resistor	R1	1	100	
	R2, R3	2	110	
	R4, R12	2	75	
	R5, R6	2	47 kΩ	
	R8	1	1 MΩ	
Transient voltage suppressor	TVS	1	SM6T12CA	STMicroelectronics, SMB package
Metal oxyde varistor	MOV	1		Coupling to the main
Capacitor	C8	1	470 nF	
Inductance	L6	1	15 µH	

Table 19. BOM for single-ended mode configuration

Description	Designator	Quantity	Value/PN	Comment
AFE smart metering	ST-AFE-PLCTR	1	ST_PLC_AFE	QFN48 package
Capacitor	C1, C15, C26	3	100 nF	
	C3	1	39 nF	
	C4	1	82 nF	
	C6, C20	2	10 µF	
	C9, C10, C11, C12	4	2.2 nF	
	C13, C17, C18, C31	4	1 nF	
	C14, C16, C27	3	22 nF	
	C24	1	22 µF	
	C29	1	10 nF	
Schottky diode	D3, D4	2	STPS1L30A	STMicroelectronics, SMA package
	D5, D6	2	STPS3L40S	
Inductance	L1	1	330µH	
	L2	1	150 µH	
	L7	1	1 mH	
Resistor	R1, R4, R12	3	75	
	R2	1	150	
	R5, R6	2	47 kΩ	
	R8	1	1 MΩ	
Transient voltage suppressor	TVS	1	SM6T6V8CA	STMicroelectronics, SMB package
Metal oxyde varistor	MOV	1		Coupling to the main
Capacitor	C8	1	470 nF	
Inductance	L6	1	15 µH	

10.7 ST-PLC-AFE consumption (no load)

Table 20. Power consumption matrix

<table>
<tr><th colspan="6">Register bits</th><th></th><th></th><th></th></tr>
<tr><th>TX_EN</th><th>RX_EN</th><th>PA_EN</th><th>PA2_EN</th><th>DAC_EN</th><th>HP_filter EN</th><th>AVDD</th><th>DVDD</th><th>PA_VDD</th></tr>
<tr><td rowspan="4">1</td><td rowspan="4">0</td><td rowspan="3">1</td><td rowspan="2">1</td><td>1</td><td rowspan="5">0</td><td>2.9 mA</td><td>130 µA</td><td>60 mA</td></tr>
<tr><td rowspan="6">0</td><td>2.1 mA</td><td>130 µA</td><td>60 mA</td></tr>
<tr><td rowspan="5">0</td><td>2.1 mA</td><td>130 µA</td><td>31 mA</td></tr>
<tr><td rowspan="4">0</td><td>1.8 mA</td><td>130 µA</td><td>23 µA</td></tr>
<tr><td rowspan="3">0</td><td rowspan="2">1</td><td>2.8 mA</td><td>130 µA</td><td>23 µA</td></tr>
<tr><td>1</td><td>3.4 mA</td><td>130 µA</td><td>23 µA</td></tr>
<tr><td>0</td><td>0</td><td>590 µA</td><td>130 µA</td><td>23 µA</td></tr>
</table>

10.8 Zero crossing detector

The ST-PLC-AFE integrates two zero crossing detectors which are used to detect when the mains signal crosses 0 V. Such information is used to ensure that the device is properly synchronized while it is communicating on the power lines.

Figure 52 shows the signal behavior when an AC main signal is applied on the zero crossing input pin of the device with an in-series resistor of 1 MΩ. The AC main voltage in this example is 220 V at 50Hz. The zero crossing detector behaves similarly when 110 V of AC voltage is applied at 60 Hz.

Figure 52. Zero crossing detector with 220 V AC main signal

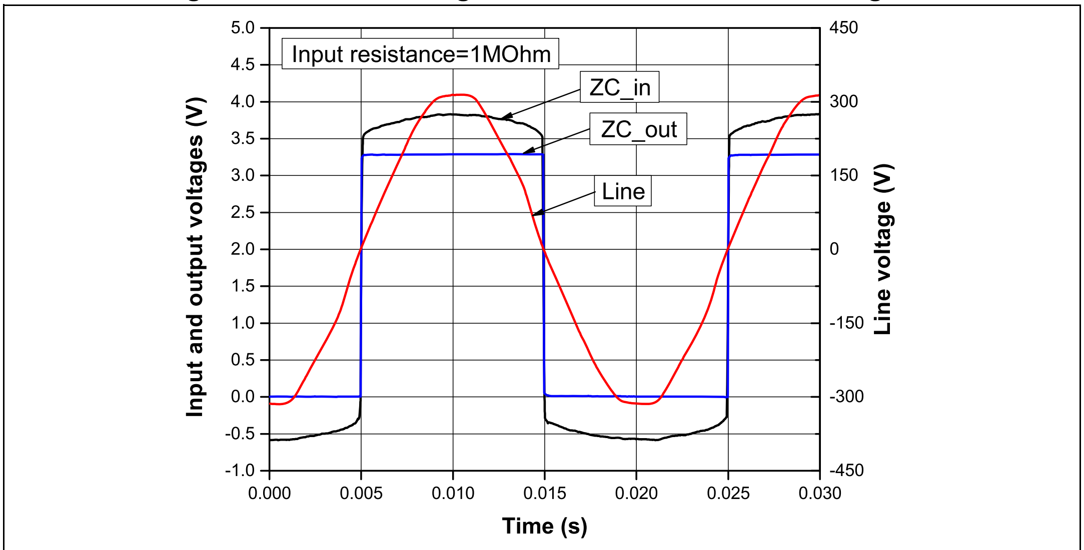
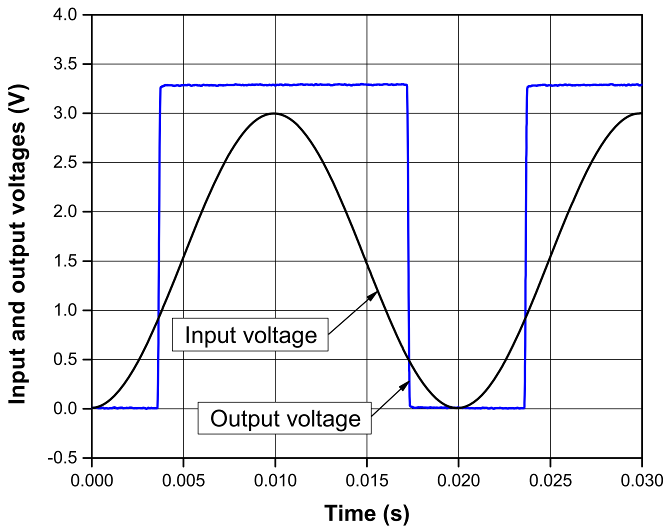


Figure 53 shows the zero crossing detector threshold voltages. To avoid unwanted toggling, this block integrates an in-built hysteresis.

Figure 53. Zero crossing detector threshold voltages



10.9 PCB layout recommendations

For optimized performance, it is recommended to follow the advice below:

- Minimize track length to have low-inductance connections to ground pins.
- Place bypass capacitors as close as possible to all VDD connections.
- Keep the ground plane as homogeneous as possible by adding through-hole vias on the PCB. This helps to have the same reference voltage at each point of the PCB by minimizing parasitic ground inductance due to ground-current return paths.
- Limit the number of tracks that cut the ground plane dissipation because tracks running parallel to the ST-PLC-AFE limit power dissipation. It is recommended to have tracks that are orthogonal to the device.

10.10 Power-line demonstration and development kit

A full demonstration board and development kit is available for evaluation. Please contact the STMicroelectronic sales office for tool access.

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

11.1 QFN48 package information

Figure 54. QFN48 package outline

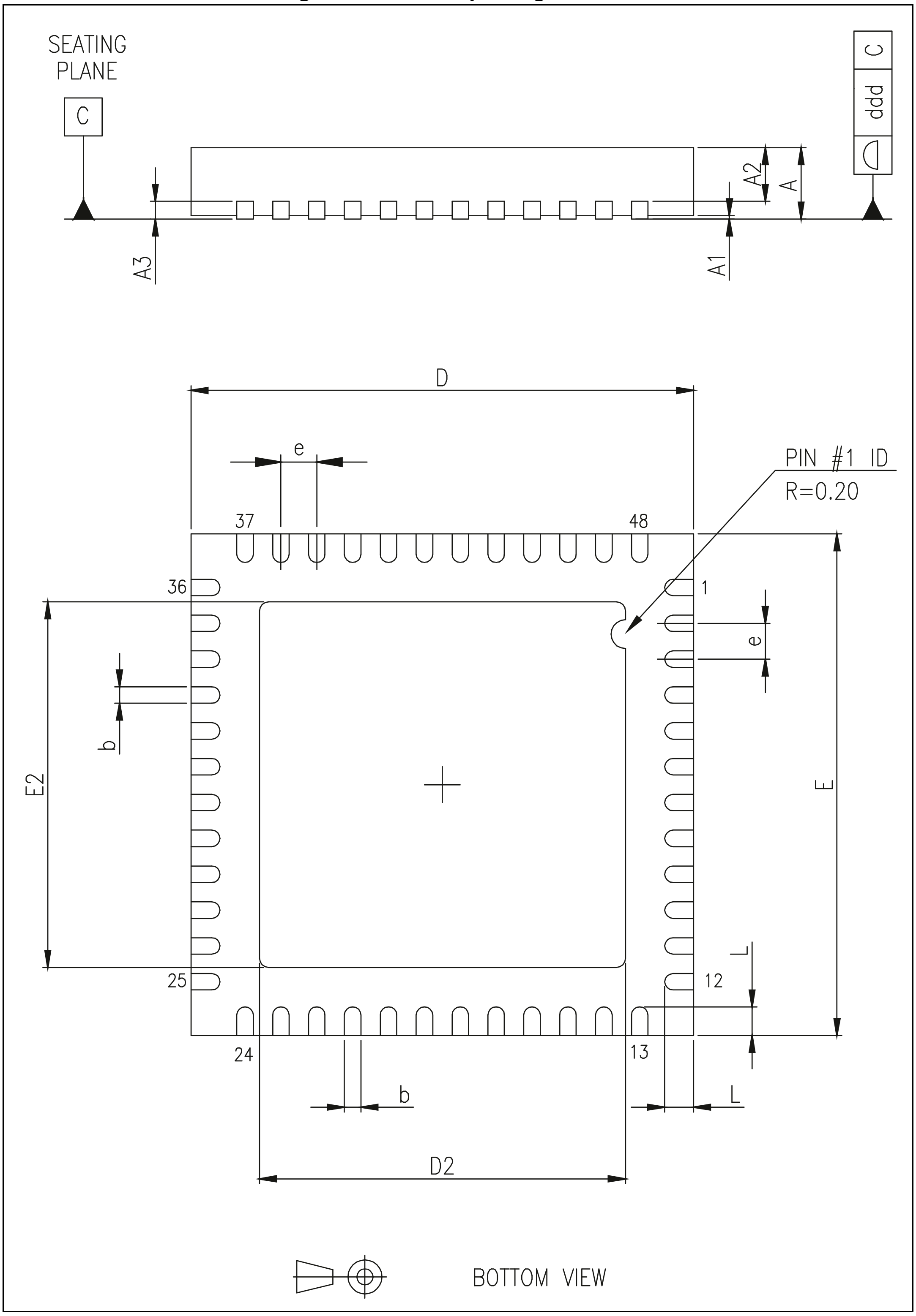


Table 21. QFN48 mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.75	0.85	0.95	0.030	0.033	0.037
A1		0.02	0.05		0.001	0.002
A2		0.65	0.70		0.026	0.028
A3		0.20			0.008	
b	0.2	0.25	0.30	0.008	0.010	0.012
D	6.85	7.00	7.15	0.270	0.276	0.281
D2	3.95	4.10	4.25	0.156	0.161	0.167
E	6.85	7.00	7.15	0.270	0.276	0.281
E2	3.95	4.10	4.25	0.156	0.161	0.167
e	0.45	0.50	0.55	0.018	0.020	0.022
L	0.35	0.40	0.45	0.014	0.016	0.018
ddd			0.08			0.003

12 Ordering information

Table 22. Order codes

Order code	Temperature range	Package	Packing	Marking
ST-PLC-AFETR	40 °C to 125 °C, extended junction temperature range	QFN48 exposed PAD	Bulk quantity 2500	PLC_AFE

13 Revision history

Table 23. Document revision history

Date	Revision	Changes
01-Feb-2016	1	Initial release