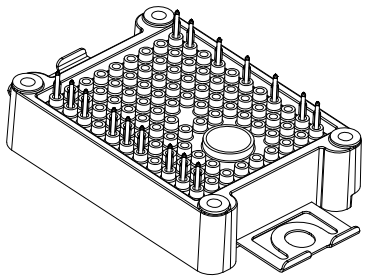
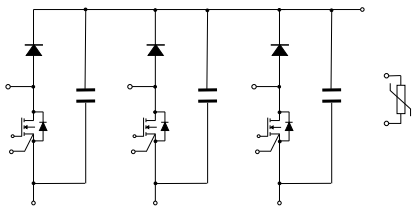
A1TB45W65M5-FC

Datasheet

ACEPACK 1 power module, boost topology 650 V, MDmesh M5 Power MOSFETs with SiC diode and NTC



ACEPACK 1



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Features

- ACEPACK 1 power module
  - UL certified 2.5 kV insulation voltage
  - Press fit contact pins
  - Integrated DC link capacitor
- Triple boost topology
  - 650 V MDmesh M5 Power MOSFETs
  - 650 V, 1.45 V, Power Schottky SiC diode
- Integrated NTC temperature sensor

Applications

- Battery charger
- UPS
- Solar applications

Description

This ACEPACK 1 power module realizes a triple boost topology with three DC link capacitors and NTC that integrates three 650 V M5 Power MOSFETs and three SiC power Schottky diodes, all from STMicroelectronics.

This product is suitable as an AC-DC stage of battery management and in any UPS systems.

Product status link
A1TB45W65M5-FC

Product summary	
Order code	A1TB45W65M5-FC
Marking	A1TB45W65M5-FC
Package	ACEPACK 1
Leads type	Press fit
Packing	Tray

1 Electrical ratings

T_J = 25 °C unless otherwise specified.

1.1 MOSFET

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	650	V
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 100 °C	25	A
I_{DM}	Drain current (pulsed)	100	A
dv/dt(1)	Peak diode recovery voltage slope	15	V/ns
dv/dt(2)	MOSFET dv/dt ruggedness	50	V/ns
P_{TOT}	Total power dissipation at T_C = 25 °C	250	W
T_J	Maximum junction temperature	150	°C
T_{Jop}	Operating junction temperature range	-40 to 150	°C

1. *I_{SD}≤ 58 A, di/dt = 400 A/µs, V_{DS} (peak)< $V_{(BR)DSS}$, V_{DD} = 400 V (from discrete device characterization).*
2. *V_{DS}≤ 520 V (from discrete device characterization).*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case (each MOSFET)	0.5	°C/W

Table 3. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 25 A		52	68	mΩ
		V_{GS} = 10 V, I_D = 25 A T_C=150 °C		114		
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1 mA	3	4	5	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C (1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V		6420		pF
C_{oss}	Output capacitance			170		pF
C_{rss}	Reverse transfer capacitance			11		pF
$C_{o(tr)}$(2)	Equivalent output capacitance time related	V_{GS} = 0 V, V_{DS} = 0 to 520 V		536		pF
$C_{o(er)}$(3)	Equivalent output capacitance energy related			146		pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain		1.3		Ω
Q_g	Total gate charge	V_{CC} = 520 V, I_D = 25 A, V_{GS} = 10 V		143		nC
Q_{gs}	Gate-emitter charge			38		nC
Q_{gd}	Gate-collector charge			64		nC

1. *Defined by design, not subject to production test.*
2. *$Co_{(tr)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
3. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*

1.2 SiC Schottky diode

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{RRM}	Repetitive peak reverse voltage	650	V
T_J	Maximum junction temperature	150	°C
T_{Jop}	Operative junction temperature range	-40 to 150	°C

Table 5. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case (each diode)	1.65	°C/W

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_F	Forward voltage drop	I_F = 20 A	T_J = 25 °C	-	1.35	-	V
			T_J = 150 °C	-	1.49	-	
I_R	Reverse leakage current	V_R = 650 V	T_J = 25 °C	-	30	-	µA
			T_J = 150 °C	-	280	-	

1.3 DC link capacitor

Table 7. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{MAX}	Maximum DC voltage	630	V
T_{Jop}	Operative junction temperature range	-40 to 150	°C

Table 8. Electrical characteristics

Symbol	Parameter	Value	Unit
C	Capacitance value	47	nF
	Tolerance	±10	%

1.4 NTC (B57451V5103G362)

Table 9. Absolute maximum ratings for NTC temperature sensor, considered as stand-alone

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{25}	Resistance rating	T = 25 °C		10		kΩ
$\Delta R_{25}/R$	Resistance tolerance		-2		+2	%
R_{100}	Resistance rating	T = 100 °C		674.8		Ω
$\Delta R_{100}/R$	Resistance tolerance		-4.75		4.75	%
$R_{25/50}$	B-value	T=25 °C to 50 °C		3940		K
$R_{25/85}$		T=25 °C to 85 °C		3980		
$R_{25/100}$		T=25 °C to 100 °C (±1%)		4000		
T	Operating temperature range		-40		150	°C

Figure 1. NTC typical resistance vs temperature

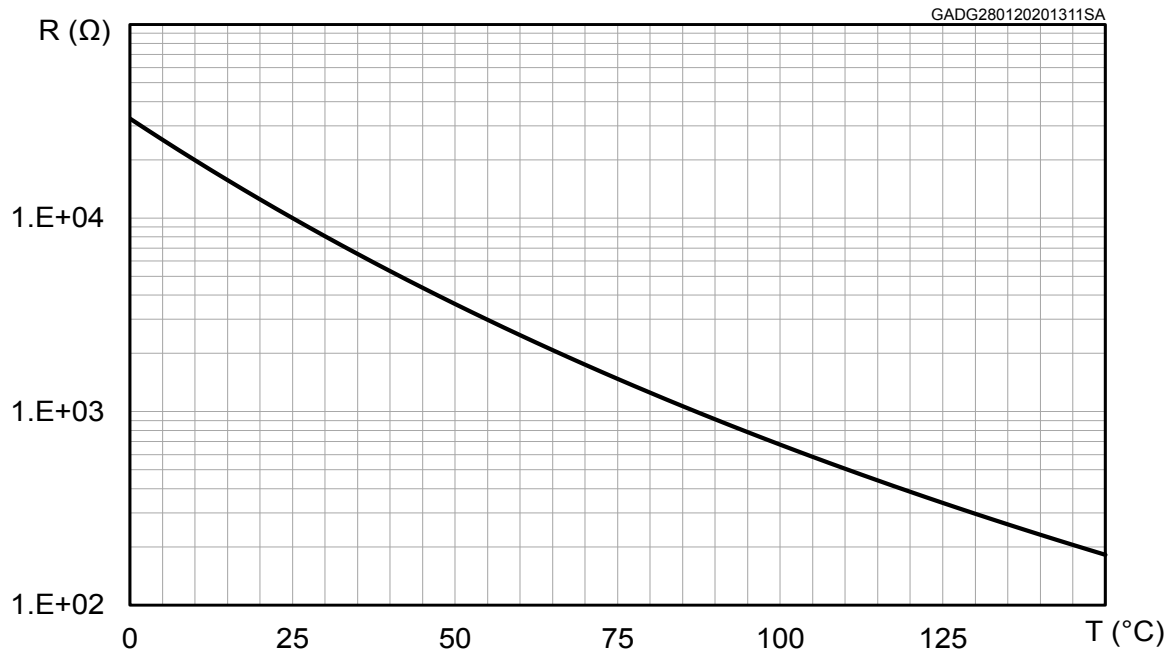
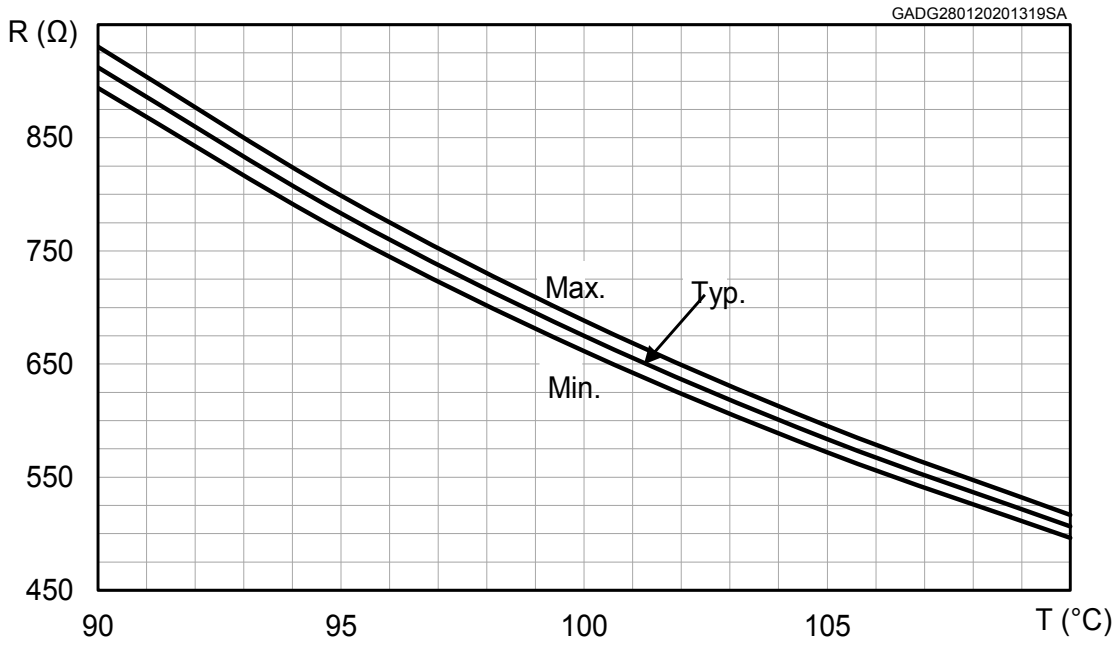


Figure 2. **NTC resistance vs temperature, zoom**



1.5 Package

Table 10. **Absolute maximum ratings for ACEPACK 1 package**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{isol}	Isolation voltage (AC voltage t = 60 s)		-	2.5	kV
T_{stg}	Storage temperature range	-40	-	125	°C

2 Electrical characteristics (curves)

Figure 3. Power MOSFET maximun transient thermal impedance

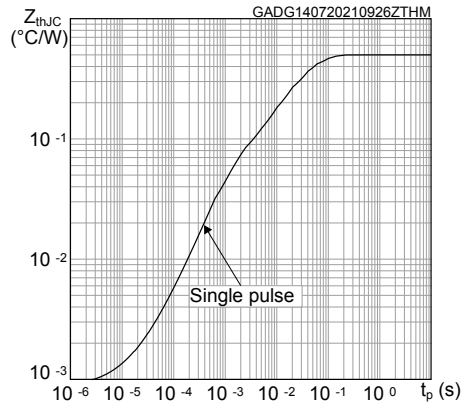


Figure 4. Boost diode maximun transient thermal impedance

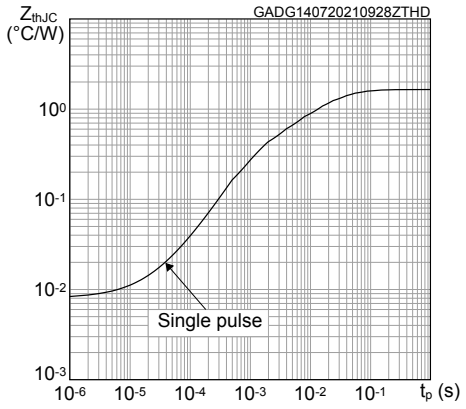


Figure 5. Power MOSFET typical output characteristics

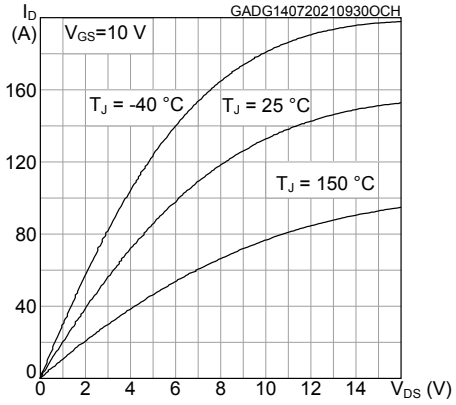


Figure 6. Power MOSFET typical transfer characteristics

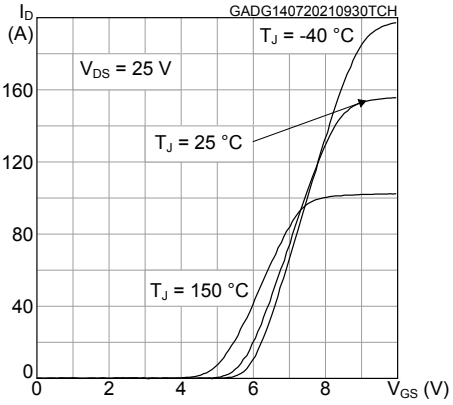
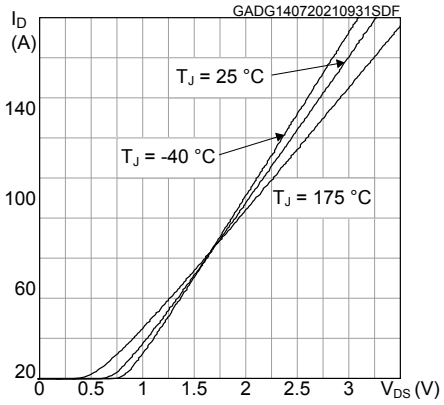


Figure 7. Boost diode typical forward charactheristics



3 Electrical topology and pin description

Figure 8. **Electrical topology and pin description**

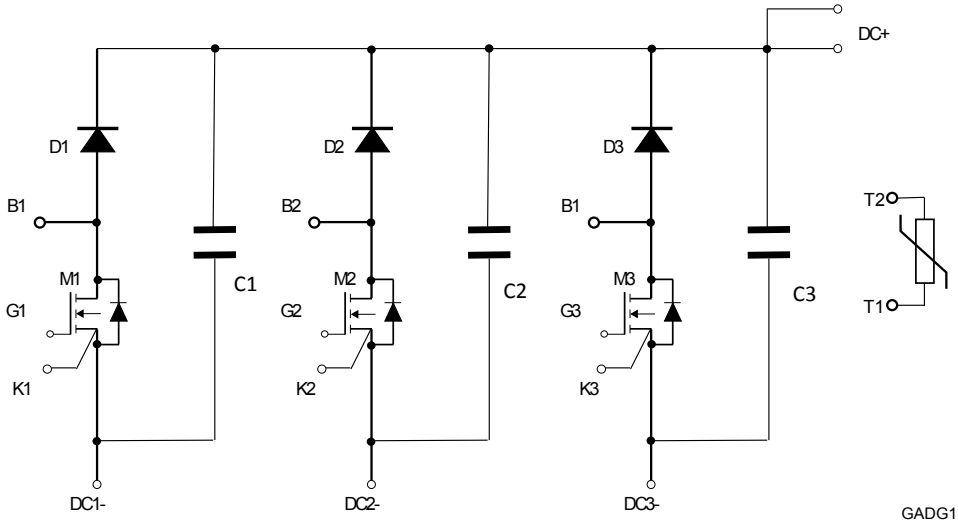


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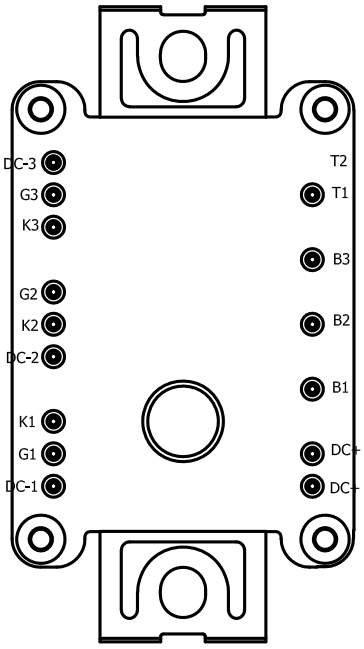
Figure 9. **Package top view with pinout**



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 ACEPACK 1 triple boost press fit package information

Figure 10. ACEPACK 1 triple boost press fit package outline (dimensions are in mm)

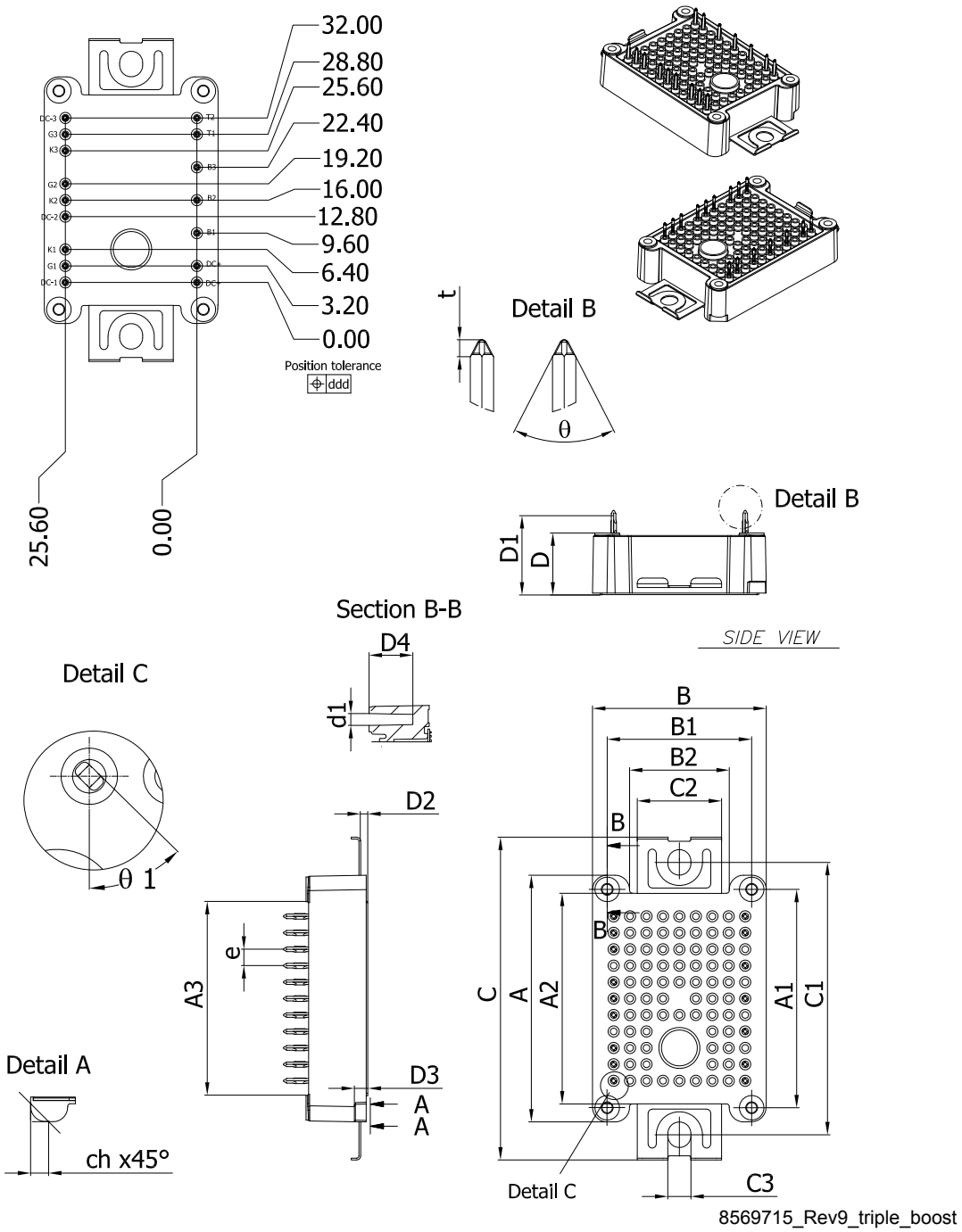
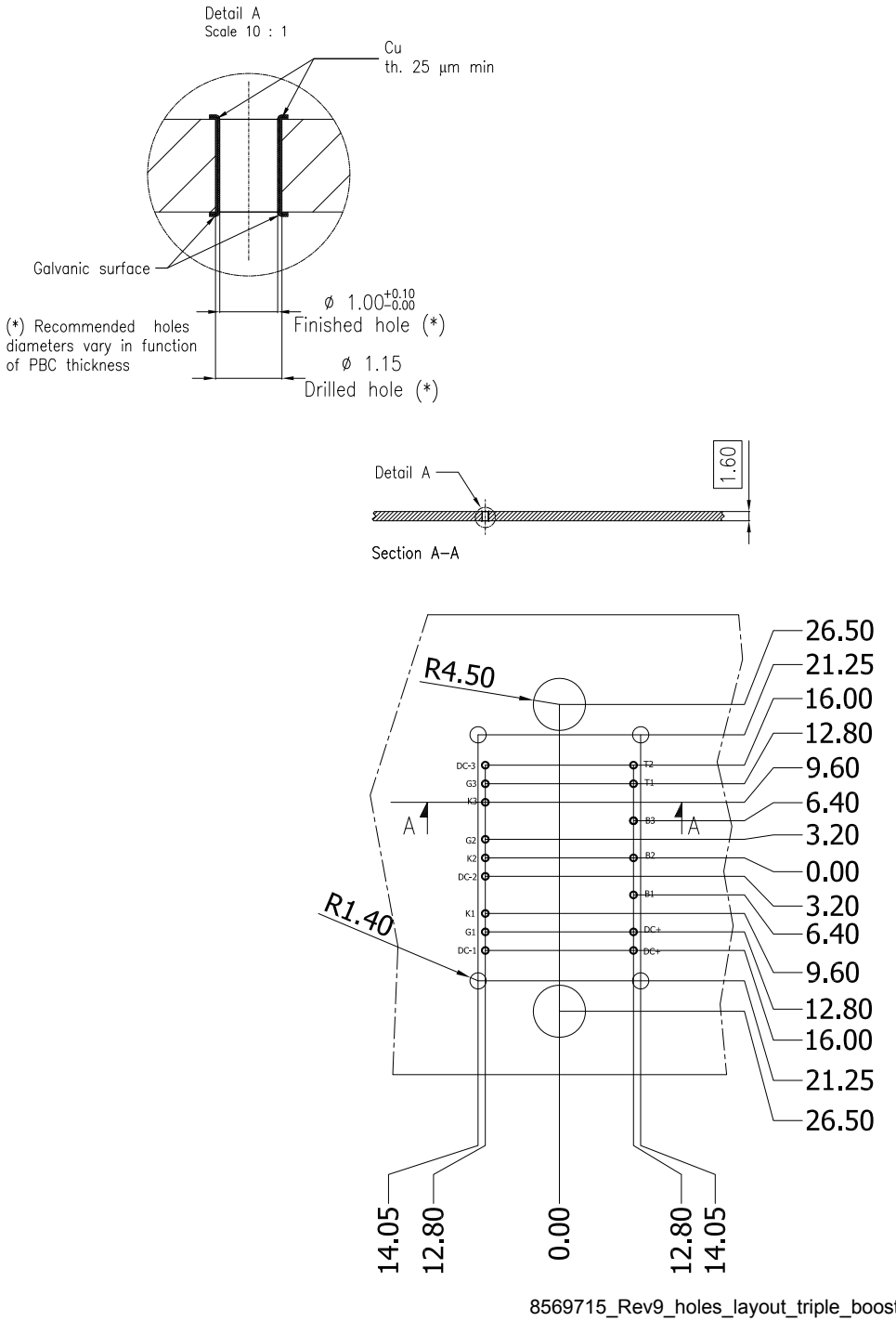


Table 11. ACEPACK 1 triple boost press fit package mechanical data

Ref.	mm		
	Min.	Typ.	Max.
A	47.70	48.00	48.30
A1	42.30	42.50	42.70
A2	40.80	41.00	41.20
A3		36.80 REF	
B	33.50	33.80	34.10
B1	27.90	28.10	28.30
B2	19.20	19.40	19.60
C	62.30	62.80	63.30
C1	52.90	53.00	53.10
C2	16.20	16.40	16.60
C3	4.40	4.50	4.60
D	11.65	12.00	12.35
D1	15.90	16.40	16.90
D2	1.10	1.30	1.50
D3	2.30	2.50	2.70
D4			8.50
t	0.30	0.40	0.50
θ	52°	60°	68°
θ1		45°	
ddd		0.40	
e		3.20 BSC	
d1		2.30 REF	
ch		3.50 REF	

Figure 11. ACEPACK 1 triple boost press fit PCB holes layout (dimensions are in mm)



8569715_Rev9_holes_layout_triple_boost_press_fit

Revision history

Table 12. **Document revision history**

Date	Revision	Changes
30-Jul-2021	1	First release.

Contents