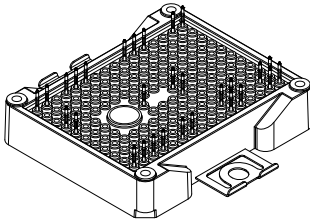
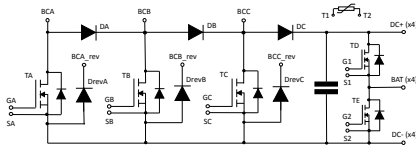


## ACEPACK 2 power module, triple boost (650 V, 49 mΩ typ.) plus half-bridge topology (650 V, 23.5 mΩ typ.) SiC Power MOSFET gen. 3 with NTC and capacitance



ACEPACK 2



### Features

- ACEPACK 2 power module
  - Triple boost switch 49 mΩ of typical  $R_{DS(on)}$
  - Half-bridge switch 23.5 mΩ of typical  $R_{DS(on)}$
  - Insulation voltage 2.5 kVrms
  - Integrated NTC temperature sensor
  - Integrated DC link capacitor
  - DBC Cu-Al<sub>2</sub>O<sub>3</sub>-Cu based
  - Press-fit contact pins

### Application

- DC-DC converters
- Solar inverters

### Description

This power module realizes a triple boost plus half-bridge topology in an ACEPACK 2 module with NTC and capacitance, integrating the latest advances in silicon carbide MOSFETs from STMicroelectronics, represented by third generation technology. This modular solution is used to realize complex topologies with very high power density and efficiency requirements.



#### Product status link

[A2TBH45M65W3-FC](#)

#### Product summary

Order code	A2TBH45M65W3-FC
Marking	A2TBH45M65W3-FC
Package	ACEPACK 2
Leads type	Press-fit
Packing	Tray

# 1 SiC MOSFET (TA, TB, TC)

$T_J = 25\text{ °C}$  unless otherwise specified.

**Table 1. Absolute maximum ratings (TA, TB, TC)**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	650	V
$V_{GS}$	Gate-source voltage	-10 to 22	V
	Gate-source voltage, recommended operating values	-5 to 18	
$I_D$	Drain current (continuous) at $T_H = 25\text{ °C}$	28	A
$I_{DM}$	Peak pulsed drain current at $t_p = 1\text{ ms}$	78	A
$T_J$	Maximum junction temperature	150	°C
	Operating junction temperature range under switching conditions	-40 to 150	

**Table 2. Thermal data (TA, TB, TC)**

Symbol	Parameter	Value	Unit
$R_{thJH}$	Thermal resistance, junction-to-heat sink, each switch (TIM = 120 $\mu\text{m}$ , $\lambda = 3\text{ W}\cdot\text{m}^{-1}\cdot\text{°C}^{-1}$ )	1.98	°C/W

**Table 3. On/off state (TA, TB, TC)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 18\text{ V}$ , $I_D = 15\text{ A}$		49	72	m $\Omega$
		$V_{GS} = 18\text{ V}$ , $I_D = 15\text{ A}$ , $T_J = 150\text{ °C}$		64		
$V_{GS(th)}$	Gate threshold voltage	$I_D = 5\text{ mA}$ , $V_{DS} = V_{GS}$	1.85	3.10	4.2	V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$			10	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0$ , $V_{GS} = -10\text{ to }22\text{ V}$			$\pm 100$	nA
$C_{iss}$	Input capacitance			920		pF
$C_{oss}$	Output capacitance	$f = 1\text{ MHz}$ , $V_{DS} = 400\text{ V}$ , $V_{GS} = 0\text{ V}$		94		pF
$C_{riss}$	Reverse transfer capacitance			13		pF
$Q_g$	Total gate charge				39.5	
$Q_{gs}$	Gate-source charge	$V_{DS} = 400\text{ V}$ , $V_{GS} = -5\text{ to }18\text{ V}$ , $I_D = 20\text{ A}$		11.5		nC
$Q_{gd}$	Gate-drain charge			14.5		nC

**Table 4. Switching energy (TA, TB, TC)**

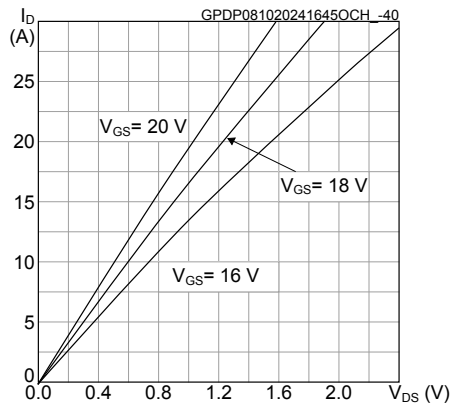
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
dv/dt	On	$V_{DS} = 400\text{ V}$ , $I_D = 15\text{ A}$ , $R_G = 4.7\text{ }\Omega$ ,	-	42.2	-	V/ns
	Off	$V_{GS} = -5\text{ to }18\text{ V}$	-	46	-	

**Table 5. Source-drain diode (TA, TB, TC)**

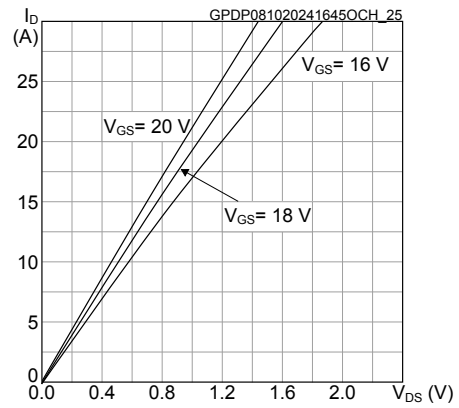
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}$	Forward on voltage drop	$V_{GS} = 0\text{ V}$ , $I_{SD} = 15\text{ A}$	-	2.8	-	V

## 1.1 Electrical characteristics diagrams (TA, TB, TC)

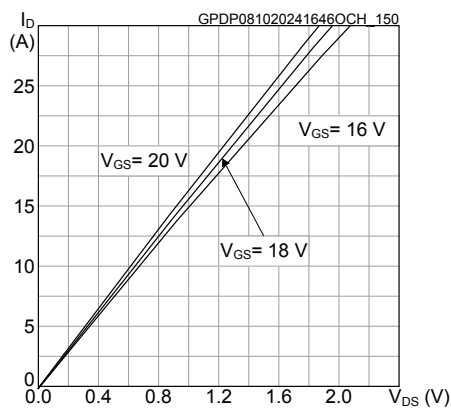
**Figure 1. Typical output characteristics,  $T_J = -40\text{ }^\circ\text{C}$  (TA, TB, TC)**



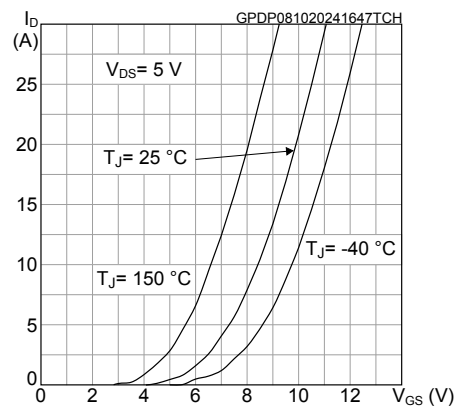
**Figure 2. Typical output characteristics,  $T_J = 25\text{ }^\circ\text{C}$  (TA, TB, TC)**



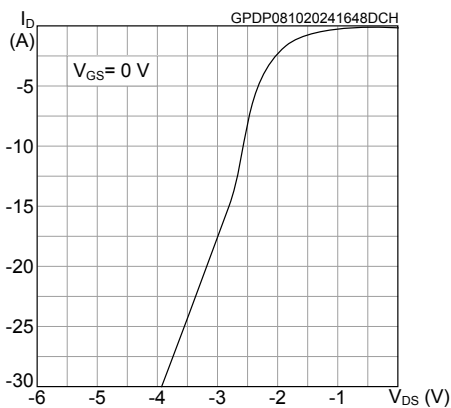
**Figure 3. Typical output characteristics,  $T_J = 150\text{ }^\circ\text{C}$  (TA, TB, TC)**



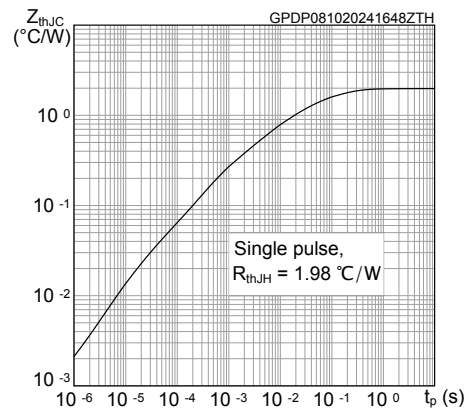
**Figure 4. Typical transfer characteristics (TA, TB, TC)**



**Figure 5. Typical diode characteristics, terminal (TA, TB, TC)**



**Figure 6. Maximum transient thermal impedance (TA, TB, TC)**



## 2 SiC MOSFET (TD, TE)

$T_J = 25\text{ °C}$  unless otherwise specified.

**Table 6. Absolute maximum ratings (TD, TE)**

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	650	V
$V_{GS}$	Gate-source voltage	-10 to 22	V
	Gate-source voltage, recommended operating values	-5 to 18	
$I_D$	Drain current (continuous) at $T_H = 25\text{ °C}$	52	A
$I_{DM}$	Peak pulsed drain current at $t_p = 1\text{ ms}$	157	A
$T_J$	Operating junction temperature range	-55 to 150	°C
$T_{stg}$	Storage temperature range		°C

**Table 7. SiC diode thermal data (TD, TE)**

Symbol	Parameter	Value	Unit
$R_{thJH}$	Thermal resistance, junction-to-heat sink, each switch (TIM = 120 $\mu\text{m}$ , $\lambda = 3\text{ W}\cdot\text{m}^{-1}\cdot\text{°C}^{-1}$ )	1.21	°C/W

**Table 8. SiC MOSFET on/off states (TD, TE)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 18\text{ V}$ , $I_D = 30\text{ A}$	-	23.5	35	m $\Omega$
		$V_{GS} = 18\text{ V}$ , $I_D = 30\text{ A}$ , $T_J = 150\text{ °C}$	-	28		
$V_{GS(th)}$	Gate threshold voltage	$I_D = 10\text{ mA}$ , $V_{DS} = V_{GS}$	1.8	3.1	4.2	V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$	-		20	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0$ , $V_{GS} = -10\text{ to }22\text{ V}$	-		$\pm 100$	nA
$C_{iss}$	Input capacitance	$f = 1\text{ MHz}$ , $V_{DS} = 400\text{ V}$ , $V_{GS} = 0\text{ V}$	-	1840		pF
$C_{oss}$	Output capacitance		-	188		pF
$C_{rSS}$	Reverse transfer capacitance		-	26		pF
$Q_g$	Total gate charge	$V_{DD} = 400\text{ V}$ , $V_{GS} = -5\text{ to }18\text{ V}$ , $I_D = 20\text{ A}$	-	79		nC
$Q_{gs}$	Gate-source charge		-	23		nC
$Q_{gd}$	Gate-drain charge		-	29		nC

**Table 9. SiC MOSFET switching energy (TD, TE)**

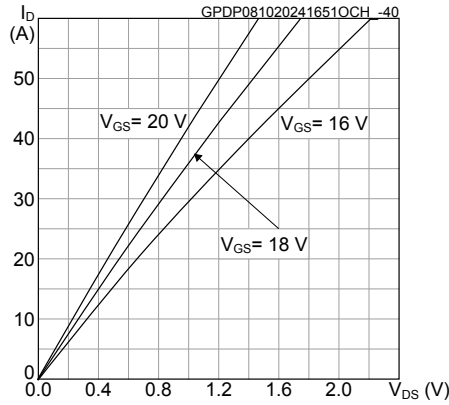
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
dv/dt	On	$V_{DD} = 400\text{ V}$ , $I_D = 15\text{ A}$ , $R_G = 4.7\text{ }\Omega$	-	23.8	-	V/ns
	Off	$V_{GS} = -5\text{ to }18\text{ V}$	-	252.1	-	

**Table 10. SiC MOSFET source-drain diode (TD, TE)**

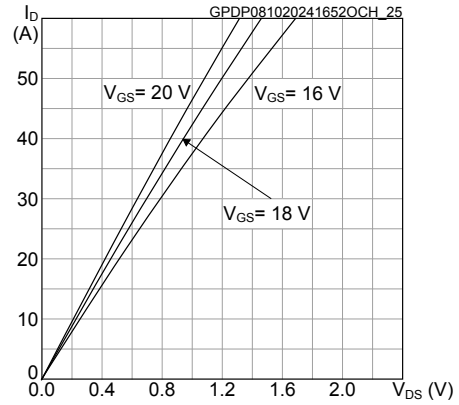
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}$	Forward on voltage drop	$V_{GS} = 0\text{ V}$ , $I_{SD} = 30\text{ A}$	-	2.8	-	V

## 2.1 Electrical characteristics diagrams (TD, TE)

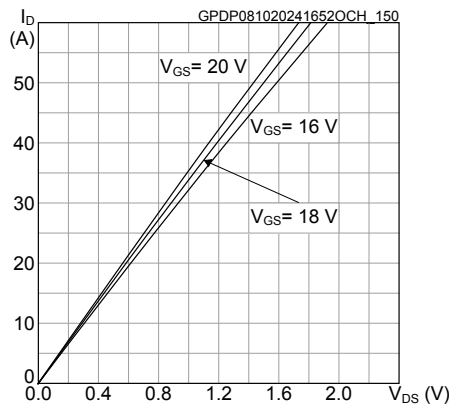
**Figure 7. Typical output characteristics,  $T_J = -40\text{ }^\circ\text{C}$  (TD, TE)**



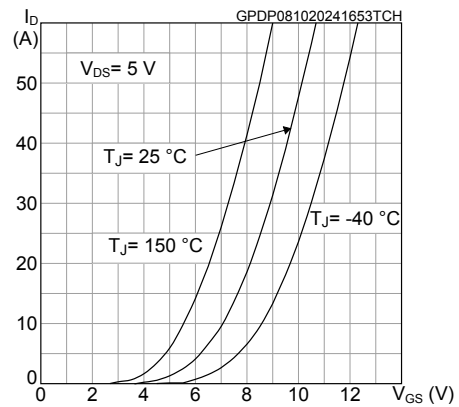
**Figure 8. Typical output characteristics,  $T_J = 25\text{ }^\circ\text{C}$  (TD, TE)**



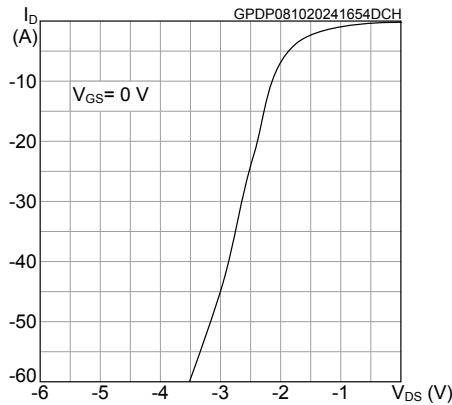
**Figure 9. Typical output characteristics,  $T_J = 150\text{ }^\circ\text{C}$  (TD, TE)**



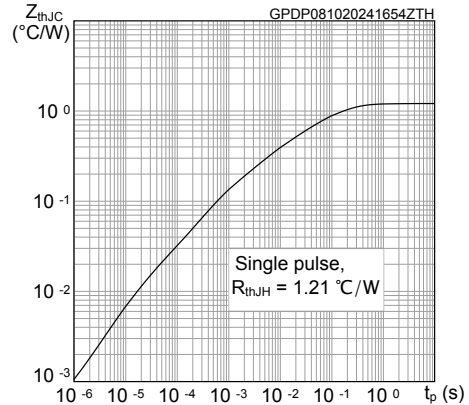
**Figure 10. Typical transfer characteristics (TD, TE)**



**Figure 11. Typical diode characteristics, terminal (TD, TE)**



**Figure 12. Maximum transient thermal impedance (TD, TE)**



### 3 SiC diode (DA, DB, DC)

$T_J = 25\text{ °C}$  unless otherwise specified.

**Table 11. Absolute maximum ratings (DA, DB, DC)**

Symbol	Parameter	Value	Unit
$V_{RRM}$	Repetitive peak reverse voltage	650	V
$I_{F(AV)}$	Forward surge current $T_H = 85\text{ °C}$	20	A
$T_J$	Maximum junction temperature	150	°C
	Operating junction temperature range under switching conditions	-40 to 150	

**Table 12. SiC diode thermal data (DA, DB, DC)**

Symbol	Parameter	Value	Unit
$R_{thJH}$	Thermal resistance, junction-to-heat sink, each switch (TIM = 120 $\mu\text{m}$ , $\lambda = 3\text{ W}\cdot\text{m}^{-1}\cdot\text{°C}^{-1}$ )	1.95	°C/W

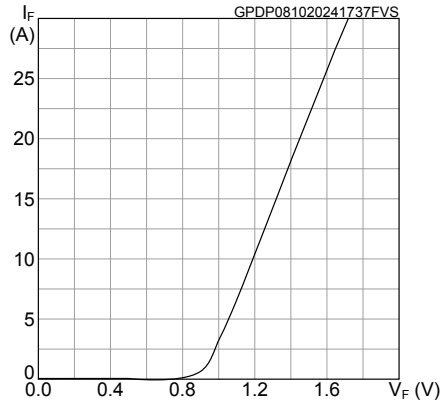
**Table 13. SiC diode electrical characteristic (DA, DB, DC)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_R$	Reverse leakage current	$V_R = V_{RRM}$	-	46	224	$\mu\text{A}$
		$V_R = V_{RRM}$ , $T_C = 150\text{ °C}$	-	230		
$V_F$	Forward voltage drop	$I_F = 20\text{ A}$	-	1.4		V
		$I_F = 20\text{ A}$ , $T_C = 150\text{ °C}$	-	1.6		
$Q_g$	Total capacitive charge	$V_R = 400\text{ V}$	-	70		nC
$C_J$	Total capacitance	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$	-	1400		pF
		$V_R = 400\text{ V}$ , $f = 1\text{ MHz}$	-	90		

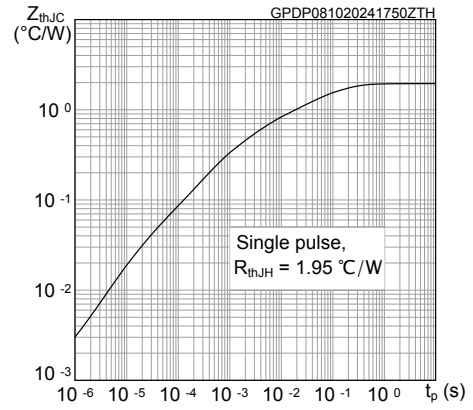


### 3.1 Electrical characteristics diagrams (DA, DB, DC)

**Figure 13. Typical forward voltage drop (DA, DB, DC)**



**Figure 14. Maximum transient thermal impedance (DA, DB, DC)**



## 4 Rectifier diode (Drev A, B, C)

$T_J = 25\text{ °C}$  unless otherwise specified.

**Table 14. Rectifier diode absolute maximum ratings (Drev A, B, C)**

Symbol	Parameter	Value	Unit
$V_{RRM}$	Repetitive peak reverse voltage from $T = -40\text{ °C}$ to $+175\text{ °C}$	800	V
$I_{F(RMS)}$	Forward RMS current	48	A
$T_J$	Maximum junction temperature	150	°C
	Operating junction temperature range under switching conditions	-40 to 150	

**Table 15. SiC diode thermal data (Drev A, B, C)**

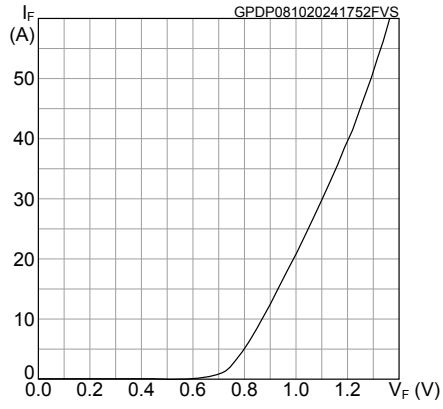
Symbol	Parameter	Value	Unit
$R_{thJH}$	Thermal resistance, junction-to-heat sink, each switch (TIM = 120 $\mu\text{m}$ , $\lambda = 3\text{ W}\cdot\text{m}^{-1}\cdot\text{°C}^{-1}$ )	1.67	°C/W

**Table 16. Rectifier diode electrical characteristic (Drev A, B, C)**

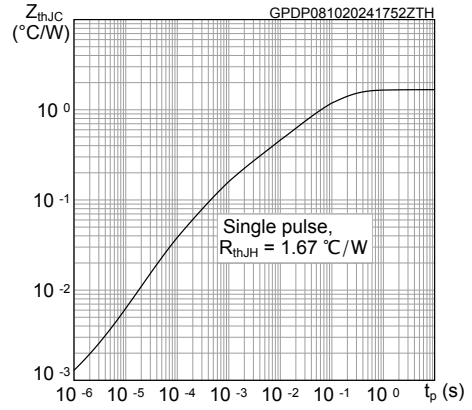
Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
$I_R$	Reverse leakage current	$T_J = 25\text{ °C}$	$V_R = V_{RRM}$	-		2	$\mu\text{A}$
		$T_J = 150\text{ °C}$		-	10	100	
$V_F$	Forward voltage drop	$T_J = 25\text{ °C}$	$I_F = 30\text{ A}$	-	1.1		V
		$T_J = 150\text{ °C}$		-	1		

### 4.1 Electrical characteristics diagrams (Drev A, B, C)

**Figure 15. Typical forward voltage drop (Drev A, B, C)**



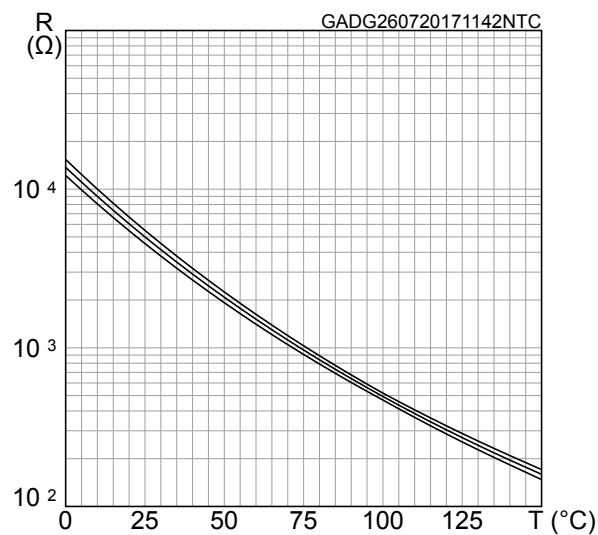
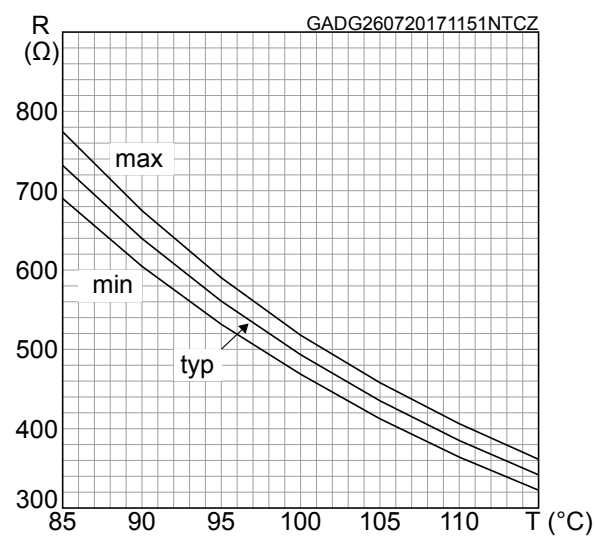
**Figure 16. Maximum transient thermal impedance (Drev A, B, C)**



## 5 NTC

**Table 17. Absolute maximum ratings for NTC temperature sensor, considered as stand-alone**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R <sub>25</sub>	Resistance rating	T = 25 °C		5		kΩ
R <sub>100</sub>	Resistance rating	T = 100 °C		493		Ω
ΔR <sub>100</sub> /R	Resistance tolerance		-5	5	%	
B	B value	T = 25 to 50 °C		3375		K
		T = 25 to 85 °C		3411		
T	Operating temperature range		-40		150	°C

**Figure 17. NTC typical resistance vs temperature**

**Figure 18. NTC resistance vs temperature, zoom**


## 6 DC link capacitor (C1210X473KDRACTU)

**Table 18. Absolute maximum rating for capacitor**

Symbol	Parameter	Value	Unit
V <sub>MAX</sub>	Maximum DC voltage	1000	V
C	Capacitance	47	nF
T	Operating temperature range	-40 to 125	°C

## 7 Package

Table 19. ACEPACK 2 package

Symbol	Parameter	Value	Unit
V <sub>ISO</sub>	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage, t = 60 s)	2.5	kVrms
CTI	Comparative tracking index	200	V
L <sub>s</sub>	Stray inductance module loop	10	nH
T <sub>stg</sub>	Storage temperature range	-40 to 125	°C

## 8 Electrical topology and pin description

Figure 19. Electrical topology and pin description

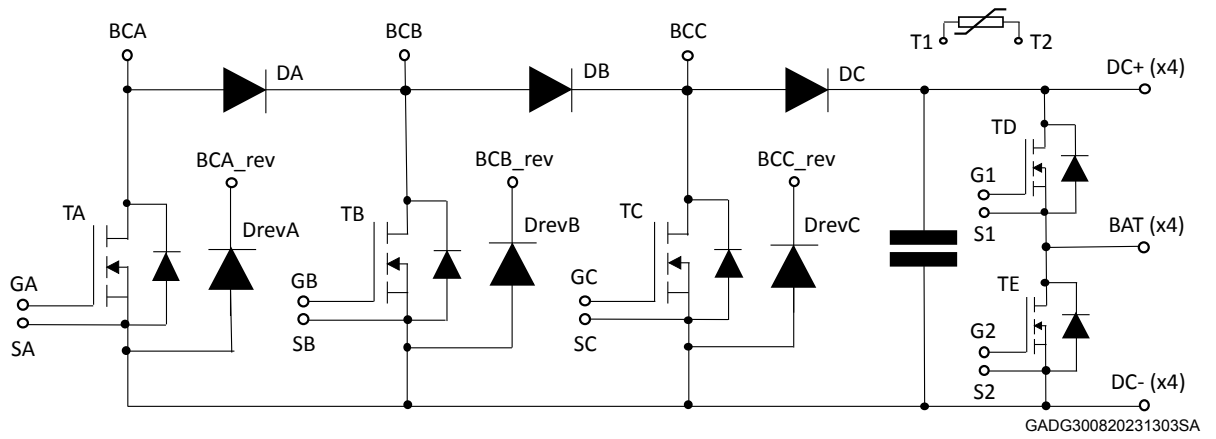
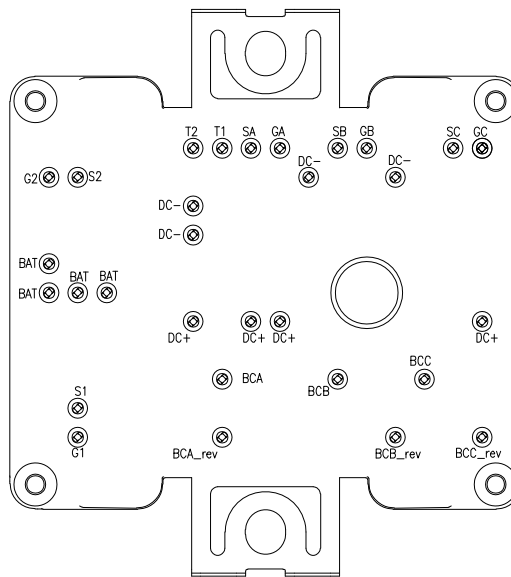


Figure 20. Package top view with pinout

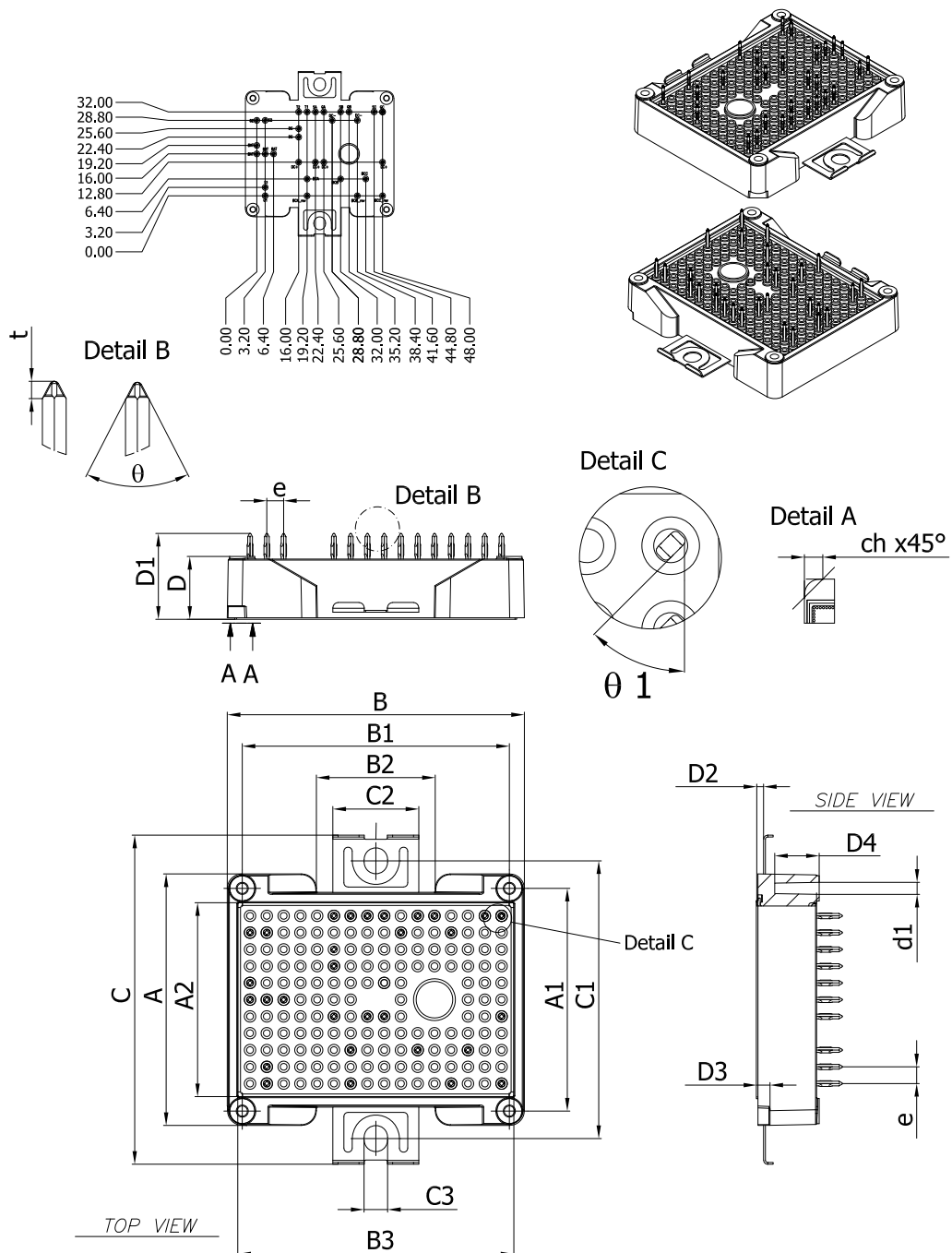


## 9 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 9.1 ACEPACK 2 triple boost plus half-bridge press-fit package information

**Figure 21.** ACEPACK 2 triple boost plus half-bridge press-fit package outline (dimensions are in mm)



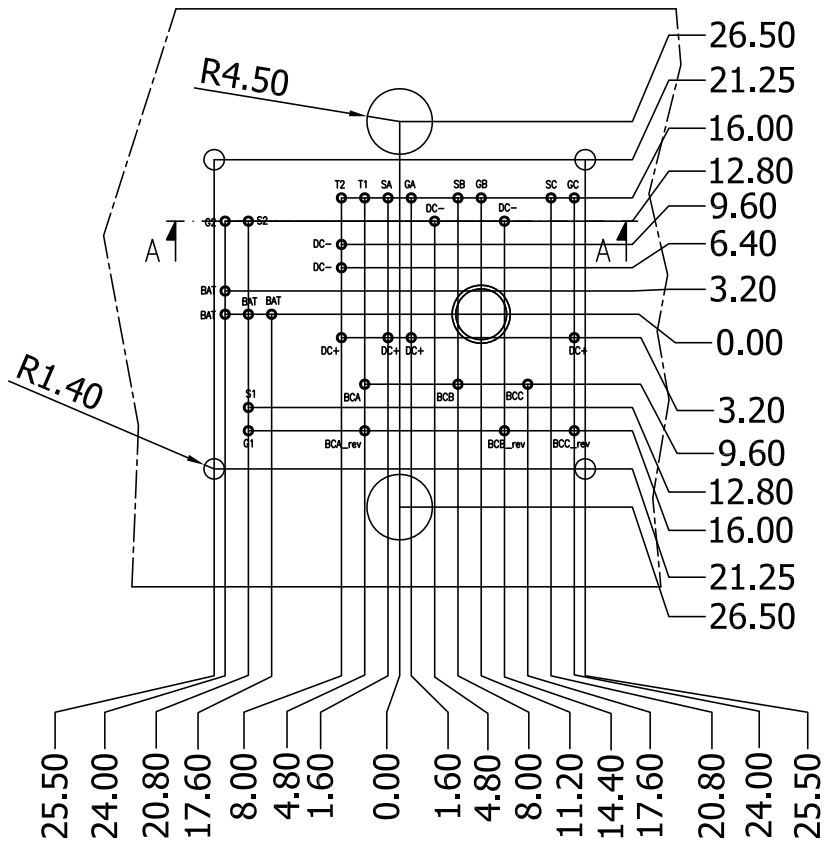
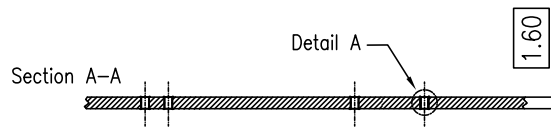
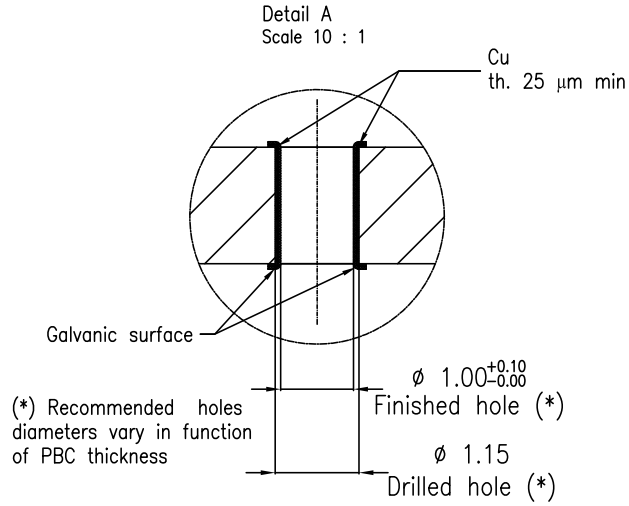
8569722\_15\_TripleBoost



**Table 20. ACEPACK 2 triple boost plus half-bridge press-fit mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	47.70	48.00	48.30
A1	42.30	42.50	42.70
A2	37.00 REF		
B	56.40	56.70	57.00
B1	50.85	51.00	51.15
B2	22.40	22.70	23.00
B3	52.70 REF		
C	62.30	62.80	63.30
C1	52.90	53.00	53.10
C2	16.20	16.40	16.60
C3	4.40	4.50	4.60
D	11.65	12.00	12.35
D1	15.90	16.40	16.90
D2	1.10	1.30	1.50
D3	2.30	2.50	2.70
D4			8.50
t	0.30	0.40	0.50
$\theta$	52°	60°	68°
$\theta_1$		45°	
e	3.20 BSC		
d1	2.30 REF		
ch	3.50 REF		

**Figure 22. ACEPACK 2 triple boost plus half-bridge press-fit recommended PCB holes layout (dimensions are in mm)**



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## Revision history

**Table 21. Document revision history**

Date	Revision	Changes
26-Jan-2024	1	First release.
15-Oct-2024	2	<p>Modified <i>Features</i>, <i>Section 1: SiC MOSFET (TA, TB, TC)</i>, <i>Section 3: SiC diode (DA, DB, DC)</i>, <i>Section 4: Rectifier diode (Drev A, B, C)</i> and <i>Section 2: SiC MOSFET (TD, TE)</i>.</p> <p>Added <i>Section 1.1: Electrical characteristics diagrams (TA, TB, TC)</i>, <i>Section 2.1: Electrical characteristics diagrams (TD, TE)</i>, <i>Section 3.1: Electrical characteristics diagrams (DA, DB, DC)</i> and <i>Section 4.1: Electrical characteristics diagrams (Drev A, B, C)</i>.</p> <p>Added <i>Section 6: DC link capacitor (C1210X473KDRACTU)</i>.</p> <p>Minor text changes.</p>
28-Oct-2024	3	Updated title, <a href="#">Features</a> , and <a href="#">Application</a> in cover page.

## Contents

<b>1</b>	<b>SiC MOSFET (TA, TB, TC)</b> .....	<b>2</b>
1.1	Electrical characteristics diagrams (TA, TB, TC) .....	4
<b>2</b>	<b>SiC MOSFET (TD, TE)</b> .....	<b>5</b>
2.1	Electrical characteristics diagrams (TD, TE) .....	7
<b>3</b>	<b>SiC diode (DA, DB, DC)</b> .....	<b>8</b>
3.1	Electrical characteristics diagrams (DA, DB, DC) .....	9
<b>4</b>	<b>Rectifier diode (Drev A, B, C)</b> .....	<b>10</b>
4.1	Electrical characteristics diagrams (Drev A, B, C) .....	11
<b>5</b>	<b>NTC</b> .....	<b>12</b>
<b>6</b>	<b>DC link capacitor (C1210X473KDRACTU)</b> .....	<b>13</b>
<b>7</b>	<b>Package</b> .....	<b>14</b>
<b>8</b>	<b>Electrical topology and pin description</b> .....	<b>15</b>
<b>9</b>	<b>Package information</b> .....	<b>16</b>
9.1	ACEPACK 2 triple boost plus half-bridge press-fit package information .....	16
	<b>Revision history</b> .....	<b>19</b>

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